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Low Power SRAM Design with Reduced Read/Write Time

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Abstract

This paper explores the design and analysis of Static Random Access Memories (SRAMs) which focusses on optimizing delay and power. CMOS SRAM cell consumes very less power and have less read and write time. Higher cell ratios can decrease the read and write time and improve stability. PMOS transistor with less width reduces the power consumption. In this paper, 6T SRAM cell is implemented with reduced read and write time, delay and power consumption. It has been noticed often that increased memory capacity increases the bit-line parasitic capacitance which in turn slows down voltage sensing, to avoid this problem use optimized scaling techniques and further, get improve performance of the design.

Keywords: Six transistor SRAM, Delay, Power, Aspect ratio.

1. Introduction

Low power SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory [P. Barnes2010, S. Hesley, et.al, 2009]. Due to the increased integration and operating speeds, power dissipation has become an important consideration both as well as due to the explosive growth of battery operated appliances.

There are two purposes of an SRAM (Static Random Access Memory) design: First is to provide a direct interface with the CPU at speeds not attainable by DRAMs and second is to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. The second driving force for SRAM technology is low power applications. In

this case, SRAM are used in most portable equipment because the DRAM refresh current is several orders of magnitude more than the low-power SRAM standby current.

We started to design SRAM with two objectives, first to lower the operating voltage from 3V to 1.8V. Second to reduce active and static power consumption for battery operated application. But it has been observed that the stability of memory is seriously affected by the decrease in supply voltage (V_{dd}) [Evelyn Grossar 2006]. By optimizing the aspect ratio of the memory and improving the pre-charge circuitry we can achieve these goals. For a stable operation of SRAM, cell ratio must be in order to 1.5 -2, along with the pull up ratio lower than the 1.8. These ratios are standard for 0.25u technology [Jan M. Rabaey 2003]. In 0.18u technology these ratio is varied for getting desired performance. One new technique is used for reducing the power of the memory cell. Although, this technique is discussed in [Stefan Cosemans 2007], some other work also been published in literature [Kenneth W.Mai, 1998,K.Takeda et.al.,2006] for low power and High Speed SRAM. But most of the work is done on peripheral circuitry for reducing the power and increasing the speed. According to the First it shows the designing of 6T SRAM cell with conventional bit-lines, than 6T with short buffered bit-line is presented for reducing both power consumption and delay. Thirdly the stability of cell is accurately measured while this work

2. Methdology

A CMOS SRAM cell is made up of six MOSFETS which has lower power consumption in standby mode and a greater immunity to transient noise and voltage variation than 4T resistive load cell just because it is preferred over resistive load cell for high speed low power operation. The storage cell has two stable states denotes by 0 and 1. Other than two inverters two additional access transistors serve to control the access to a storage cell during read and write operations. Access to the cell is enabled by the word line (WL) which controls the two access transistors M5 and M6 which, in-turn, control whether the cell should be connected to the bit lines: BL and BLB. Although it is not strictly necessary to have two bit-lines, global bit-line arrangement is helpful to maintain the stability of the cell and reduce the voltage swing which have initial impact on the power dissipation of the cell. Another advantage is, it reduce the complexity of the SRAM cell.

During read access, Pre-charge circuitry is used for differential sense amplifier at the end of the bit-line which are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs. The symmetric structure of SRAM allows for differential signalling, which makes small voltage swings more easily detectable.

Cell has three different states:

Standby: Idle circuit
If the word line is not active then M5 and M6 disconnect the cell from the bit lines and the two cross coupled inverter will continue to reinforce each other as long as they are connected to the supply.

Reading: Data has been requested
It totally depends on pre-charging concept, as both the bit-lines and word line are active high. Sometimes a small delta delay is occurred across the bit-lines which will resolved by attaching a sense amplifier at the end of the cell. The higher the sensitivity of sense amplifier, the faster the speed of read operation.

Writing: Updating the contents
Whatever the value we want to written same value is applied to the bit-lines. Bit-line input drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross coupled inverters. Careful sizing of the transistors in an SRAM is needed to ensure proper operation.

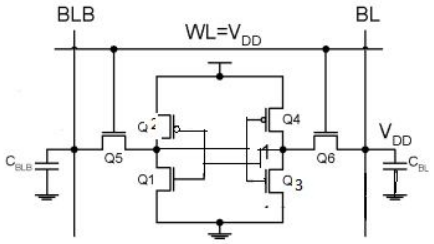

Fig. 1: 6T SRAM cell.

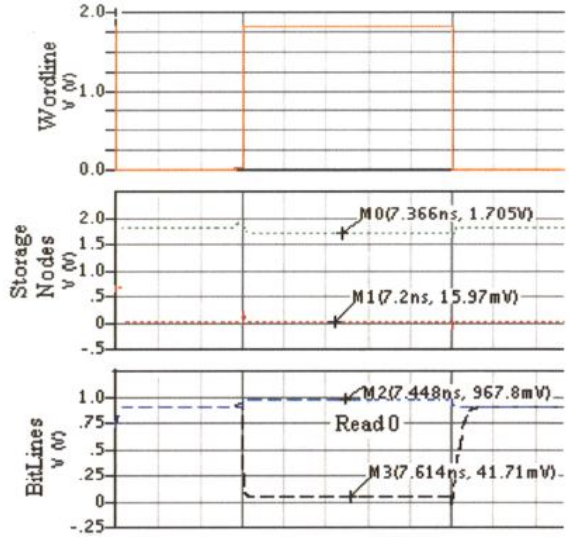

Fig 2: Read Operation

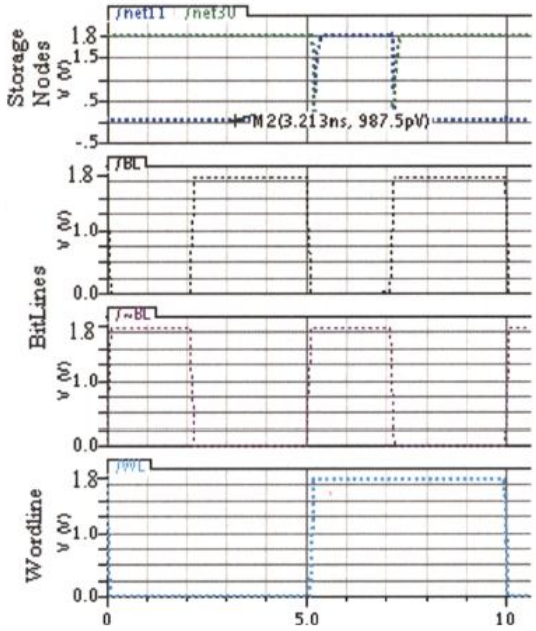

Fig. 3: Write Operation.

Optimum sizing [S. Subbanna 2006, G.G. Shahidi, et al 2010] is required for various factors like minimum delay, power, vary aspect ratio (W/L ratio) [K. Itoh 2006, A.P. Chandrakasan et al. 2009]. Delay analysis also been done by varying the capacitances.

3. Results

Stable Data retention remains the main objective when designing a cell and to maintain it aspect ratio of each transistor in the gain factor is varied. On varying capacitance values and aspect ratio, we get a minimum delay as well as less power consumption.

Table 1: Simulation results after varying aspect ratio keeping capacitance constant

Aspect ratio of MOSFET		Effect on parameters	
NMOS (W/L)	PMOS (W/L)	C_{cap} Value	Delay Factor(t_d)
1 µ	2 µ	1pf	0.025ns
2 µ	4µ	1pf	0.021ns
4 µ	8 µ	1pf	0.016ns

Table 2: Effect of capacitance variation on Delay factor.

NMOS (W/L)	PMOS (W/L)	C_{cap} Value	Delay Factor
1 µ	2 µ	5pf	0.011ns
4 µ	8 µ	10pf	0.009ns

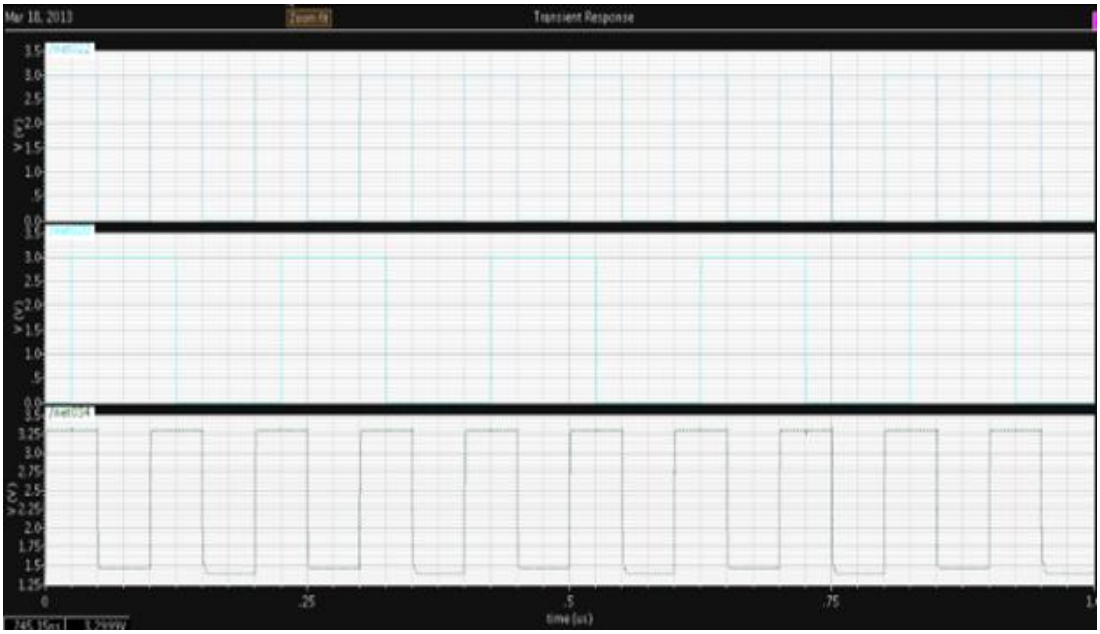

Fig. 4: Waveform of the cell.

4. Conclusion and Future Scope

The SRAM is designed for high speed operation, with low power technique by using small voltage swings on the bit-lines during write operation. Cell is being modified such that it is used as a latch type sense amplifier to amplify and store the small swing write data presented on the bit-lines which reduces power and delay factor.

Parameters	Result from Literature survey[x]	Result obtained from Proposed design
Process Technology	0.25um	180nm
Power supply voltage	2.5v	1.8v
Pre-charge voltage	0.9v	1v
Power consumption	3.4mW	3.146mW
Delay	3.4ns	2.ns

[x]Results are taken from the design described in[Bharadwaj S. Amrutur 1999].

Scaling will affect delay and power of SRAMs as a function of their size and technology. Simple analytical models for delay are used to explore range of design possibilities.

In future, lekage current will play a vital role to reduced power consumption. By creating a layout of own transistors from standard library of cadence tool, cell area will be reduced significantly.

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