Hybrid filter with CPPM for Suppression of Common Mode Voltage and Differential Mode Harmonics in Three Phase PV Inverter

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Abstract

In Pulse Width Modulation (PWM) Inverters, the peaks of output Common Mode Voltage (CMV) are very high due to the instantaneous imbalance of 3-Phase Voltages. The CMV will produce a huge pulsating Common Mode Current (CMC) through the distributed capacitance of the system and will cause the high shaft voltage leads to damage of the motor bearing. The CMC could interfere with the adjacent devices along the ground wire and even will result in the wrong operation of the devices. The Differential Mode (DM) is conducted on the signal line and ground line in the opposite direction to each other, which causes harmonics there by noise in the line and will, distorts the system. In this paper, a Hybrid filter is used to reduce the CMV and DM harmonics in a three-phase inverter with Carrier Peak Position Modulation (CPPM).In the proposed scheme, hybrid filter is implemented for Photovoltaic (PV) based inverter fed 3-Phase Induction motor with a modified RCC MPPT technique. The above scheme is implemented in Simulink environment of the MATLAB.

Keywords: Carrier peak position modulation (CPPM), common-mode voltage (CMV), differential-mode(DM) harmonics, Ripple current correlation maximum power point tracking(RCC MPPT), hybrid filter.

I. INTRODUCTION

In the engine control frameworks driven by heartbeat width regulation (PWM) inverters, the tops of yield regular mode (CM) voltage are high because of the momentary awkwardness of three phase voltages. The CM voltage (CMV) will
deliver a colossal throbbing CM current (CMC) through the conveyed capacitance of the framework[1],[2]. The Common Mode bearing current produced through the electrostatic/capacitive coupling between the stator and the rotor windings[3],[4]. Most available control patterns are focused on space-vector modulation (SVM) in recent studies [5],[6]. For the inverter with the spasmodic PWM (DPWM) methodology [7], [8], the CMV is lessened by maintaining a strategic distance from the era of zero vectors. Under various bearer extremity blends there are distinctive DPWM techniques, for example, dynamic zero state PWM (AZSPWM)[9], remote state PWM (RSPWM)[10], close state PWM (NSPWM)[11]. For the sinusoidal PWM (SPWM) control inverter, the CMV can be diminished by utilizing the carrier phase shift (CPS) methodology. High common-mode voltage (CMV) of an output will be produced in the conventional sinusoidal pulse width modulation three-phase inverter. Although the carrier phase-shift method can be used to reduce the peaks of CMV, it has the best suppression effect only when the SPWM modulation index is no more than 2/3. This letter presents a new scheme of carrier peak position modulation (CPPM) to break the limitation of modulation index. In this scheme, the peak positions of the triangular carriers are delayed or advanced to avoid the zero state. Thus, the peaks of CMV will be reduced under any modulation index [12]-[13]. At the point when the zero state shows up, rather than the standard symmetric triangular transporter, a slanted triangular bearer is utilized to tweak the reference voltages. Consequently, the zero state is maintained a strategic distance from and the CMV is decreased.

At the point when the framework is set up, the CMV dv/dt assumes a definitive part in the CMC. In the inverter, the crest estimation of the yield CMC is affected by CMV dv/dt and circulated capacitance of the framework. In previously stated procedures, albeit the yield CMVs of inverters can be decreased to ±Vdc/6, the progression level of CMV is still Vdc/3 when their switches are exchanging. CM channels can be separated into uninvolved and dynamic ones.

Dynamic CM channels are of more mainstream concern. In some dynamic channels, the dynamic gadgets are working in the straight area and the inversion voltage is delivered to repay the CMV of the three-phase inverter [14]. Most inactive channels are acknowledged with two regular ways: a CM stifle or CM transformer falling into the fundamental circuit; a resistor-capacitor(RC) or resistor-inductor-capacitor (RLC) lessening system paralleling into the primary circuit. The downsides of detached CM channels are as per the following: its cumbersome size, high power misfortune, and so on. The dynamic channel is actualized by utilizing a multi-level inverter and the four-level voltage is respected balance the CMV. Under the CPPM technique, the yield CMV of the inverter will be just two level. So the dynamic CM channel in the crossover channel is intended to be a basic half-connect structure, which can be utilized to balance all the CMV. The single tuned channel and the current low-pass channel shape an aloof DM channel. The hybrid filter is implemented for Photo Voltaic(PV) based inverter fed 3-phase Induction motor with a modified RCC MPPT technique[16]. The RCC MPPT is reduced component count which makes the implementation easier.
II. CMV IN THREE-PHASE INVERTER

In the three-phase inverter as shown in Fig. 1, the output CMV $v_{cm}$ can be expressed as

$$V_{cm} = \frac{(v_a + v_b + v_c)}{3} \quad (1)$$

Where $v_a$, $v_b$, and $v_c$ are the output voltages of three legs respectively.

Fig. 2. Modulation of three-phase reference voltages with different carriers (top), three-phase output pulses (middle) and output CMVs (bottom) in the three-phase inverter under (a) the conventional SPWM strategy, (b) the CPS strategy, and (c) the CPPM strategy.
Fig. 2(a) shows $v_a$, $v_b$, and $v_c$ are of high (or low) level, which is called the zero state, the peaks of the output CMV are maximal (about $\pm V_{dc}/2$). If the peaks of three carriers are mutually staggered $T_c/3$ ($T_c$ is the carrier cycle) in the inverter, the probability for the occurrence of the zero state will be the lowest. As shown in Fig. 2(b), the occurrence frequency and the duration time of $\pm V_{dc}/2$ in CMV are reduced greatly. In order to avoid the zero state in all cases, the variant oblique triangular carrier is used to modulate the reference sinusoidal voltage as shown in fig. 2(c).

III. OPERATING PRINCIPLE AND IMPLEMENTATION OF MPPT ALGORITHM IN 3-PHASE INVERTER CONNECTED PV SYSTEM.

For a three-phase inverter system, the value of instantaneous power $p(t)$ injected into the 3 pulsates at twice the grid frequency. This causes the dc-link voltage to oscillate at 100 Hz. For the single-stage PV system connected with 3-phase inverter given in Fig. 4, the terminals of the PV array is directly connected across the dc link capacitor, and therefore the output voltage of the PV array, $v(t)$ also oscillates at 100 Hz. The PV array current, $i(t)$ and the power fed by the PV array, $p(t)$ also contains a ripple. The ripple content of a general time varying quantity, $x(t)$ can be expressed as

$$\bar{x}(t) = x(t) - \bar{x}(t)$$

Where $\bar{x}(t)$ represents the ripple content, and $\bar{x}(t)$ represents the moving average component. The general quantity $x(t)$ can be PV array voltage, $v(t); current, i(t);$or power, $p(t). The power can be obtained by finding the product of voltage and current as expressed in(3)

$$p(t) = v(t)i(t) \rightarrow (4)$$

Fig. 5, the operating point is on right of MPP and $e(t)$ is negative. As the average value of error signal indicates the distance of the operating point from MPP, the operating point can be controlled by passing the average error signal through a PI controller.

The ripples $v(t)$ and $p(t)$ can be obtained by subtracting the average values from the respective signals using LPFs. The product of these ripples is used as input to a PI
controller. The reference signal thus obtained is compared with PV array voltage and the error obtained is passed through another PI controller to obtain the load angle.

**Fig.4.** Single-stage PV connected with 3-phase inverter

**Fig.5:** Block diagram showing implementation of the proposed MPPT algorithm.

**IV. HYBRID FILTER**
A special design of DM filter aims at the suppression of the DMV harmonics in the carrier frequency band, because the DMV harmonics will make the THD exceed the standards. Using the CPPM strategy can ensure that the output CMV will be only two-level Voltage.

**A. Active CM Filter**
In the design procedure of the active CM filter, the switching circuit structure must be determined in accordance with the characteristic of the CPPM strategy firstly.

**Fig.6:** Structure of the active CM filter.
Secondly, the coupling mode of the filter output must be designed. Lastly, the acquisition mode of the CMV signal must be selected. Because the output CMV in the inverter with CPPM is a two-level voltage, a single-phase inverter structure can be designed to generate a reverse two level voltage to the CMV.

As shown in Fig. 6, the output voltage $v_{rcm}$ of the half-bridge is $\pm kV_{dc}/2$. The counteractive voltage of the CMV can be generated. The class of the dc-side voltage in the active CM filter can be changed by the proportional coefficient $k$. The active CM filter is coupled into the main circuit of the three-phase inverter is the output current of the active circuit is injected into the main circuit through the filter network in parallel (as shown in Fig.7)

![Diagram of control signals for the active CM filter](image)

**Fig.7:** Generation for the control signals of the active CM filter under (a) the detection-control scheme, and (b) the calculation-control scheme.

It is connected to the logic circuit, the dead-time process circuit, and the gate driver through an optocoupler. One terminal of the optocoupler is Point P (its potential is $\pm V_{dc}/6$ under the CPPM strategy), the other is Point Q (its potential is $-V_{dc}/6$). This scheme has two weak points. One is the delay from “detection” to “control.” To solve the former problem, a faster optocoupler can be adopted to detect the voltage and the signal process should be simplified as far as possible in the implementation.
B. Passive DM Filter
As analyzed in Section III, the THD of the output DMV in the three-phase inverter with CPPM is substandard markedly when the carrier frequency is low. Since most harmonic energy locates in the carrier frequency band, filtering out the harmonics near the carrier frequency can greatly improve the DM characteristic of the inverter’s output.

What needs to be suppressed is mainly the carrier frequency harmonics, so a simple single tuned filter can be adopted to parallel in the line–line output of the three-phase inverter. There are two types of three-phase single tuned filters. In view of the connection with the active CM filter, the Y-type filter is better than the -type one. If the inductor $L_h$ and the capacitor $C_h$ in Fig. 7(b) are designed to satisfy the single tuned filter can greatly suppress the harmonics near the carrier frequency.

$$F_c = \frac{1}{(2\pi \sqrt{L_h C_h})}$$

C. Hybrid Filter
The hybrid filter in the design plan (see Fig. 6). In Fig. 7, the proportional coefficient $k$, which is mentioned in Part A of Section IV, is set 1/3.

From Fig. 7, it can be seen that the mid-point of the inverter dc input is equipotential with the ground in essence because of the Line Impedance Stabilization Network (LISN). Then the voltage at any point is equal to the potential difference from the point to the mid-point of the dc input. Because the output CMVs of the inverter with the CPPM strategy are $\pm V_{dc}/6$, the dc input voltage levels of the active CM filter must also be $\pm V_{dc}/6$ when $k = 1/3$. So the dc voltage of the active filter can be taken from the divided voltage of the inverter dc voltage through the middle capacitor which is one of the series capacitors on the inverter dc-side. The potentials of the middle capacitor’s two ends are just $\pm V_{dc}/6$. It will form an organic whole to connect the above designed active CM filter with the passive DM filter through the neutral point n.
VI. SIMULATION VALIDATION

Fig. 10 shows the output CMVs of the inverter under different conditions. Fig. 10(a) shows that the peaks of CMV (above 350 V and below −350 V) will appear in every carrier cycle under the conventional SPWM strategy. Under the CPPM strategy, the CMV wave is generally between −117 V and +117 V. Even if the overshoot of the jump edges is taken into consideration, the CMV peaks are not outside the range of 240 V Fig. 10 (b). In order to analyze the CMV magnitudes at different frequencies, Fig. 10 also gives the calculated FFT by the oscilloscope.

![Graphs of CMV under different strategies](image)

**Fig.10.** Simulation results of the CMV $v_{cm}$ in the three-phase inverter without a hybrid filter (a) under the conventional SPWM strategy or (b) under the CPPM strategy, and (c) with the detection-control hybrid filter or (d) with the calculation-control hybrid filter under the CPPM strategy.
Under the conventional SPWM strategy, the maximal peak of the CMV in the frequency domain is up to 44 dBV, whereas it is only about 36 dBV under the CPPM strategy. Under the CPPM strategy, the output CMVs of the inverter with the hybrid filter are shown in Fig.10(c) and (d). By using the detection control or the calculation-control hybrid filter, in the CMV there are only some spikes, whose duration is of microsecond level. The spikes do not exceed 100 V. As a result, the CMV spikes appear much more frequently in Fig.10(c). Due to the switching dead-time of IGBTs and P-MOSFETs, in the CMV with calculation-control scheme, there will also be some spikes which are slightly wider than that with detection-control scheme. The simulation results (Fig. 10(d)) show that the negative effects of the switching dead-time on CMV filtering do not occur at every switching moment and just appear one time per carrier cycle, which is much lower than the occurrence frequency of the spikes by using detection-control scheme.

![Image](image1)

![Image](image2)

![Image](image3)

**Fig.11.** Simulation results of the CMC $i_{cm}$ in the three-phase inverter (a) under the conventional SPWM strategy without a hybrid filter, and under the CPPM strategy (b) with the detection-control hybrid filter or (c) with the calculation-control hybrid filter.
Fig. 11 shows the output CMCs of the inverter under different conditions. The peaks of CMC are derived from \( \frac{dv}{dt} \) of the CMV jump edges. Under the conventional SPWM strategy, each jump step of the CMV is greater than 233 V and forms high CMC peak 1.5 A, see Fig. 11(a). The simulation FFT result of its CMC shows that the maximal peak in the frequency domain is about \(-24 \text{ dBA}\). After the hybrid filter is added in the three-phase inverter, the CMC peaks are decreased obviously. Under the calculation control scheme, the spikes of the CMC are less than 300 mA [Fig. 11(c)].

![Voltage vs Time](image1)

(a)

![Voltage vs Time](image2)

(b)

![Voltage vs Time](image3)

(c)

**Fig. 12.** Simulation results of the DMV \( v_{AB} \) in the three-phase inverter (a) under the conventional SPWM strategy or (b) under the CPPM strategy without a hybrid filter, and (c) under the CPPM strategy with the hybrid filter.

Fig. 12 shows the output DMV \( v_{AB} \) in the inverter under different conditions. The FFT results in Fig. 12(a) and (b) confirm the previous simulation conclusion: the major harmonics of the DMV are near the carrier frequency. Under the conventional SPWM strategy and the CPPM strategy without a hybrid filter, the maximal magnitudes of the DM harmonics are 20 dBV and 30 dBV respectively. As shown in Fig. 12(c), the harmonic peak of the DMV in the carrier frequency band is reduced by more than 20 dBV while the hybrid filter is added. Table V lists the THD of the output DMV in the inverter under three conditions.
VII. HARMONICS OF DMV

For the asymmetrical regular-sampled SPWM, the output voltage of Phase $r$ ($r = a, b, c$) in the three-phase inverter can be expressed by (2). In (2), $J_n$ is the $n$th order Bessel function; $f_0$ is the output power-frequency; $m$ is the carrier index; $n$ is the baseband index; $q = m + nf_0/f_c$; $\theta_{rc}$ and $\theta_{r0}$ are the initial phases of the carrier and the reference sinusoid respectively. The DMV $V_{ab}$ between Leg A and Leg B of the three-phase inverter under the conventional SPWM strategy can be deduced. Its result is revealed in (3).

$$V_r(t) = \frac{2V_{dc}}{\pi} \sum_{m=0}^{\infty} \sum_{n=1}^{\infty} \frac{1}{q} J_n\left(\frac{qMa\pi}{2}\right) \sin\left[\left(\frac{(m+n)\pi}{2}\right)\right] \cos[m(2\pi f_c t + \theta_{rc}) + n(2\pi f_0 t + \theta_{r0})]$$

(4)

$$v_{ab,SPWM}(t) = -\frac{4V_{dc}}{\pi} \sum_{m=0}^{\infty} \sum_{n=1}^{\infty} \frac{1}{q} J_n\left(\frac{qMa\pi}{2}\right) \sin\left[(m+n)\frac{\pi}{2}\right] \sin\left(n\frac{\pi}{3}\right) \sin\left[2\pi(mf_c + nf_0)t - \frac{n\pi}{3}\right]$$

(5)

$$V_{ab,PS}(t) = -\frac{4V_{dc}}{\pi} \sum_{m=0}^{\infty} \sum_{n=1}^{\infty} \frac{1}{q} J_n\left(\frac{qMa\pi}{2}\right) \sin\left[(m+n)\frac{\pi}{2}\right] \sin\left[(m+n)\frac{\pi}{3}\right] \sin\left[2\pi(mf_c + nf_0)t - \frac{(m+n)\pi}{3}\right]$$

(6)

**TABLE - I**

INITIAL PHASES OF DIFFERENT LEGS

<table>
<thead>
<tr>
<th>Strategy</th>
<th>Leg A</th>
<th>Leg B</th>
<th>Leg C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\theta_{ac}$</td>
<td>$\theta_{a0}$</td>
<td>$\theta_{bc}$</td>
</tr>
<tr>
<td>Conventional SPWM</td>
<td>0</td>
<td>0</td>
<td>-2\pi/3</td>
</tr>
<tr>
<td>CPS</td>
<td>0</td>
<td>0</td>
<td>-2\pi/3</td>
</tr>
</tbody>
</table>
Under different strategies, the DMVs of the three-phase inverter with no-load (i.e., load impedance is infinite) are simulated. The simulated parameters are listed in Table II.

**TABLE-II**

SIMULATED PARAMETERS IN THREE-PHASE INVERTER

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Commentary</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}$</td>
<td>700 V</td>
<td>DC-side voltage</td>
</tr>
<tr>
<td>$L_f$</td>
<td>900 $\mu$H</td>
<td>Inductor of low-pass filter</td>
</tr>
<tr>
<td>$C_f$</td>
<td>25 $\mu$F</td>
<td>Capacitor of low-pass filter</td>
</tr>
<tr>
<td>$f_0$</td>
<td>50 Hz</td>
<td>Output power-frequency</td>
</tr>
</tbody>
</table>

FFT) results of the DMV $v_{AB}$ under three strategies at $f_c$ = 3.6 kHz. The maximal harmonic peak of DMV usually appears at the carrier frequency. In the inverter with the conventional SPWM strategy, the $\sin(n\pi/3)$ [emphasized by dots in (3)] will cause the magnitude of DMV at $f_c$ ($m = 1$, $n = 0$) to be zero, and the $\sin[(m + n)\pi/2]$ will cause the magnitudes of DMV at the adjacent frequencies of $f_c$ (viz. $m = 1$, $n = 1$) to be zero. In this case, the harmonic peak of DMV will appear at the frequency of $f_c - 2f_0$ or $f_c + 2f_0$ [at 3.5 kHz or 3.7 kHz as shown in Fig. 13(a)].
Fig. 13: Simulated FFT results of output DMV in the inverter under the (a) conventional SPWM strategy, (b) CPS strategy for without hybrid filter, and (c) CPPM strategy for with hybrid filter at $f_c = 3.6$ kHz.
According to (4), the magnitude of DMV under the CPS strategy at $f_c$ will not be zero and even will be large. Although the harmonics of the output DMV will be somewhat reduced through the low-pass filter, the total harmonic distortion (THD) of DMV would be serious and even be substandard when the designed carrier frequency is low. In Fig. 13(b), the magnitude of the DMV harmonic at $f$ is still about 8% of the fundamental magnitude despite the fact that the low-pass filter is used.

The CPPM strategy is based on the CPS strategy. The difference between them is that the carrier peak position is changed for a short time in a small range. Hence the output DMV harmonics in the inverter with CPPM will be similar to that with CPS. Compared Fig. 13(c) with Fig. 13(b), see that the harmonic magnitude in the carrier frequency band is almost the same and the THD in Fig. 13(c) is slightly higher. Table III lists the simulated DMV THDs under different carrier frequencies. Under the condition of low $f_c$, if the CMV is suppressed by the CPPM strategy, an extra DM filter is needed to reduce the harmonics in the carrier frequency band.

### TABLE IV
Simulated THD of output DMV

<table>
<thead>
<tr>
<th>Carrier frequency</th>
<th>THD</th>
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<tbody>
<tr>
<td></td>
<td>SPWM</td>
</tr>
<tr>
<td>2.5</td>
<td>9.41</td>
</tr>
<tr>
<td>3.6</td>
<td>4.07</td>
</tr>
<tr>
<td>5.0</td>
<td>2.03</td>
</tr>
<tr>
<td>10.0</td>
<td>0.56</td>
</tr>
</tbody>
</table>

### TABLE V
Simulated THD of output line-line voltage

<table>
<thead>
<tr>
<th>Condition</th>
<th>Without hybrid filter</th>
<th>With hybrid filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD</td>
<td>SPWM</td>
<td>CPPM</td>
</tr>
<tr>
<td></td>
<td>4.07</td>
<td>8.07</td>
</tr>
</tbody>
</table>

**CONCLUSION**

Through the above analysis, the hybrid filter, which is designed in this paper to suppress the CMV and DM harmonics of the three-phase inverter by using RCC method MPPT technique in 3-phase PV inverter connected is simple structure, flexible in application, compatible in THD standard, easy installation.
REFERENCES


