

FPGA Implementation of PV based Quasi Z-Source Cascaded Multilevel Inverter

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Abstract

This paper presents the FPGA implementation of PV based five-level Quasi Z-source inverter (QZSI). PV is mathematically modeled along with maximum power point tracking (MPPT) using perturb and observe (P & O) algorithm. Out of the reported modulation strategies, this paper deals with the phase shifted sinusoidal pulse width modulation (PSPWM) for pulse generation and maximum constant boost control technique for shoot-through generation. For the proposed topology, simulation was carried out using Matlab/Simulink. The hardware is implemented for the PV based five-level QZSI. The generation of pulses for the switches is carried out using Xilinx-Matlab interface and fused the program in FPGA-SPARTAN3E. Hardware of the proposed single-phase QZSI inverter is implemented to verify the simulation results.

Key words: Photovoltaic, Pulse width modulation, Maximum power point tracking, Field Programmable Grid Array, Phase shift PWM, Quasi Z-Source inverter

I. INTRODUCTION

Due to increasing scarcity of the conventional energy resources, there is an alarm for finding out the renewable energy resources all over the world. One such important renewable source is solar energy. Several researches are going on to improvise the trapping of solar energy. Here, the proposed topology uses PV source for each of the bridges in the five-level cascaded QZSI. Under continuously varying insolation and temperature, it becomes essential to track the highest power point of the PV. So, Perturb and Observe algorithm is used to find out the maximum power point tracking of the PV source as it is the simplest of all MPPT algorithms and easily implementable with the requirement of measuring only a few parameters. A cascaded

H-Bridge five-level inverter with Quasi-impedance network is considered here to obtain both inversion and boost capability in a single stage. The QZSI is the sub topology and has all the advantages of Z-source inverter. In addition to that, it has continuous input current characteristic which makes it more suitable for the PV applications. Due to the capability of bearing the shoot through due to impedance network, this five level QZSI can produce boosted output voltage with reduced THD. Several modulation strategies are available for generation of shoot through states. For the proposed topology, maximum constant boost control technique is used as it has constant shoot through duty ratio. Implementation of the proposed topology in hardware requires the generation of pulses for the switches by some means. It is practically made possible using FPGA-SPARTAN3E by fusing the program built in the Xilinx-Matlab interface. The Simulink model of the pulse generation is drawn in the Xilinx-Matlab interface and the program is fused in Diligent Nexys2 FPGA-SPARTAN3E kit. The details are provided in the upcoming sections.

II. PV BASED QUASI Z-SOURCE INVERTER

Fig. 1 shows the PV based five-level cascaded H-bridge QZSI. It consists of PV sources and impedance networks separately in each of the H-bridges. The QZSI extends several advantages over the ZSI such as continuous current from the input DC source, cut down component ratings, and enhanced reliability.

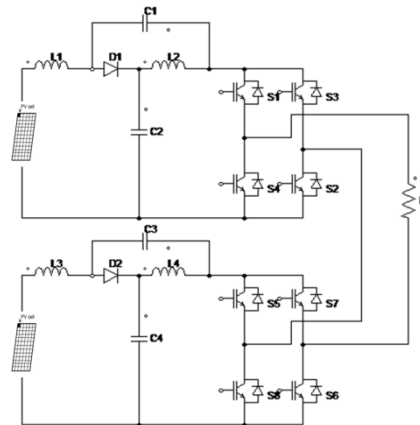


Fig. 1. PV based five-level QZSI

III. MATHEMATICAL MODELING OF PV

The PV module has been modeled using mathematical equations is shown in fig.2. The equations are given below.

Module's photo-current:

$$I_L = [I_{scr} + K_i(T - 298)] * \frac{\alpha}{1000} \quad (1)$$

Module's reverse saturation current:

$$I_{rs} = \frac{I_{sCr}}{e^{\left(\frac{qV_{OC}}{N_S K A T}\right) - 1}} \tag{2}$$

Module's saturation current:

$$I_o = I_{rs} \left[\frac{T}{T_r}\right]^3 e^{\left[\frac{qE_{g0}}{Bk} \left[\frac{1}{T_r} - \frac{1}{T}\right]\right]} \tag{3}$$

The output current of the PV module is

$$I = N_P * I_L - N_P * I_o \left[\exp \left\{ \frac{q * (V_{PV} + I R_S)}{N_S A k T} \right\} - 1 \right] \tag{4}$$

Where $V = V_{OC}$, $N_P = 1$ and $N_S = 36$, I is the PV array output current, V is the PV array output voltage, N_S is the number of cells in series, N_P is the number of cells in parallel, q is the charge of an electron, k is the Boltzmann's constant, A is the p-n junction ideality factor, T is the cell temperature in Kelvin, I_{rs} is the cell reverse saturation current [16]-[17].

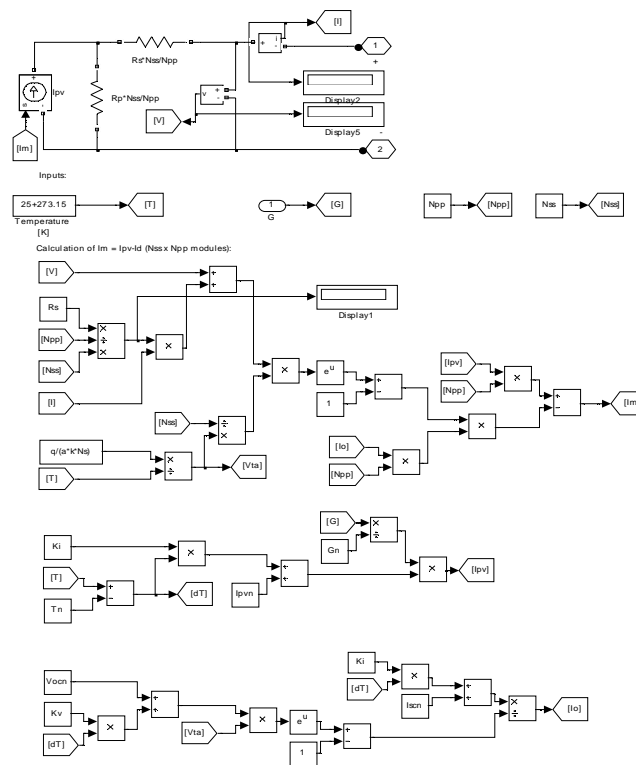


Fig.2 Mathematical modeling of PV module.

IV. IMPLEMENTATION OF PERTURB AND OBSERVE MAXIMUM POWER POINT TRACKING

In this section, the simplest of the MPPT algorithms-Perturb and Observe algorithm has

been discussed. It is implemented for the PV module that is designed in the section III. This algorithm needs the measurement of only two parameters such as PV current and voltage. By perturbing the input at definite intervals, the operating point can be driven to the maximum power point. The flow chart and the simulation model for the MPPT is shown in fig.3 and fig.4 respectively.[20]-[21]

V. QZSI OPERATION AND SWITCHING STATES

The shoot-through state is forbidden in the traditional VSI, because it will cause a short circuit of the voltage source and damage the devices. With the QZSI and ZSI, the unique LC and diode network connected to the inverter bridge modify the operation of the circuit, allowing the shoot-through state. This network will effectively protect the circuit from damage when the shoot-through occurs and by using the shoot-through state, the (quasi-) Z-source network boosts the dc-link voltage. [2],[5],[7]The equivalent circuits in the two states are shown in fig.5 and 6.The switching states of five-level QZSI is in Table 1.

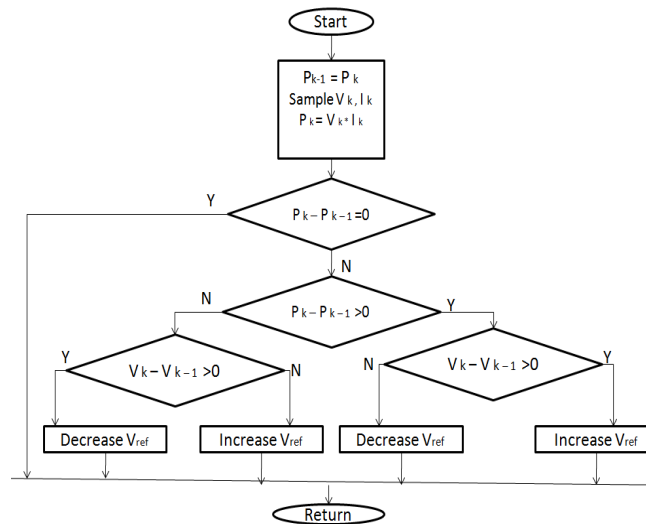


Fig 3. Flowchart of the P & O algorithm

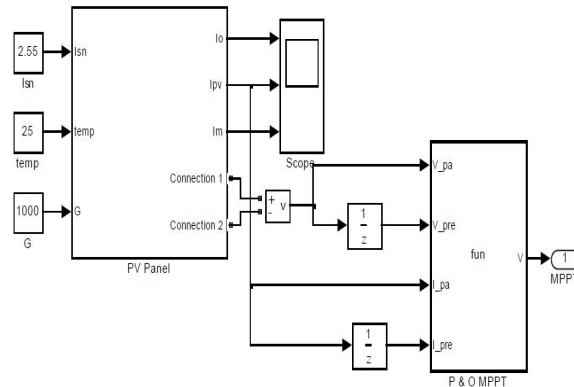


Fig 4. PV module implemented with MPPT

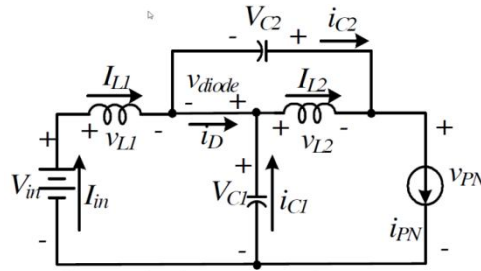


Fig.5 Equivalent circuit of QZSI in Non-Shoot through states

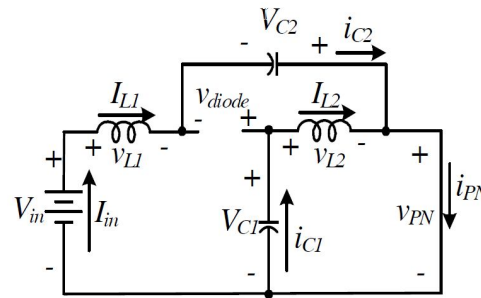


Fig.6 Equivalent circuit of QZSI in Shoot through states

TABLE I Switching States of five-level QZSI

| Output Voltage | State | ON Switches |
|------------------|---------------|------------------------------------------------------------------------------------------------|
| 2V _s | Active | S ₁ ,S ₂ ,S ₅ ,S ₆ |
| V _s | Active | S ₁ ,S ₃ ,S ₅ ,S ₆ |
| V _s | Shoot-through | S ₁ ,S ₂ ,S ₃ ,S ₄ ,S ₅ ,S ₆ |
| V _s | Active | S ₁ ,S ₂ ,S ₅ ,S ₇ |
| V _s | Shoot-through | S ₁ ,S ₂ ,S ₅ ,S ₆ ,S ₇ ,S ₈ |
| 0 | Zero | S ₁ ,S ₃ ,S ₅ ,S ₇ |
| 0 | Shoot-through | S ₁ ,S ₂ ,S ₃ ,S ₄ ,S ₅ ,S ₇ |
| 0 | Shoot-through | S ₁ ,S ₃ ,S ₅ ,S ₆ ,S ₇ ,S ₈ |
| -V _s | Active | S ₁ ,S ₃ ,S ₇ ,S ₈ |
| -V _s | Shoot-through | S ₁ ,S ₂ ,S ₃ ,S ₄ ,S ₇ ,S ₈ |
| -V _s | Active | S ₃ ,S ₄ ,S ₅ ,S ₇ |
| -V _s | Shoot-through | S ₃ ,S ₄ ,S ₅ ,S ₆ ,S ₇ ,S ₈ |
| -2V _s | Active | S ₃ ,S ₄ ,S ₇ ,S ₈ |

VI. PSPWM WITH MAXIMUM CONSTANT BOOST CONTROL FOR QZSI

In this paper, the PWM generation is carried out with phase shift sinusoidal PWM. Because it has balanced switching action and the remarkable attribute is that the phase shift angle can be used to control the output voltage of the MLI. In order to introduce the shoot-through states, three techniques are available. They are simple boost, maximum boost and maximum constant boost. Maximum constant boost has been

considered due to the constant shoot through duty ratio. In order to maintain constant duty cycle, the upper and lower shoot through values should be periodical. This control strategy is suitable for low frequency applications as the ripple in the capacitor voltage and the inductor current is highly reduced.[7]-[11] The pulse generation using PSPWM and maximum constant boost (MBC) control technique is shown in the fig.7

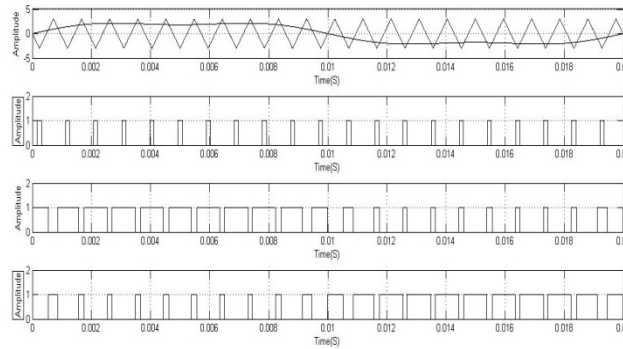


Fig.7 Pulse generation using PSPWM with MBC technique

VII. SIMULATION RESULTS

The simulation of the proposed topology has been carried out using Matlab/Simulink. The simulation parameters are shown in Table II. The simulation was carried out with an input voltage of 10 V for each bridge and switching frequency of 1 kHz.

TABLE II SIMULATION PARAMETERS

| PV Parameters | Rating | QZSI Parameters | Rating |
|-----------------------|-----------------------|--------------------------|-----------------|
| Open circuit voltage | 21.24 V | Input Voltage per bridge | 10 V |
| Short circuit current | 2.55 A | Inductors | 5mH |
| No of cells | 36 | Capacitors | 1150 μ H |
| Insolation | 1000 W/m ² | Inductor resistance | 0.0005 Ω |
| Ideality factor | 1.5 | Capacitor resistance | 0.005 Ω |
| Operating temperature | 298 K | Boost Factor | 1.66 |
| | | Switching frequency | 1 kHz |

The output voltage waveform for the simulated five-level QZSI is shown in fig.8. For an input voltage of 10 V at each bridge from the PV source, the output voltage is boosted to 40V.

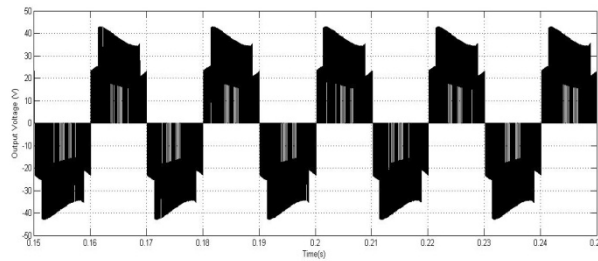


Fig 8. Output Voltage of five-level QZSI with MBC technique

VIII. FPGA IMPLEMENTATION FOR PULSE GENERATION

The pulse generation for the switches in the hardware prototype is made easily possible by the use of FPGA-SPARTAN3E. The Xilinx Matlab interface is essential for the generation of pulses in a way similar to that of the Simulink model. But here, the creation of carrier wave and reference wave is fully based on counter and the explicit period of the clocking signal. The block diagram of the pulse generation using FPGA is shown in the fig.9

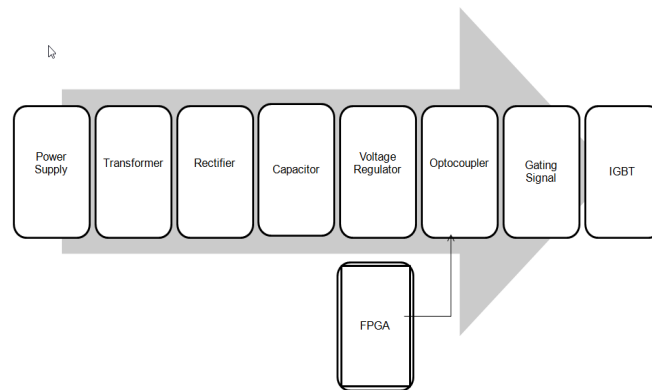


Fig.9 Block diagram representing the gating circuit using FPGA

IX. STEPS TO IMPLEMENT FPGA-SPARTAN3E BASED PULSE GENERATION

The flow chart for the steps to implement the FPGA based pulse generation is given in fig.10

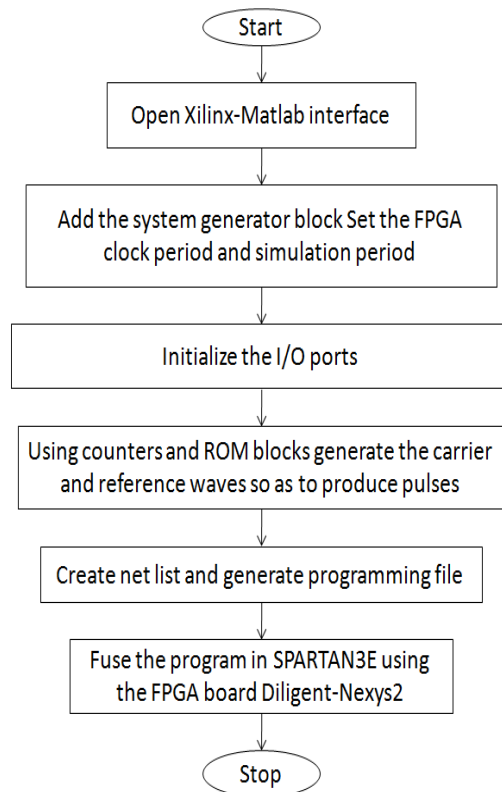


Fig.10 Flow chart for the steps to implement the pulse generation using FPGA-SPARTAN3E

X. GATING PULSE GENERATION PATTERN USING FPGA-SPARTAN3E

The pulse generation circuit in the Xilinx-Matlab interface is shown in fig.11

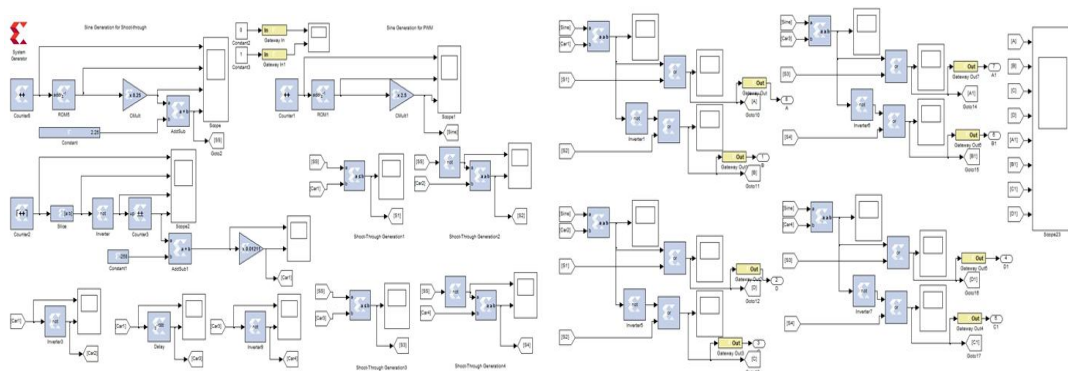


Fig 11. Pulse generation using Xilinx-Matlab interface

The pulse generation is similar to that generated using Matlab-Simulink software. The maximum constant boost implemented with PSPWM. The generated pulses for the switches using Xilinx-Matlab interface has been implemented in hardware using Digilent-Nexys2. The Nexys2 has SPARTAN3E FPGA for fusing the program. The netlist for the program was generated and the program was fused to FPGA so as to generate pulses in the output ports of the Digilent-Nexys2. These pulses are then given to the gating circuit so as to provide pulses to the IGBT's. Figure12 shows the hardware setup for the pulse generation using FPGA-SPARTAN3E.

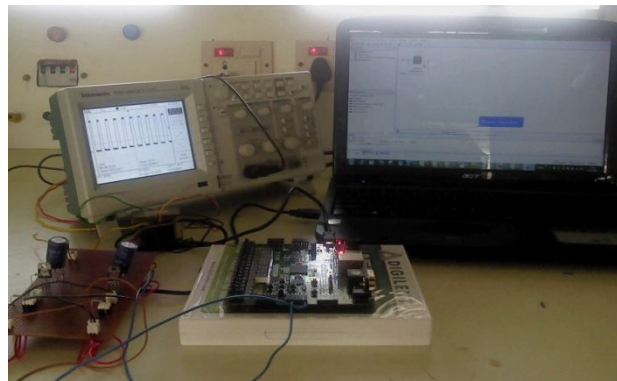


Fig 12 Hardware setup for the pulse generation using FPGA-SPARTAN3E

The pulse pattern obtained is shown in fig 13. It is same as that of the pulses obtained using Matlab-Simulink.

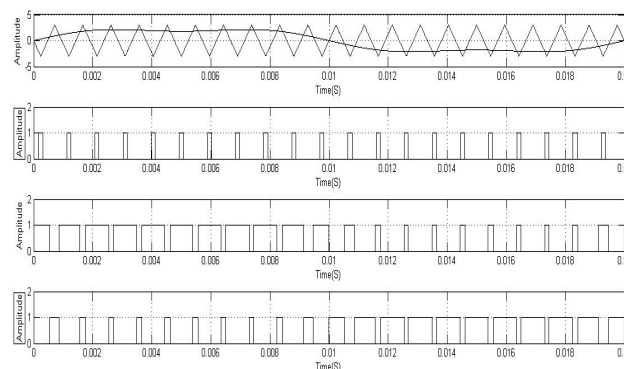


Fig 13. Pulse pattern obtained using FPGA –SPARTAN3E

XI. HARDWARE PROTOTYPE THE FIVE LEVEL CASCADED H BRIDGE QUASI Z SOURCE INVERTER

The hardware prototype of the impedance network and the five-level cascaded H bridge quasi Z-source inverter are shown in the fig 14. It has been sourced with PV panels of 9V rating. The maximum constant boost implemented phase shifted PWM

was generated using Xilinx-Matlab interface and the program was fused to NEXYS2-SPARTAN3E. These pulses were given to the gating circuit which was developed using Printed Circuit board (PCB). The impedance network was made as per the design and connected between PV source and the cascaded H-bridge network. The whole interface setup is shown in the below picture. Table III provides the components used for the hardware implementation of the proposed topology.

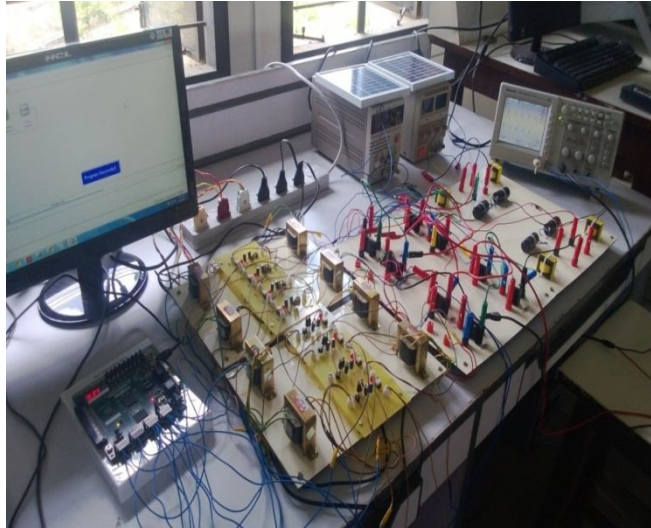


Fig.14 Hardware Prototype of the five-level QZSI

TABLE III COMPONENTS USED FOR HARDWARE IMPLEMENTATION

| Name of the component | Specification |
|------------------------------|----------------------|
| Optocoupler | MCT2E |
| Rectifier | W08 |
| Transformer | 15-0-15 V |
| Voltage Regulator | 7812 |
| Capacitor | 1000 μ F,63 V |
| IGBT | FGA25N120 |
| Solar Panel | 9V,3W |
| Dilligent-Nexys2 | SPARTAN3E |

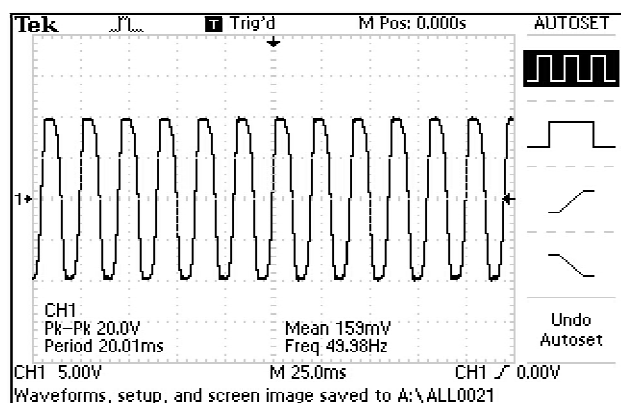


Fig.15 Output Voltage obtained from the hardware prototype of five-level QZSI

The output voltage obtained from the developed hardware model of the five-level cascaded H bridge quasi Z-source inverter is shown in the fig.15. The output voltage is boosted to 20 V for an input voltage of $\sim 7V$ at each stage of the bridges using PV panels. The voltage has been boosted approximately to match the boost factor of 1.66.

XII. CONCLUSION

In this paper, the PV based cascaded H Bridge Quasi Z source multi-level inverter was analyzed. Its impedance network was designed for a switching frequency of 1 kHz. The phase shift carrier technique was implemented with maximum constant boost control as it resulted in low THD and low voltage stress compared to other multicarrier PWM techniques. With PV open circuit voltage of 10 V, the output voltage obtained was 40 V which is approximately 1.66 times the input voltage. Therefore, the proposed MLI eliminates the intermediate DC-DC converter and proves to be a suitable candidate for PV as it provides a higher gain and reduced cost.

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