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Design and Fabrication of Micromachined Absolute Micro Pressure Sensor

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Abstract

Absolute micro pressure sensors have been designed and fabricated in batches, which will be capable to give output responses in form of voltage signal as a function of pressure. The piezoresistive effect has been chosen for this device because it provides an observable resistance changes that is a linear function of pressure and is observable at low stress levels. A membrane is used as a stress-magnifying device. The pressure-induced stresses in the membrane are sensed by properly oriented piezoresistors interconnected to form a bridge. For the purpose of pressure sensing, boron doped polysilicon piezoresistors have been fabricated in half Wheatstone bridge configuration. A 100 µm sized square membrane, over which polysilicon resistors are deposited, has been realized having thickness of 0.8 µm with the help of a sacrificial layer of LPCVD polysilicon thin film. Highly selective anisotropic etching of silicon has been performed in 45% wt KOH at 75 ^{o}C for conical cavity formation under the membrane. The developed fabrication process is competent to provide nearly 1089 chips of 1mm x 1mm size on a two-inch diameter silicon (100) wafer.

Keywords: LPCVD, Polysilicon, Piezoresistors, Etching, MEMS and Membrane

Introduction

Micromachined pressure sensors have found wide applications in areas such as automotive systems, industrial control, environmental monitoring and biomedical diagnostics. In recent years, substantial research has been carried out on micromachined, diaphragm type pressure sensors [1, 5]. These sensors are fabricated by means of new manufacturing technologies such as bulk-micromachining [6, 7] or surface micromachining [8, 9]. Many of them use silicon and its piezoresistivity as the detection mechanism. These transducers function when the resistivity of the sensing resistors changes as the diaphragm deflects due to applied pressure. Since the piezoresistive effect was discovered, the piezoresistive sensors have been widely employed in mechanical signal sensing. Pfann and Thurston [10] designed several types of semiconductor stress gauges to measure the longitudinal, transverse and shear stresses, as well as torque. Pressure sensors based on piezoresistive characteristics of polysilicon film on Si (100) have potentials due to ease in its integration with microelectronics leading towards the realization of Micro-Electro-Mechanical-Systems (MEMS) employing smart sensors [11, 12]. A piezoresistive pressure sensor consists of three major active components namely, a membrane, piezoresistors and their configuration. These three components are responsible for the sensitivity of the device. The most common configuration is the Wheatstone bridge [13, 14]. Sensitivity of the bridge, however, depends on the location of the resistors on the membrane. The strained membrane offers a stress profile in the form of fringes of tensile and compressive stresses, particularly near the edges of a membrane. The width and the sharpness of these fringes depend upon the area and thickness of the membrane. In order to increase the sensitivity of the pressure sensor, the membrane thickness should be thin to maximize the load deflection responses. In addition to this, location of piezoresistors on the membrane and their shape, contribute significantly in influencing the resolution of the Wheatstone bridge. On the membrane, piezoresistors are delineated using conventional microelectronic process, comprising of optical photolithography, CVD techniques for polysilicon film deposition and doping techniques to bring down the resistivity of the film. The most important task during KOH etching for the cavity formation is to handle mask edge alignment with the cavity edges otherwise yields of the device will be zero percent [15, 16].

Nowadays the silicon piezoresistive pressure sensor is considered a mature technology in the industry. Therefore, sensor-manufacturing costs become more significant in sensor design considerations. Several studies have investigated the pressure sensor to reduce the manufacturing cost and time. One of the solutions is using a thinner wafer. However, this solution becomes increasingly more difficult as the thickness of the wafer becomes thinner [17]. Another solution is to etch from the front side of the silicon wafer. P. A. Alvi et al. [18] etched the silicon wafer from the front side laterally and sealed it by using CVD techniques.

This study presents a novel fabrication technique of a silicon based piezoresistive pressure sensor to reduce its mass production cost and to simplify its fabrication process. The process sequence is important for its optimization. In the following sections of this paper, the fundamental theory, design parameters and fabrication process of these pressure sensors are first discussed and systematic approach adopted to develop the technology for the fabrication of the device is then presented.

Designing

In layout of the device i.e. Micro pressure sensor, as shown in figure (1), the hatch-lined objects are the resistors, square box with dotted lines is the membrane, the two blacken rectangles are the etch holes through which etch material enters in the bulk of the substrate, five square boxes towards the periphery are the contact pads and the lines from resistors to these pads are the metal contact lines. The corresponding design parameters are mentioned below;

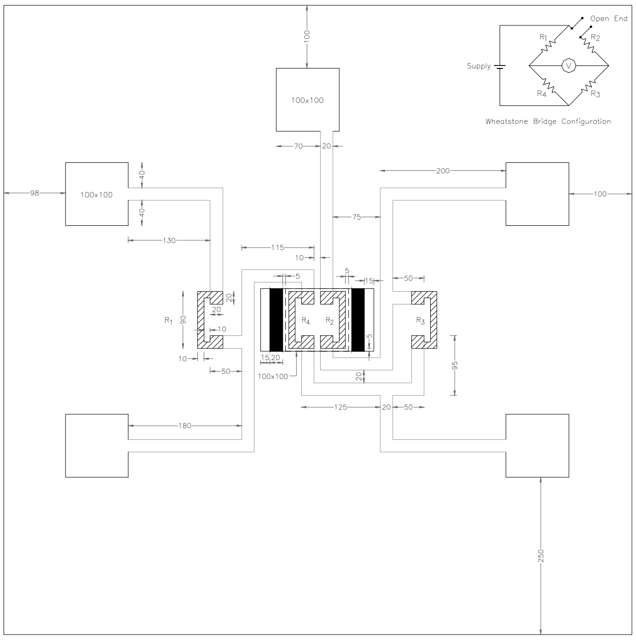

Figure 1: Schematic diagram of the Layout of the micro pressure sensor.

Chip size : 1mm x 1mm
Membrane size : 100 µm x 100 µm
Membrane thickness : 0.7 µm
Resistor’s configuration : half- Wheatstone bridge
Resistor’s length : 110 µm
Resistor’s width : 10 µm
Resistor’s pad size : 20 µm x 20 µm
Resistor’s thickness : 1.0 m
Metal contact pad size : 100 µm x 100 µm
Metal contact line width : 20 µm
Resistor’s value : 0.22 KΩ
Sheet resistivity of resistors: 20 Ω/□

The Wheatstone bridge configuration of the resistances over the membrane contributes maximum in influencing the sensitivity of the device. This also includes the shape and location of each piezoresistors of the configuration. The ratio of the two resistances in each branch of the Wheatstone bridge is the parameter, which is crucial to optimize the sensitivity of the sensor as a whole. The change in the resistances due to strain on the membrane develops potential difference, which translates the applied pressure. In order to increase the sensitivity of the bridge, the resistors are placed on the membrane so as to get maximum change in potential difference.

In the present work, any two opposite resistors of the bridge configuration are placed on the membrane where stress will occur and the other two outside the membrane where stress will not occur. The output voltage signal under the pressure applied is given by

$$V_{out} = \frac{2 \cdot R_n . \Delta R_e}{(R_e + R_n)^2} V_{in}$$

Where R_e (called effective resistance) and R_n (called non-effective resistance) are the values of resistors placed on strained membrane and outside the membrane, respectively. R_e is the change in the effective resistance due to pressure exerted on the membrane.

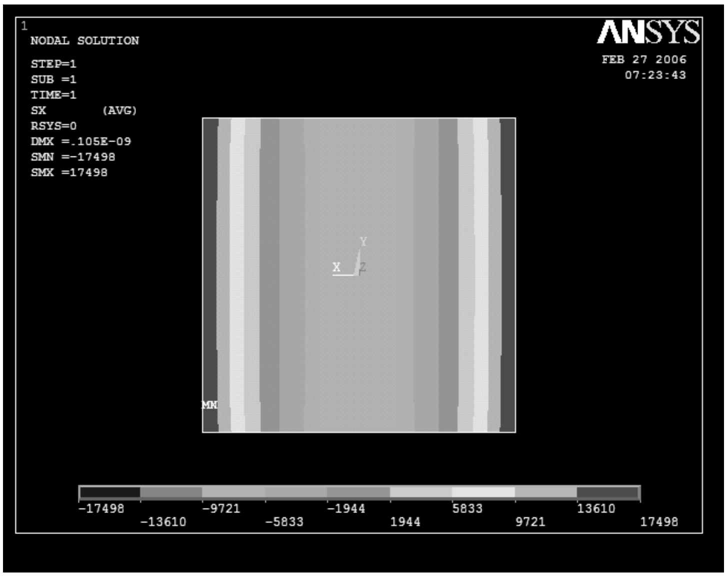

Figure 2: Simulated stress profile of a strained composite membrane of thickness 0.8 μm on application of 344-psi pressure.

The simulated stress profile, shown in Figure 2, is the result of analysis of the device membrane using ANSYS software. From this, it is clear that stress is maximum at the edges and decreases as it moves away towards the center. Accordingly, the design layout with the resistors oriented in the transverse direction should give more sensitivity, as the resistors will experience maximum stress and hence maximum piezo-effect. The shapes of the resistors are chosen to ensure maximum length that can be accommodated in the membrane. The actual size of the membrane is kept 100μm x 100μm to realize a miniature sized pressure sensor- a micro sensor so that it will be compatible with other microelectronic devices. Keeping the width of the resistors 10μm and a square of 20μm x 20μm for contacts of contact lines, the total length comes out to be 150μm. Since the square of 20μm x 20μm is on either ends and is to be connected with the conducting metals, the net length of the resistors is only 110μm for 100μm x 100μm membrane.

Piezoresistors deposited over the membrane are made of boron-doped polysilicon because of good piezoeffect. Polysilicon has better stability and can be used in operating temperature up to 200 ^{o}C. With increasing polysilicon layer thickness the sheet resistivity decreases. For 1.0μm thick poly Si layer the sheet resistivity can be brought down in the range of 15-20 Ω/□. This way by controlling the polysilicon layer thickness, values of the polysilicon resistors can be designed for the given membrane.

The dimension of the sacrificial layer (polysilicon), to realize cavity later on, is kept 180μm x 100μm with 40μm each extending on either sides from the membrane dimensions. This is done so that etch holes of sufficient dimension can be accommodated beyond the actual membrane but within the dimension of sacrificial layer. This condition is necessary for sealing the cavity in the later stage. The dimension of the etch hole is kept 20μm x 100μm, maintaining 5μm from the membrane edge on either side. This dimension for etch hole is sufficient to provide passage for wet etchant to create cavity. The width of the metal contact lines are kept 20μm and the minimum gap between two contact lines is tried to keep at least twice its width. The dimension for metal contact pads is kept 100μm x 100μm. Here five pads are used instead of four since one of the arms is opened. This provision is for the purpose of balancing the bridge externally if required and if not required then by shorting, it can be used normally. Leaving sufficient space on all the sides, the size of a single chip comes up to be 1mm x 1mm. This is a pretty small size. Leaving grid size of 0.1mm (the size that can be comfortably run by die-slicer blade), the numbers of devices that can be fabricated on a single wafer of 2 inches diameter after leaving sufficient space for alignment marks on either side are an array of 33 x 33 giving 1089 devices.

Fabrication Process

A p-type silicon wafer of diameter 2 inch with (100) orientation and thickness of 280±20 microns is the starting substrate (see fig. 3). For a proper V-shape cavity formation, silicon with (100) is the ultimate choice. The absolute micro pressure sensors are constructed by using lateral front-side etching technology, a combination of bulk and surface micro machining technology. The process starts with cleaning the wafer followed by following sequence:

(1) SiO_2 thermally grown.
(2) Si_3N_4 (LPCVD).
(3) PLG-1 (window opening), RIE of Si_3N_4 + wet etching of SiO_2.
(4) Polysilicon deposition (sacrificial layer) by LPCVD.
(5) PLG-2 + RIE (for Poly etch).

(6) PECVD of ($Si_3N_4 + SiO_2 + Si_3N_4$), then annealing.
(7) LPCVD polysilicon
(8) Boron Doping of Poly Si for piezoresistorsPLG-3 + Poly etch (for defining resistors)
(10) Metallization of Al for resistor pads and contact lines
(11) PLG-4 + Wet etching of Al
(12) APCVD SiO_2 + PECVD Si_3N_4
(13) PLG-5 + RIE of composite layer ($Si_3N_4 + SiO_2 + Si_3N_4$)KOH Etching for Poly Si & Si in bulk of substrate
(15) APCVD SiO_2 + PECVD Si_3N_4 (For sealing and passivation)PLG-6 + RIE ($SiO_2 + Si_3N_4$)
(17) PLG-7 + RIE (for grid).

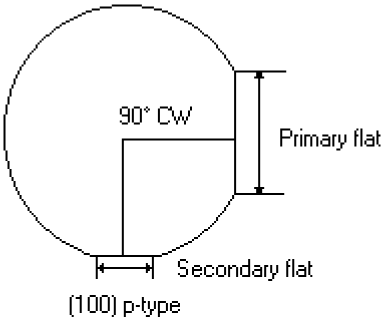

Figure 3: A p-type Si wafer with (100) orientation.

Results and Discussion

A processed chip can bee seen in figure (4), which can be compared with the layout details shown in figure (1). The two resistors have been placed on the thin diaphragm below which a micrometer conical cavity exists. Presently, the device is at packaging and characterization stage. A detailed test performance of the device shall be reported later on elsewhere**.**

Conclusion

The technology developed to fabricate the absolute micro pressure sensor has been described. This technology is suitable for the batch fabrication of the pressure sensors, to provide nearly 1089 chips of 1mm x 1mm size on a two-inch diameter silicon (100) wafer. The designing of the sensor depends on the simulated results of the stress profile on a strained diaphragm, which helps in the placements of the resistors. The most crucial part of the fabrication process is the mask –edge alignment with the cavity edges during KOH etching for the cavity formation.

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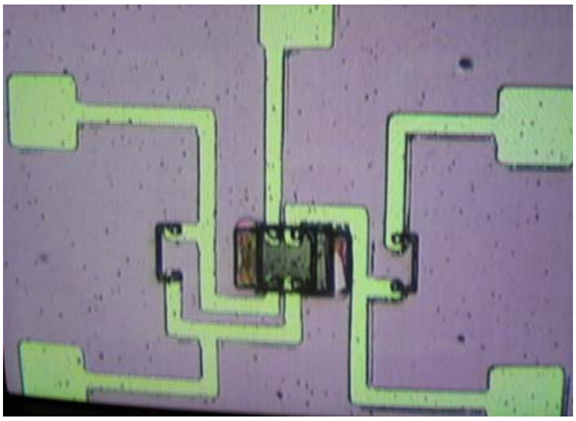

Figure 4: A photograph of processed chip on silicon wafer.

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