A Novel Approach to Enhance Performance in Near-Threshold Logic

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Abstract

Leakage currents raise exponentially with scaling of channel length in MOSFET. As a result overall power Consumption became a severe issue in chip designing. Various techniques have been introduced to reduce these leakage currents. But these currents can’t be reduced completely. A simple solution to this issue is to utilize these leakage currents for the circuit operation itself. This is possible with weak inversion circuit or sub-threshold circuit design where the power supply is applied less than or equal to the threshold of MOS transistor. Our approach employs dynamic threshold technique to the sub-threshold circuit technique to improve performance. Simulation results show that our method gives better results than conventional methods.

Keywords: Scaling, Leakage Currents, Dynamic Threshold, Sub-threshold design.

I.INTRODUCTION:

Various technologies have been developed mainly to achieve three important factors. They are power, area and speed. Among the three power is the first order design constraint in many applications especially in SOC designs. Because as the technology is progressing the functionalities that can be incorporated into a system are increasing. As a result power dissipation will be more in such circuits. If the power dissipation is more, then the circuit life time will be less. Cooling fans can be used but it is cost effective. So power reduction is important in many applications where delay is not a constrain. By reduction power consumption in a circuit, still more transistors can be incorporated to increase the functionalities.

Types of Power consumptions that take place in CMOS circuits are

1. Leakage or static power
2. Short circuit power
3. Dynamic power

Static power consumption takes place when circuit is in idle state. Short circuit power consumption takes place when both pmos and nmos transistors are ON and current flows from supply to the ground directly. And dynamic power consumption takes place due to the switching activity i.e., charging and discharging of output capacitance. The importance of cache memories has been aggressively increasing due to the processors speed based on the technology. So power reduction is very important factor in designing memories.

II. LEAKAGE CURRENTS:
Leakage current is the current that flows when the circuit is in steady state. Mainly there are three types of leakage currents. They are sub-threshold leakage current, gate leakage current and junction leakage current Sub-threshold leakage current flows when the gate voltage is less than the threshold of transistor. Gate leakage current flows at higher electric fields due to the reduced oxide thickness. And junction leakage current flows due to reverse bias voltages. Sub-threshold current is dominant among the three.

III. WEAK INVERSION CIRCUIT DESIGN:
Over the past years, circuits are operated in super-threshold region where the conduction currents are more. But there are some applications which need less current for their operation. Sub-threshold designs are used in those applications where the weak inversion current is used as their conduction current. Delay will be more in such type of circuits. But power consumption is very low.
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In sub-threshold designs, the supply potential is made equal or less than the threshold voltage of transistor. By this all the transistors in the circuit operate in weak inversion region.

As the technology is advancing, the threshold voltage of a transistor is also scaled to maintain performance. But as $V_t$ is scaled the sub-threshold currents increase exponentially creating a serious problem at nano regime. Sub-threshold designs provide solution to this problem by making use of these leakage currents as conduction current for their operation. The current flowing in sub-threshold circuits are widely smaller than linear or saturation currents.

Sub-threshold designs provide low power consumption with large delay penalty. The delay can be calculated by the following.

$$\tau = \frac{CV_{dd}}{(V_{dd} - V_t)^x}$$  \hspace{1cm} (1)

Where $c$ is the load capacitance, $V_t$ is the MOS threshold voltage. To overcome delay effect in sub-threshold region of operation, dynamic threshold logic can be employed to sub-threshold circuits to reduce the delay factor.

IV. DYNAMIC THRESHOLD LOGIC:

To reduce delay in sub-threshold designs, DTMOS technique is employed. Usually in nmos device the body is connected to source to avoid body effect as shown in Fig. 4(a) and in pmos device the body is connected to the power supply. But in dynamic threshold logic shown in Fig 4 (b), the body is for all time connected to the gate of transistor. By this, the threshold voltage of transistor can be varied accordingly. With this arrangement when the MOS transistor is ON, its threshold voltage is lowered increasing the conduction current and decreasing transmission delay. Similarly when the transistor is OFF, the threshold is raised, reducing weak inversion current and minimizing power dissipation.

![Fig 4.1(a)Traditional N-mosfet (b) DTMOS N-mosfet](image)

Our projected method combines both sub-threshold design and DTMOS techniques to achieve ultra low power design with finest performance.
TABLE I DELAY COMPARISION

<table>
<thead>
<tr>
<th></th>
<th>(v_{dd}=1.1\text{V} )</th>
<th>(v_{dd}=0.7\text{V} )</th>
<th>(v_{dd}=0.3\text{V} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>conv.</td>
<td>sub-threshold region</td>
<td>DTMOS</td>
</tr>
<tr>
<td>INV</td>
<td>19.91 E-9</td>
<td>20.42 E-9</td>
<td>19.96 E-9</td>
</tr>
<tr>
<td>NAND</td>
<td>19.99 E-9</td>
<td>20.79 E-9</td>
<td>19.91 E-9</td>
</tr>
<tr>
<td>NOR</td>
<td>16.97 E-9</td>
<td>20.17 E-9</td>
<td>19.98 E-9</td>
</tr>
<tr>
<td>AND</td>
<td>25.89 E-9</td>
<td>31.1 E-9</td>
<td>1938 E-9</td>
</tr>
<tr>
<td>OR</td>
<td>9.99 E-9</td>
<td>12.5 E-9</td>
<td>8.89 E-9</td>
</tr>
<tr>
<td>XOR</td>
<td>9.99 E-9</td>
<td>11.3 E-9</td>
<td>9.75 E-9</td>
</tr>
<tr>
<td>1kb SRAM Cell</td>
<td>10.11 E-9</td>
<td>13.1 E-9</td>
<td>10.12 E-9</td>
</tr>
<tr>
<td>Last gate current in 1kb cell</td>
<td>25.656 n watts</td>
<td>17.69 n watts</td>
<td>8.8367 m watts</td>
</tr>
</tbody>
</table>

Fig.4.2. Layout of 1kb DT-sub-threshold SRAM

CONCLUSION:
A 1kb cache memory is implemented in Cadence Tool using 45nm technology by combining both sub-threshold and dynamic threshold techniques. Simulation results show that the proposed method operates with extreme low power and optimum performance.

REFERENCES:
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