

Understanding the Effects of Scaling in case of a High Speed and Low resolution ADC through Simulation

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Abstract

Analog to digital converters are an important system building block, as an interface between analog and digital world. Parallel comparator type /flash ADCs is used in high speed, low resolution applications. Such architectures are both technology as well as supply voltage scalable. Power requirement is the single most prominent concern in modern electronic designs which generally vary with the dimensions and the supply voltages. Such variation also affects the speed performance of the circuit. This paper is an attempt to visualise and understand the effects of scaling of dimensions as well as of power supply voltage in case of a CMOS flash ADCs for different resolutions through simulation.

Key words: ADC (Analog to digital converters), Threshold inverter, Scaling (Technology & Voltage), Delay, Power consumption.

Introduction

A variety of ADCs with different architectures, resolutions, sampling rates, power consumptions, and operating temperature ranges [1-3] are available. Because of the parallel architecture of flash ADC, all conversions are done in one cycle with many comparators. Flash analog to digital converters, are thus fastest [3, 4] for analog signal to a digital signal conversion. However power consumption and large chip area required for the implementation of flash converters have practical limits at higher resolution although power saving design method for CMOS flash ADC such as in [5] is also available. A Flash ADC using a CMOS inverter based comparator as proposed in [4,6,7] under Threshold Inverter technique for high operating speed and low power dissipation using standard CMOS technology is used here on which SPICE simulation is carried out to analyze the effects of scaling of dimensions as well as of power supply.

Simulation Results and Discussions

The SPICE simulation results – the effects of technology scaling and voltage scaling on power consumption and also on speed performance of inverter threshold flash ADCs for different resolutions are discussed in this section.

Technology Scaling

The ADC under investigation are technology scalable and are implemented using the technologies 130nm, 100nm and 70nm, also [8]. Table 1 summarizes the effects of technology scaling on the 4-bit ADC.

Table 1: Comparator Transistor sizes used for different technologies for a 4-bit ADC.

Gate Length(nm)	70		100		130	
Comparator	SITV	LITV	SITV	LITV	SITV	LITV
W_p (μm)	0.1050	4.5415	0.1500	5.7960	0.1950	10.4839
W_n (μm)	4.0809	0.1050	5.6806	0.1500	9.2813	0.1950
V_m (V)	0.2350	0.5116	0.3200	0.8	0.4007	1.0481
V_{DD} (V)	0.8	0.8	1.2	1.2	1.5	1.5
V_{LSB} (V)	0.0184	0.0184	0.0302	0.0302	0.0432	0.0432
Avg. Power (μW)	0.92	1.2	1.08	1.52	1.38	2.47
Avg. Power consumed by 4bit ADC (μW)	68.7		96.6		160	

*SITV- the smallest inverter threshold voltage

*LITV- the largest inverter threshold voltage

Similarly 6-bit ADC and 8-bit ADC can have the same sizes of, SITV and LITV if they have the same gate length i.e. technology here in this context.

The average power consumed is plotted vs the technology used and the V_{DD} scaled along-with the technology scaling is also marked in Figure 1. The power consumption decreases with the scaling of technology along-with the supply voltage, V_{DD} . It is inferred from the figure that initial decrease in the power consumption with the downscaling of technology is quite sharp than in the lower technologies. This is attributed to the deep sub-micron region effects. At small dimensions the parasitics such as channel length modulation and sub-threshold current which are little significance at higher technologies dominate the power consumption.

In-spite of decreasing the supply voltage with the downscaling of the technology a sharp decrease is obtained initially when the technology is changed from 130nm technology to 100nm technology, but the rate of decrease in power consumption is not in the same proportion when the technology has been downscaled from 100nm to 70nm. This is because in the predictive technology models, which have been used for the simulations, the threshold voltages of the PMOS and NMOS transistors are not

downscaled with the same proportion as the technology is downscaled itself. So as the deep submicron circuit operation region is approached, the need is to model the parasitic capacitances and inductances and hence the transistor models accordingly [2, 9]. Sub-threshold currents and leakage currents start dominating the overall power dissipation in the deep sub-micron region. This reduces the control of V_{DD} on the overall power dissipation in the deep sub-micron region.

The V_{DD} is also scaled down along-with the technology, as, the power requirements of the circuit to perform the same operation is also reduced with the circuit dimensions. The V_{FSR} and so is the V_{LSB} depends upon the V_{DD} and hence are scaled down too, with the technology scaling to lower feature size. The [Figure 2](#) shows the plot of V_{LSB} vs. technology used for varying V_{DD} with the technology. It is inferred from the figure that with the decreasing feature size the V_{DD} and the V_{LSB} is also decreased in size. The variation is linear i.e. the quantities directly proportional to each other.

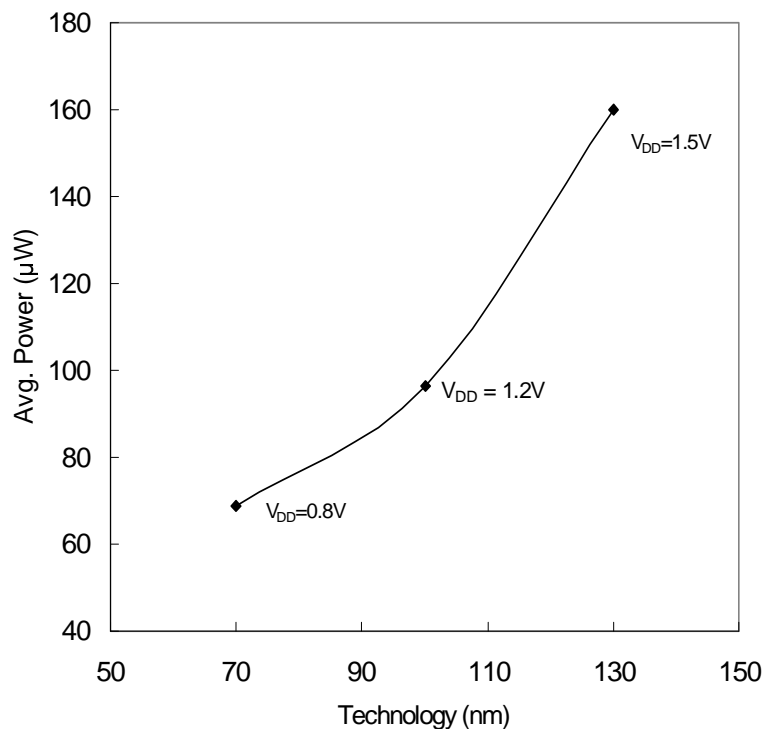


Figure 1: Technology used vs. Avg. Power.

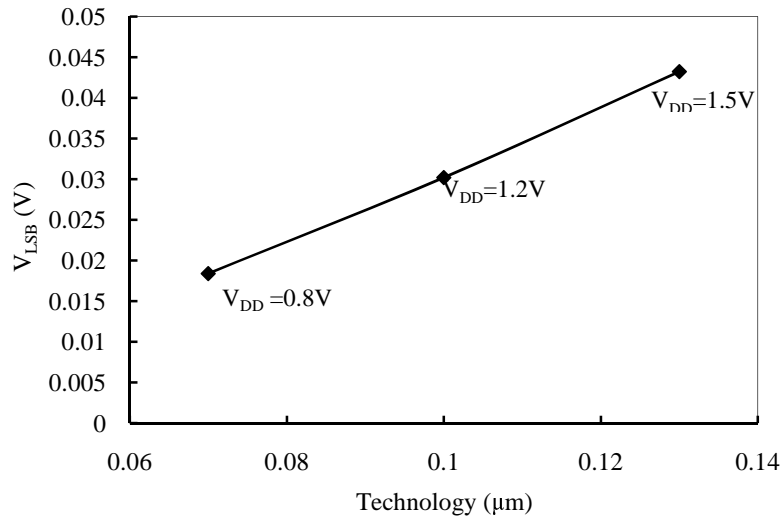


Figure 2: Variation of V_{LSB} vs. Technology used with different V_{DD} .

Power Supply Voltage Scaling

Total power dissipation in a CMOS digital circuits can be expressed as the sum of four components [10].

$$P_{total} = \alpha_T \cdot C_{load} \cdot V_{DD}^2 \cdot f_{CLK} + V_{DD} (I_{short-circuit} + I_{leakage} + I_{static}) \quad (1)$$

Where $I_{short-circuit}$ denotes the average short-circuit current, $I_{leakage}$ denotes the reverse-leakage and sub-threshold leakage currents, and I_{static} , denotes the DC current component drawn from the power supply. The switching power dissipation, the first term $P_{avg} = \alpha_T \cdot C_{load} \cdot V_{DD}^2 \cdot f_{CLK}$ in the equation (1) is the dominating component in most of the CMOS logic gate circuits, as it varies with the square of the V_{DD} , the supply voltage. One of the techniques to go for the low voltage design is through supply voltage scaling, shows, is that the total average power consumed by any CMOS logic-circuit varies in direct proportion to the supply voltage V_{DD} , because the dominant component of the total power dissipation is the dynamic power dissipation, which varies in direct proportion to the square of the supply voltage.

Although the reduction of power supply voltage significantly reduces the dynamic power dissipation, the inevitable design tradeoffs is the corresponding increase in delay.

The average power and delay as obtained by the V_{DD} scaling for 8-bit ADC designed using 130nm standard CMOS technology are tabulated in [Table 2](#). The power consumption decreases with the scaling of the supply voltage V_{DD} . The dynamic power dissipation is the dominating component in the total power dissipation in the CMOS circuits as it varies linearly with the square of the supply voltage.

Table 2: VDD scaling for 8-bit ADC in 130nm Technology.

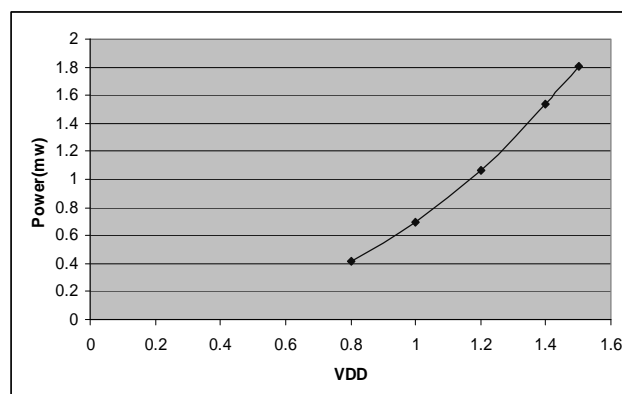
	V _{DD} (V)				
	0.8	1.0	1.2	1.4	1.5
Average Power (mW)	0.4137	0.696	1.067	1.540	1.805
Delay (ns)	4.03	2.53	1.777	1.460	1.368
Power-Delay-Product (μWs)	1.664	1.76	1.89	2.25	2.47

A. Voltage Scaling in an 8 bit Flash ADC

The power dissipation of the 8-bit Flash ADC, decreases sharply with decreasing V_{DD}, the total power dissipated in any CMOS circuit varies in accordance with the equation (1)[10]. The first component, dynamic power dissipation, varies with the square of the V_{DD}, hence dominates the overall power dissipation of the circuit under consideration. It is inferred from the data of the Table 2 that the scaling of the V_{DD} results in the lowering of power dissipation of the ADC and hence makes it suitable for the battery powered and less speed requirement devices. The V_{DD} can be scaled down to the minimum of the sum of V_{th,n}+V_{th,p} i.e. the threshold voltages of the NMOS and PMOS inverters in the particular technology used to implement the circuitry.

The Figure 3.a, 3.b, 3.c shows the plot of the power and delay corresponding to the different values of V_{DD} in contrast to each other. Delay continues to increase with decreasing V_{DD} and the average power also follows the decreasing path with the scaling of the V_{DD} to lower voltages. The power-delay product is important in finding out the optimum performance of the CMOS circuits. This is required to find out the extent of the compromise which can be made in power consumption and delay, without affecting the performance of the circuit significantly.

The price of the lowering of power dissipation by scaling the V_{DD} is paid in terms of the corresponding increase in the delay time, hence, the sampling rate of the ADC circuit is affected. The figure shows the increasing delay is shown with the decreasing V_{DD}.

**Figure 3.a:** Voltage-scaling Effects on power in 8-bit flash ADC.

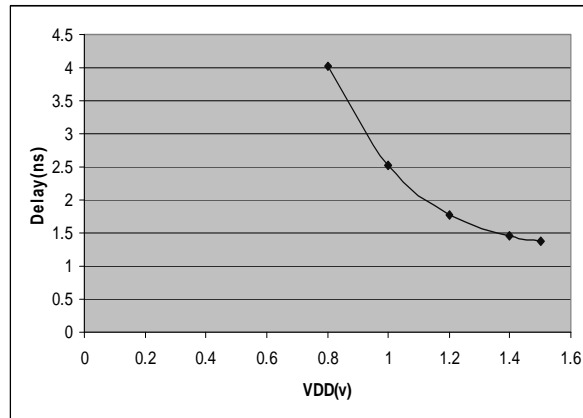


Figure 3.b: Voltage-scaling Effects on delay in 8-bit flash ADC.

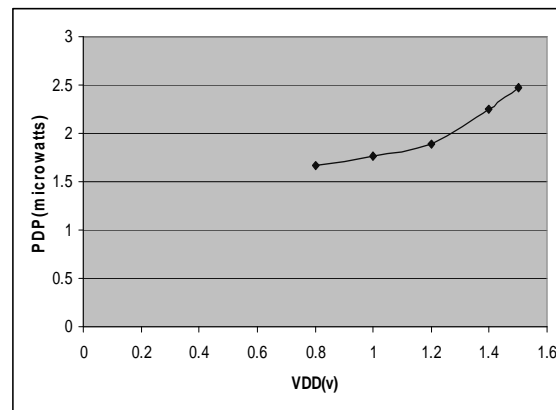


Figure 3.c: Voltage-scaling Effects on Power Delay Product in 8-bit flash ADC.

B. Voltage-Scaling in a 3-bit Flash ADC

A brief analysis of the average power dissipation in a 3-bit Flash ADC designed in 100nm technology has also been performed using SPICE. The average power dissipation results for varying supply voltage V_{DD} scaled down from 1.2V to 0.6V are also tabulated in the [table 3](#). The data obtained shows the decrease in the Average power with the scaling of the power supply voltage.

Table 3: VDD scaling for 3-bit ADC in 100nm technology.

V_{DD} (V)	Average Power (μ W)
1.2	96.69
1	58.10
0.9	42.64
0.8	29.73
0.7	19.35
0.6	16.0

Graphical representation of the variation of the Average Power dissipation with respect to the supply voltage scaling is plotted in the Figure 4. It is inferred from the graphical view that at higher V_{DD} , the average power dissipation reduction is more linear as compared to that at lower values of V_{DD} . This can be explained for the expression of the total average power dissipation from equation (1) that at higher values of V_{DD} the dynamic power dissipation which is the function of square of the power supply voltage, as given in equation (2).

$$P_{dynamic} = \alpha_T \cdot C_{load} \cdot V_{DD}^2 \cdot f_{CLK} \quad (2)$$

But, the V_{DD} is further scaled down to the lower values such that it is slightly greater than $V_{th,n} + |V_{th,p}|$, at such a low level of the supply voltage the dominating share of the dynamic power is further shared by the short circuit power and the static power dissipation due to increasing sub-threshold currents, and leakage currents in the static operation mode. The short-circuit power is given by,

$$P_{short-circuit} = \frac{1}{12} \cdot k \cdot \tau \cdot f_{CLK} (V_{DD} - 2V_T)^3 \quad (3)$$

Where τ =rise time=fall time; $k_n=k_p=k$; $V_{T,n} = V_{T,p} = V_T$ are so taken to simplify the expression and to calculate it for a symmetric inverter.

The third component is briefed as in equation (4), it has been inferred that the second and third components of the total power dissipation of a CMOS circuit are proportional to first power of V_{DD} only, but on other parameters also which have a significant effect on the overall circuit dissipation when at a low value of the V_{DD} .

$$P_{static} = V_{DD} (I_{leakage} + I_{static}) \quad (4)$$

As given in equation (3), $P_{short-circuit}$ is directly proportional to the $(V_{DD}-2V_T)^3$, so when the V_{DD} approaches V_T then the V_T dominates the short circuit power dissipation i.e. short circuit power decreases because of the low supply voltage.

Conclusion

In general power consumption decrease with the downscaling of technology but at smaller dimensions the decline in power consumption is less because of the effect of sub micron region where parasitics (capacitances and inductances) become dominant which reduces the control of the VDD on overall power dissipation.

There is reduction in power dissipation with down scaling of supply voltage but it is achieved at the cost of speed performance. Hence it could be used in battery operated and less speed required devices.

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Abbreviations

- Full-scale range of analog input voltage (V_{FSR})
- V_{LSB} is the quantization step
- $V_{LSB} = \frac{V_{FSR}}{2^n - 1}$
- inverter threshold voltage (V_m)
- $V_{Th,p}$ and $V_{Th,n}$ represent the threshold voltage of PMOS and NMOS devices, respectively
- W_n & W_p - transistor widths
- V_{DD} - Power supply voltage