

Novel Work on Low Power Multiplexer for High Speed Switching Devices Using Sleep Transistor Techniques

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Abstract

In nanometer advances, static power utilization is a noteworthy concern. In addition to innovation in downsizing and higher working rates of CMOS VLSI circuits, the leakage power is being upgraded. As the geometries of the procedure decrease, increases in thickness of the device as well as the voltage of the threshold just as the thickness of the oxide decreases to keep pace with execution. Different strategies for controlling sub threshold leakage reduction. Furthermore, another method for small and quick leakage is also suggested here. Because of the elevated transistor density, low threshold and ultrathin dielectric, the leakage control dissemination increases rapidly as the innovation scales down to deep submicron level. The new suggested circuit approach includes sleepy Multiplexer and associate Transistors to reduce leakage current with an appropriate W/L ratio. The suggested scheme provides fast execution as it incorporates NMOS Transistor into the framework with greater electron mobility. Intemperate by and substantial execution highlight is inserted into small-scale devices in nanotechnology development. In this paper where conventional Multiplexer consume 170 μ w in 180nm technology as such at 45nm technology it's consume 27 μ w in active mode. In sleepy multiplexer both active as well as static mode the power dissipation reduces 12 times, at 180nm technology sleepy Multiplexer consume power 80 μ w in active mode and in static mode its consumes 24 μ w power, as well as at 45nm technology Sleepy Multiplexer consume 6.6 μ w power in active mode and in static mode its consume 2.5 μ w.

Keywords: static mode, Sleepy Multiplexer, nanometer, Intemperate.

Introduction

Power is viewed as one the main significant factor in planning the present VLSI circuits. Complete Power losses establish both Dynamic as well as Static loss. Presently a day's static power loss also has turned into key vexation. Sub-threshold conductance, gate oxide tunneling current, leak all along reverse biased

diodes, as well as contention current in proportional circuits are main cause for static loss.

$$P_{Total} = P_{Static} + P_{Dynamic} \quad (1)$$

Such loss happens essentially by ultra-thin channel length as well as carrier power overcoming barrier voltage. High doping scales of about $1 \times 10^{18} \text{ cm}^{-3}$ tend to decrease in barrier potential as well as extent towards carrier concentration. Indeed helps more charge movement even at low voltage ranges. Regular discharging–charging of load capacitances and short circuit current earn major portion of dynamic power loss [1].

$$P_{dynamic} = V_{DD}^2 f_{clk} \sum_n \alpha_n c_n + V_{DD} \sum_n I_{scn} \quad (2)$$

With the cutting edge innovation, however diminished supply voltages should prompt low misfortunes, anyway the need of quick exchanging action, high clock recurrence (f_{clk}), high short out flows (i_{sc}) and very mind boggling circuits prompts more advances and hence progressively unique influence losses. The leak current in MOSFETs relies upon different procedure metrics, transistor as well as the quiescent state of the circuit. Such sub-threshold leak current for $V_{GS} < V_T$ is given as:

$$I_{Ds} = I_{Dso} e^{(V_{GS}-V_T)/\eta V_T} [1 - (e^{-V_{DS}/V_T})] \quad (3)$$

Where,

$$V_T = V_{To} - \eta V_{DS} + \gamma [\phi_s + V_{SB}]^{1/2} - (\phi)^{1/2}$$

In these conditions I_{DSO} presents on threshold (subject to process and gadget geometry), V_{TO} -zero predisposition threshold voltage, γ - linearised body impact coefficient, η speaks with the impact of V_{DS} on threshold voltage, n is the sub-threshold swing coefficient, V_T -Thermal voltage range separately. η denotes depicts D I B L impact. Sub-threshold conductance is increases from (DIBL) Drain Induced Barrier lowering in which positive V_{DS} viably diminish V_T . Leak current duplicates for each 8^0 to 10^0 K ascend in temperature [1]. The sub-threshold leakage current can be decreased by expanding threshold voltage V_{TO} , expanding V_{SB} and decrease of V_{GS} , V_{DS} and bringing down the temperature range. In profound submicron CMOS circuits, the decrease in leakage current must be accomplished utilizing both procedures as well as circuit-stages strategies. On the procedure stages, leaking reduction can reaches by controls the dimensions (length, oxide thickness, junction depth and so on.) and doping profile in transistors. At the circuit stages, threshold voltage and leaking current of transistors can able to controlled by controlling the voltage ranges of different device terminals [drain, source, gate, and body (substrate)] [2].

This work introduces novel static power step-down strategies in Sleepy Multiplexers. Nonstop contracting of highlight sizes has empowered scaling of voltage and subsequently gigantic decrease in unique power. This step-down in source voltage must be corresponding with a proportional reduction in threshold voltage in sequence to remain adverse effects on delays. This threshold decrease anyway is joined by an

exponential increment in leakage current and consequently leakage control. Leakage control/current can essentially be ascribed to the put away charge in gadgets that are off which continue directing (releasing) current. As innovation scales, the significance of leakage control/current is ending up increasingly noteworthy. Truth be told it is turning into the predominant segment of generally chip control [3-6]. New advancement approaches are wanted which streamline the leakage straightforwardly immediately.

In this manner basically via diminish static power all along the idle or backup method about activity containing the circuits. Multiplexer is an all-inclusive rationale component that is most ordinarily utilized in correspondence frameworks including TDM and optical correspondence frameworks. Subsequently, it should be upgraded as far as both power and speed so as to acquire superior advanced frameworks. The expanding interest for low control VLSI circuits be tended to at various plan scales, for example, the compositional, circuit, design and the procedure innovation Scale [7-8]. On basis of circuit and design Scale, the power scattering be able to limited through adequately decreasing the sub-edge conductance evenly switch one-sided spillage flows. Short out flows, albeit thought to be insignificant, have been found to comprise 10–30 % of in general power utilization [9-10].

Literature Review

Low Power devices are always trends in market because of user requirement. To make ultra-Low power device, some techniques used by researcher till now are discusses here.

S.No	Techniques	Pros and Cons of Techniques
1.	Power Gating [6]	Combinational Circuits leakage much more than other circuit because of it consists several Input/Outputs. So, if we add sleep transistor combinational circuit, it becomes efficient.
2	Super Cutoff CMOS Techniques [8]	It is depends on drive as well as overdriven condition of sleep transistors. So, it is complex to analyze
3	Sleepy Stack Approach [1]	In this approach we can use the sleep transistor, which can implement parallel way. The area is major concern in this technique.
4	Leakage Feedback Approach [7]	In this approach two parallel transistor are used. So, the main concern about area as well as logic input/outputs
5	leakage Feedback Analog Stack	Area and delay is major drawback. So, this type of approach is not much efficient for implementation.
6	Sleep Keeper approach [5]	This approach not depends output working and in this the pull down transistor utilizes much more than pull up transistor.
7	Input Vector Control [6]	This technique based on only input vector calculation and complexity is highly pronounced.
8	Zigzag Approach [7]	Delay is major concern and the structure is complex

So, we prefer Power Grating Techniques because of in this area as well as delay is not much more concern. Sleep Transistor also efficiently implemented in combinational circuit and gives much less power dissipation.

PROPOSED DESIGN

Reduction in channel length of MOS and CMOS devices directly affect the power performance of VLSI device. As the channel length reduce into nm scale, the device size also scaled and numbers of chip per unit area has increased. Advancement in CMOS and MOS devices in term of nanometer technology had got tremendous change in power analysis. As per the nanotechnology tends towards the Pico-meter technology the power consumption in VLSI devices has enhanced. Reduction in channel length reduces the threshold voltage and oxide thickness of MOS. As the threshold voltage tends towards the sub-threshold voltage of MOS the leakage current enhanced proportionally. The leakage power of MOS indirectly proportional to leakage current as the technology scaled 180nm to 45nm MOS power leakage enhanced tremendously and per unit area power dissipation increased in standby mode. Motive of this thesis is to analyze and optimize the power consumption of MOS based sleepy inverter and sleepy multiplexer at 45nm channel length and to analyze the power delay product of sleepy inverter and sleepy multiplexer at various Nano-scale including 180nm and 45nm. Power dissipation analyzed in both modes including active and standby mode. In this paper visualization are shown according to development of sleep transistor and low power multiplexer using Novel sleepy Transistor using SPICE Tool. The proposed structure of the circuits are performed or observed from 180nm and 45nm CMOS technology. The results are observed for purpose of validation of logic operations and static, dynamic and total power dissipation. Further the analysis is extended to find the leakage power for design. The voltage range for this design is generally varies from 1.25V to 5V or 1.8V on average chosen for circuit simulation.

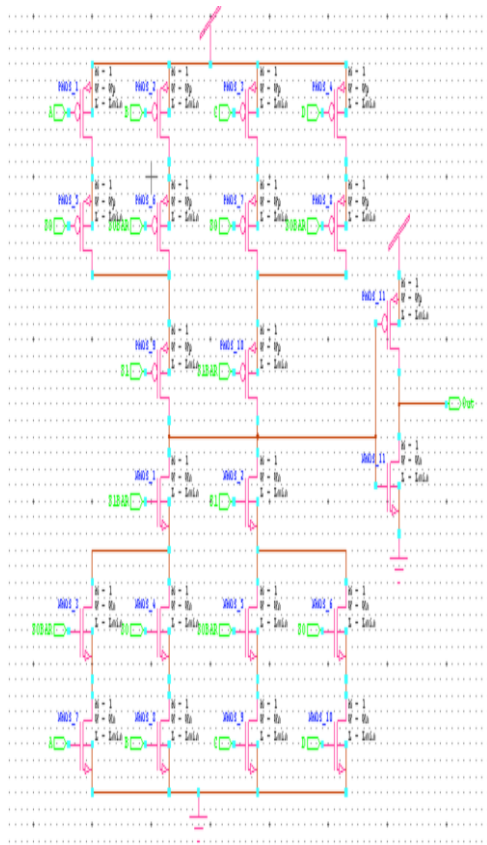


Fig.1. Conventional MOS based Multiplexer Schematic

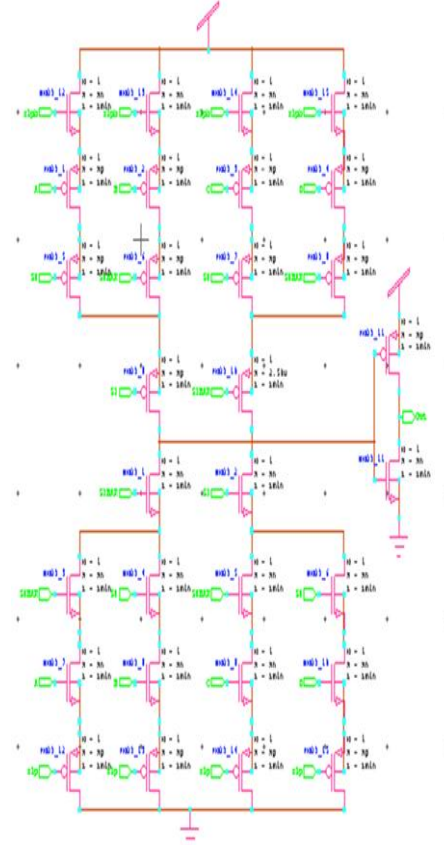


Fig.2. sleepy multiplexer schematic

Multiplexer is an universal and combinational circuit, which have versatile application in a digital system design. High power dissipation degrades the system performance reliability. To maintain the power integrity of digital system, leakage power in standby mode of basic CMOS inverter must be in range of 100 Pico Watt. Power integrity issues of a system are a step stone in digital system design. Worst power management introduced the various system performance problems including bad signal integrity.

RESULTS:

We used the Tanner simulation tool to analyze the logic circuit.

1. Conventional Multiplexer Response and Analysis

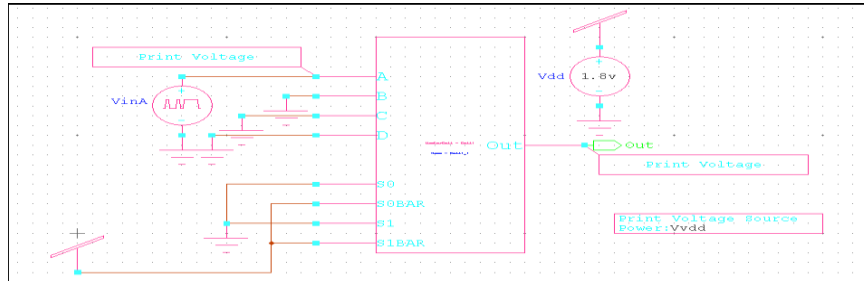


Fig.3.Multiplexer Schematic Symbol

2. Conventional Multiplexer Transient Response at 180 nm

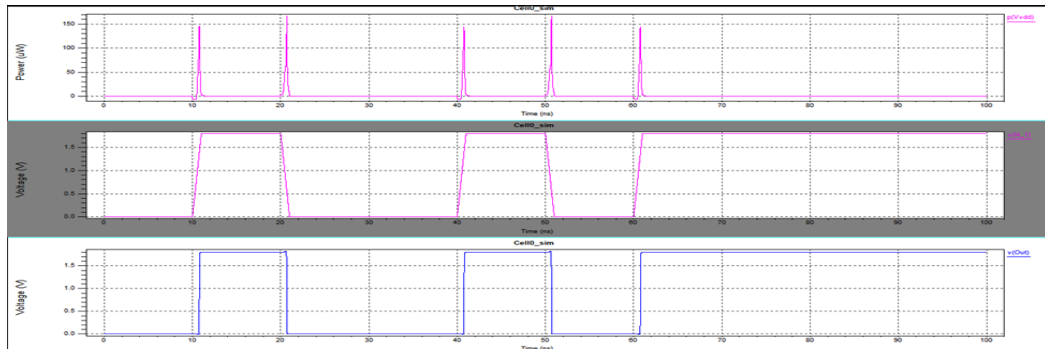


Fig.4. Conventional Multiplexer Response at 180nm

Table1: Parametric and response value of Conventional Multiplexer at 180nm

V=1.8 Volt		
Power Dissipation (Active mode)	170	microwatt
Power Dissipation (Static mode)	0.014	microwatt
Rise time	330	Picosecond
Fall time	163	Picosecond
Propagation Delay	246.5	Picosecond
Channel length	180	Nanometer
Width of NMOS	500	Nanometer
Width of CMOS	1	Nanometer

3. Conventional Multiplexer Transient Response at 45 nm

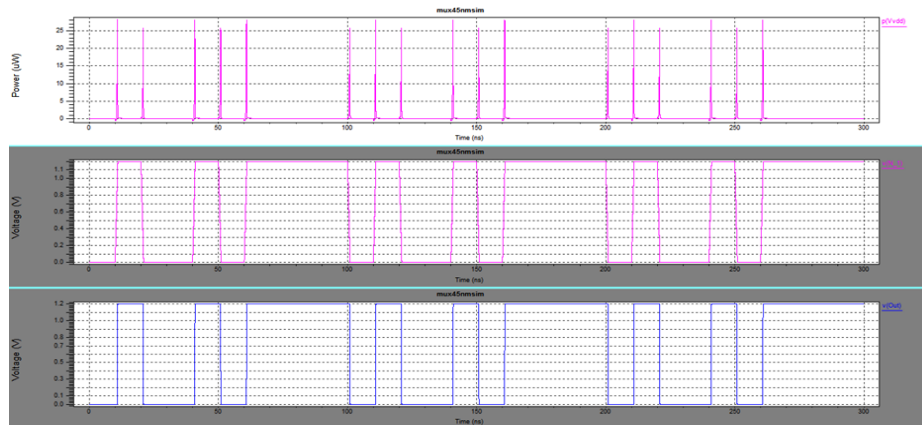


Fig.5. Multiplexer Response output at 45 nm

Table 2: Parametric and response value of Conventional Multiplexer at 45nm

V=1.8 Volt		
Power Dissipation (Active mode)	27	microwatt
Power Dissipation (Static mode)	0.005	microwatt
Rise time	212.36	Picosecond
Fall time	155.59	Picosecond
Propagation Delay	183.98	Picosecond
Channel length	45	Nanometer
Width of NMOS	100	Nanometer
Width of CMOS	200	Nanometer

4. Sleepy Multiplexer Response and Analysis

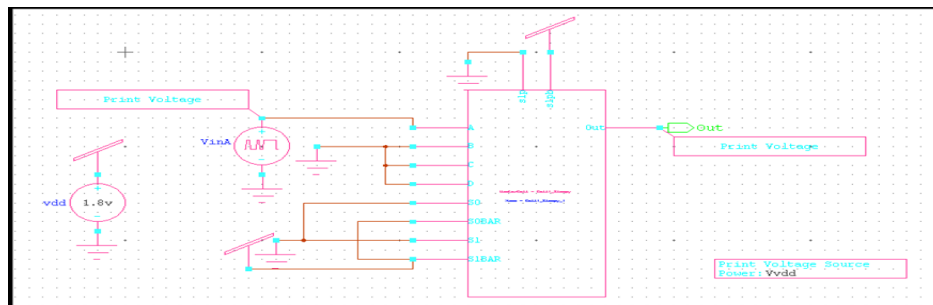


Fig.6. Sleepy Multiplexer Schematic

So we conclude that if we implemented the sleepy transistor into Multiplexer which is vital role in communication for easy working and fast response of system. Sleepy Transistor in Multiplexer gives us important combinational circuit which can add up in system and reduce power of any system. Important concern is that we can reduce static power 12 to 15 times if we shift the technology 180nm to 45nm.

5. Sleepy Multiplexer Response in Active mode at 180 nm

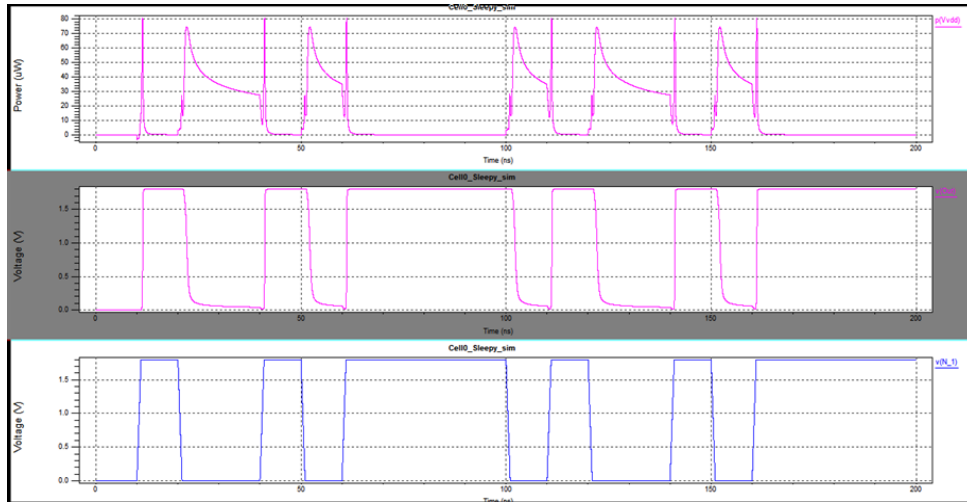


Fig.7.Sleepy Multiplexer Response in active mode at 180 nm

6. Sleepy Multiplexer Response in Active mode at 45 nm

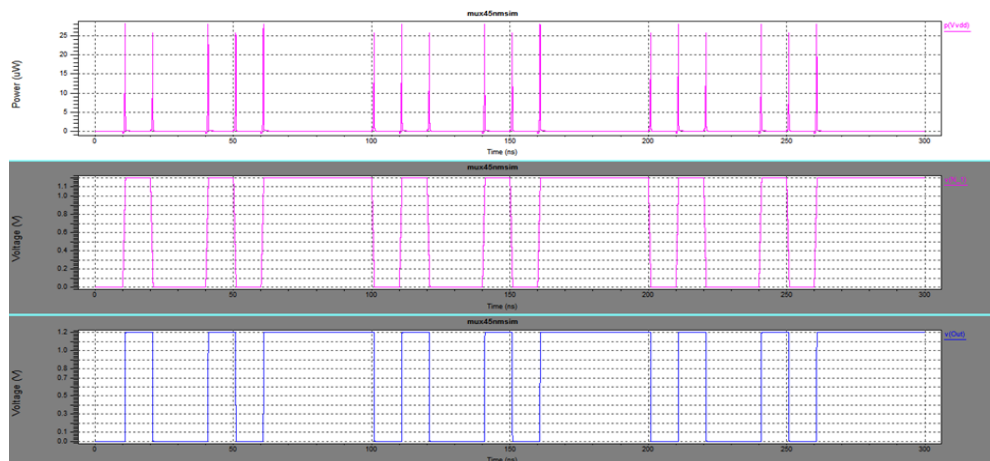


Fig.8. Sleepy Multiplexer Response in active mode at 180 nm

7.Sleepy Multiplexer in standby mode at 180 nm

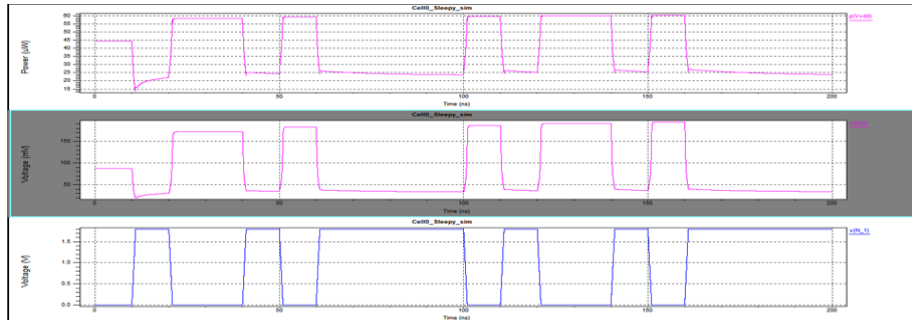


Fig.9.Sleepy Multiplexer Response in standby mode at 180 nm

8.Sleepy Multiplexer in standby mode at 45 nm

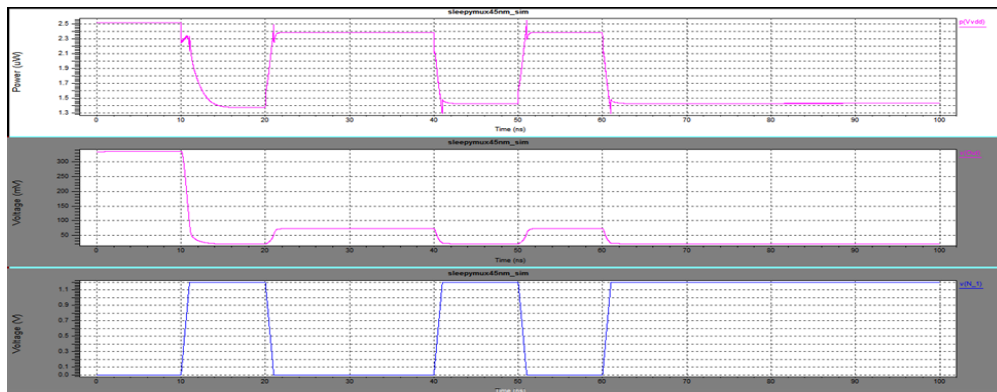


Fig.10. Sleepy Multiplexer Response in standby mode at 45 nm

Table 3:Parametric and response value of Sleepy Multiplexer at 180nm

V=1.8 Volt		
Power Dissipation (Active mode) When slp=0 and slpb=1	80	microwatt
Power Dissipation (Static mode)when slp=1 and slpb=0	24	microwatt
Rise time	622.27	Picosecond
Fall time	4.27	Picosecond
Propagation Delay	2.7	Picosecond
Channel length	180	Nanometer
Width of NMOS	500	Nanometer
Width of CMOS	1	Nanometer

Table 4: Parametric and response value of Sleepy Multiplexer at 45nm

V=1.2 Volt		
Power Dissipation (Active mode) When slp=0 and slpb=1	6.6	microwatt
Power Dissipation (Static mode) when slp=1 and slpb=0	2.5	microwatt
Rise time	1.28	Picosecond
Fall time	1.94	Picosecond
Propagation Delay	1.61	Picosecond
Channel length	45	Nanometer
Width of NMOS	100	Nanometer
Width of CMOS	200	Nanometer

9. Comparison Graph Of Conventional Multiplexer And Sleepy Multiplexer At Different Technologies

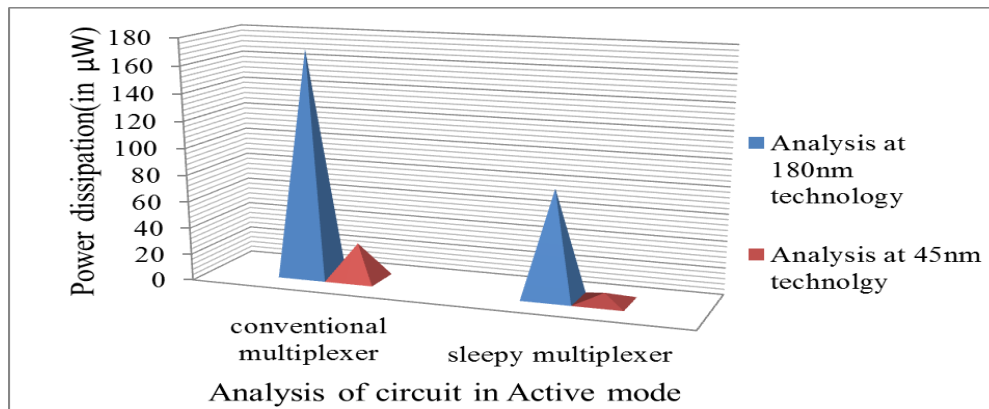


Fig.11. Analysis of Power dissipation in Active mode

In comparison graph we observe that there is reduction in power dissipation in active mode where technology lowering is work when we goes 180nm to 45nm technology in conventional multiplexer as well as sleepy multiplexer which is vital progress in saving power which is shown as above presentation. In Sleepy Multiplexer which is novel work on Multiplexer by addition of sleep transistor. We reduce 12 times power dissipation in active mode of sleepy Multiplexer and in static mode we also reduce 12 times power dissipation. Sleepy Multiplexer working like Normal Multiplexer but the advantage point of view Multiplexer is combinational circuit which includes in any system as example: use in

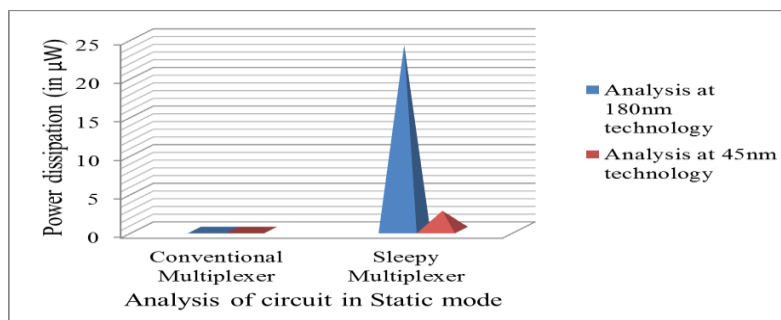


Fig.12. Analysis of Power dissipation in Static Mode

Communication system. Sleepy Multiplexer gives more advantages over conventional Multiplexer in sense of power dissipation this analysis done in comparison graph. Where conventional Multiplexer consume $170\mu\text{w}$ in 180nm technology as such at 45nm technology its consume $27\mu\text{w}$ in active mode. In sleepy multiplexer both active as well as static mode the power dissipation reduces 12 times, at 180nm technology sleepy Multiplexer consume power $80\mu\text{w}$ in active mode and in static mode Sleepy Multiplexer consumes $24\mu\text{w}$ power, as well as at 45nm technology Sleepy Multiplexer consume $6.6\mu\text{w}$ power in active mode and in static mode Sleepy Multiplexer consume $2.5\mu\text{w}$.

Conclusion

All simulation findings and assumptions demonstrate the power consumption and delay efficiency of 4 Multiplexer input circuits. Based on the Sleepy Multiplexer setup, we evaluated the parameters linked to power consumption and delay at the steady transistor length and distinct transistor concentrations of transistor channel width. It can be stated that the performance parameters of the 4x1 Mux conventional multiplexer setup are optimistic compared to 4x1 Sleepy Multiplexers based on settings. Sleepy Multiplexer setup is suggested in this article to ensure better efficiency. The summary data analysis indicates that there is an improvement in the performance parameter at different levels of the channel width of the transistor while using the SPICE Tool, the 45 nm technology for Tanner 14.1 design.

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