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A Multilevel Diode Clamped SVPWM Based Interline Dynamic Voltage Restorer with Sag & Swell Limiting Function

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Abstract

An interline dynamic voltage restorer (IDVR) is a new device for sag mitigation which is made of several dynamic voltage restorers (DVRs) with a common dc link, where each SVPWM based DVR is connected in series with a distribution feeder. During the sag period, active power can be transferred from a feeder to another one and voltage sags & swell with long durations can be mitigated. IDVR compensation capacity, however, depends greatly on the load power factor, and a higher load power factor causes lower performance of IDVR. To overcome this limitation, a new idea is presented in this paper which enables reducing the load power factor under sag & swell conditions and, therefore, the compensation capacity is increased. The proposed IDVR employs diode clamped multilevel converters with SVPWM to inject ac voltage with lower total harmonic distortion and eliminates the necessity to low-frequency isolation transformers in one side.

Keywords: Sag, swell, Mitigation, fuzzy logic, DVR,IDVR and SVPWM

I. INTRODUCTION

The American "sag" and the British "dip" are both names for a decrease in voltage to between 10 and 90% of nominal voltage for one-half cycle to one minute Sags account for the vast majority of power problems experienced by end users. They can be generated both internally and externally from an end users facility.

External causes of sags primarily come from the utility transmission and distribution network. Sags coming from the utility have a variety of cause including lightning, animal and human activity, and normal and abnormal utility equipment operation. Sags generated on the transmission or distribution system can travel hundreds of miles thereby affecting thousands of customers during a single event. Sometimes externally caused sags can be generated by other customers nearby.

The starting of large electrical loads or switching off shunt capacitor banks can generate a sag large enough to affect a local area. If the end user is already subject to chronic under voltage, then even a relatively small amplitude sag can have detrimental effects. Sags caused internally to an end user's facility are typically generated by the starting of large electrical loads such as motors or magnets. The large inrush of current required to starts these types of loads depresses the voltage level available to other equipment that share the same electrical system. As with externally caused sags, ones generated internally will be magnified by chronic under voltage.

A swell is the opposite of sag - an increase in voltage above 110% of nominal for one-half cycle to one minute. Although swells occur infrequently when compared to sags, they can cause equipment malfunction and premature wear. Swells can be caused by shutting off loads or switching capacitor banks on.

II SPACE VECTOR PULSE WIDTH MODULATION

A different approach to SPWM is based on the space vector representation of voltages in the d, q plane. The d, q components are found by Park transform, where the total power, as well as the impedance, remains unchanged.

Fig: space vector shows 8 space vectors in according to 8 switching positions of inverter, V* is the phase-to-center voltage which is obtained by proper selection of adjacent vectors V1 and V2.

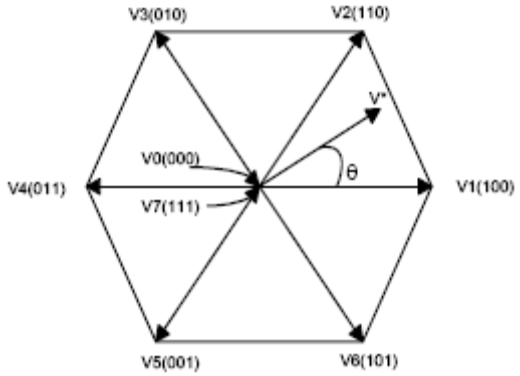


Fig 1: Inverter output voltage space vector

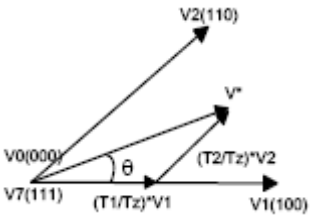


Fig 2 : Determination of Switching times

The reference space vector V* is given by Equation (1), where T1, T2 are the intervals of application of vector V1 and V2 respectively, and zero vectors V0 and V7 are selected for T0.

$$V^* T_z = V1 *T1 + V2 *T2 + V0 *(T0/2) + V7 *(T0/2)…….(4)$$

Fig. below shows that the inverter switching state for the period T1 for vector V1 and for vector V2, resulting switching patterns of each phase of inverter are shown in Fig. pulse pattern of space vector PWM.

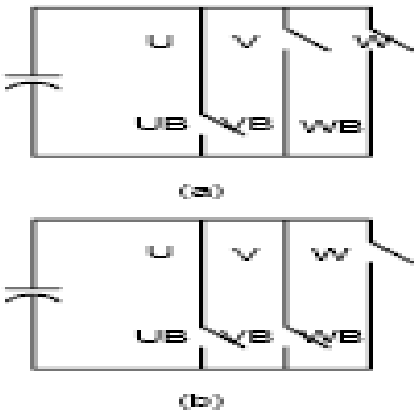


Fig 3 : Inverter switching state for (a)V1, (b) V2

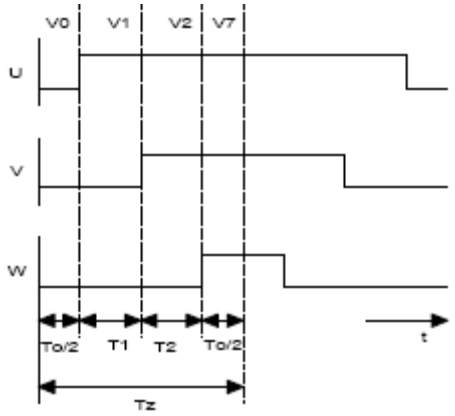
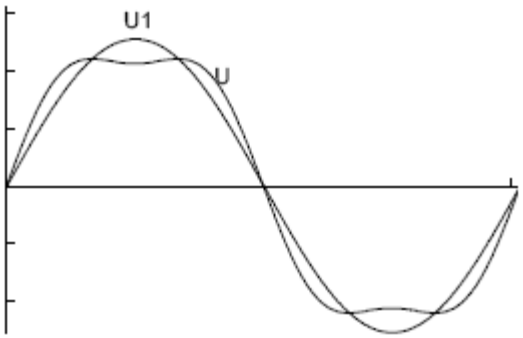


Fig 4: Pulse pattern of Space vector PWM



COMPARISON

In above Fig:- comparison, U is the phase to- center voltage containing the triple order harmonics that are generated by space vector PWM, and U1 is the sinusoidal reference voltage. But the triple order harmonics are not appeared in the phase-to-phase voltage as well. This leads to the higher modulation index compared to the SPWM.

COMPARISON OF SPWM AND SPACE VECTOR PWM

As mentioned above, SPWM only reaches to 78 percent of square wave operation, but the amplitude of maximum possible voltage is 90 percent of square-wave in the case of space vector PWM. The maximum phase-to-center voltage by sinusoidal and space vector

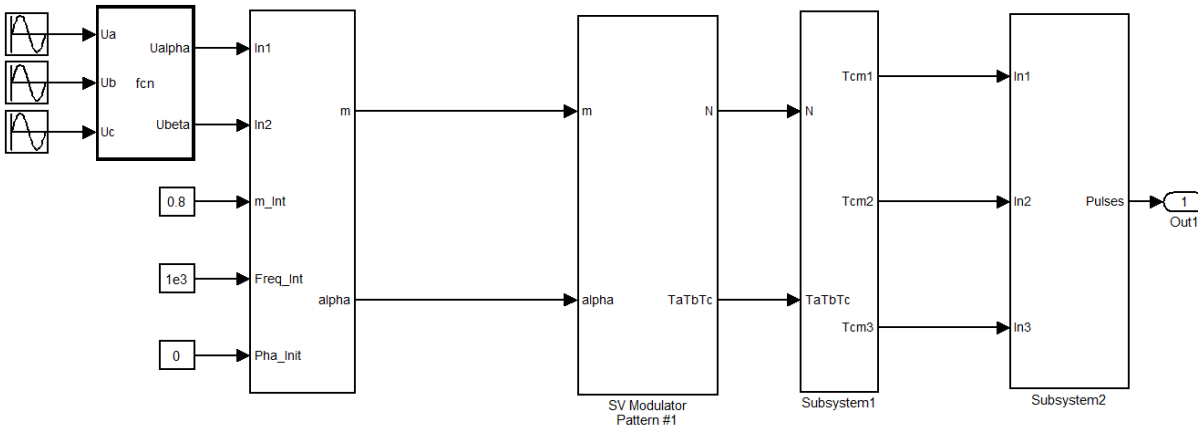


Fig 5 : Space vector PWM matlab module

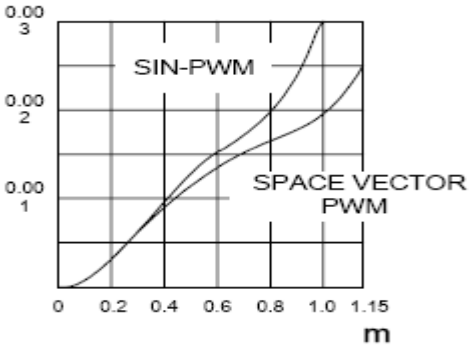
PWM are respectively

Vmax = Vdc/2 : Sinusoidal PWM

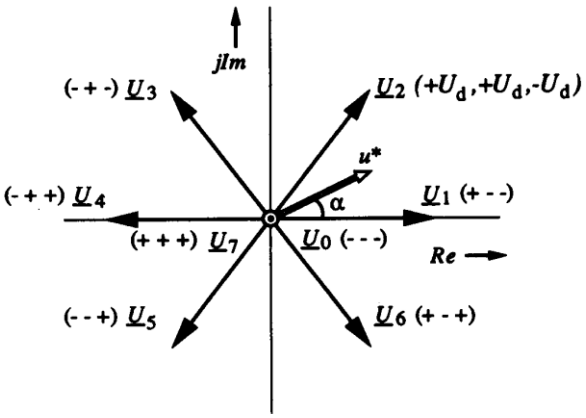
Vmax = Vdc/√3 : Space Vector PWM

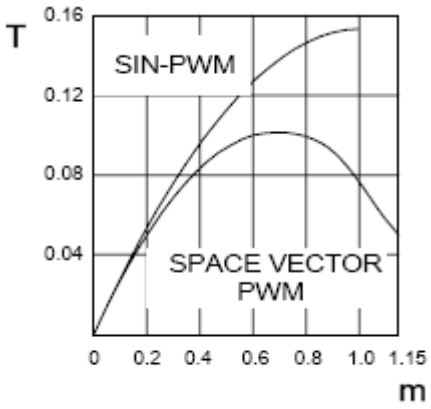
Where, Vdc is DC-Link voltage.

This means that Space Vector PWM can produce about 15 percent higher than Sinusoidal PWM in output voltage.



(a)rms harmonic current





(b) torque harmonics

SVM PWM TECHNIQUE:

The Pulse Width modulation technique permits to obtain three phase system voltages, which can be applied to the controlled output. Space Vector Modulation (SVM) principle differs from other PWM processes in the fact that all three drive signals for the inverter will be created simultaneously. The implementation of SVM process in digital systems necessitates less operation time and also less program memory.

The SVM algorithm is based on the principle of the space vector u*, which describes all three output voltages ua, ub and uc :

u* = 2/3 . (ua + a . ub + a2 . uc) ……(5)

Where a = -1/2 + j . v3/2 We can distinguish six sectors limited by eight discrete vectors u0…u7 (fig:- inverter output voltage space vector), which correspond to the 23 = 8 possible switching states of the power switches of the inverter.

III SPACE VECTOR MODULATION

The amplitude of u0 and u7 equals 0. The other vectors u1…u6 have the same amplitude and are 60 degrees shifted.

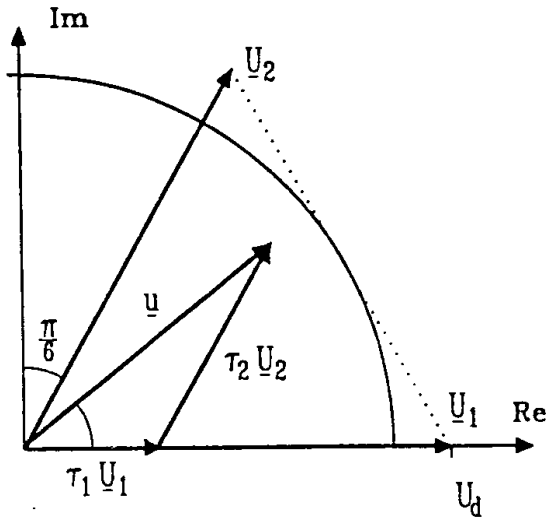
By varying the relative on-switching time Tc of the different vectors, the space vector u* and also the output voltages ua, ub and uc can be varied and is defined as:

ua = Re (u*)

ub = Re (u* . a-1)

uc = Re (u* . a-2) ……(6)

During a switching period Tc and considering for example the first sector, the vectors u0, u1 and u2 will be switched on alternatively.



Definition of the Space vector

Depending on the switching times t0, t1 and t2 the space vector u* is defined as:

u* = 1/Tc . (t0 . u0 + t1 . u1 + t2 . u2)

u* = t0 . u0 + t1 . u1 + t2 . u2

u* = t1 . u1 + t2 . u2 …….. (7)

Where

t0 + t1 + t2 = Tc and

t0 + t1 + t2 = 1

t0, t1 and t2 are the relative values of the on switching times.

They are defined as: t1 = m. cos (a + p/6)

t2 = m. sin a

t0 = 1 - t1 - t2

Their values are implemented in a table for a modulation factor m = 1. Then it will be easy to calculate the space vector u* and the output voltages ua, ub and uc. The voltage vector u* can be provided directly by the optimal vector control laws w1, v_{sa} and v_{sb}. In order to generate the phase voltages ua, ub and uc corresponding to the desired voltage vector u* the following SVM strategy is proposed.

Device connected	**Power factor**	**T.H.D**	**Compensated voltage**	**Compensated current**
Without compensator	0.62	25.5	0v	0v
With 2 level DVR	0.69	10.2	264v	2.3A
With 3 level DVR	0.72	6.5	464v	2.3A
With 5 level DVR	0.74	4.6	764v	2.3A
With 2 level STATCOM	0.69	17.8	264v	6.5A
With 3 level STATCOM	0.72	10.9	264v	7.2A
With 5 level STATCOM	0.76	6.1	264v	10.3A
With level MC-UPQC	0.83	2.2	864v	15. 3A

IV SIMULATION MODEL & RESULTS

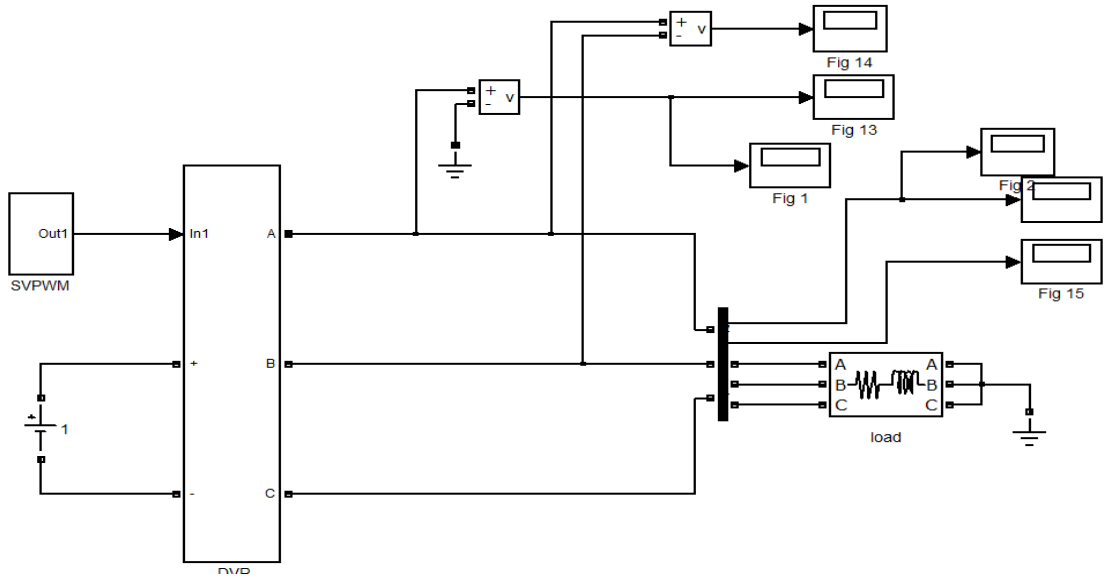


Fig 6: Multi level SVPWM based Compensator

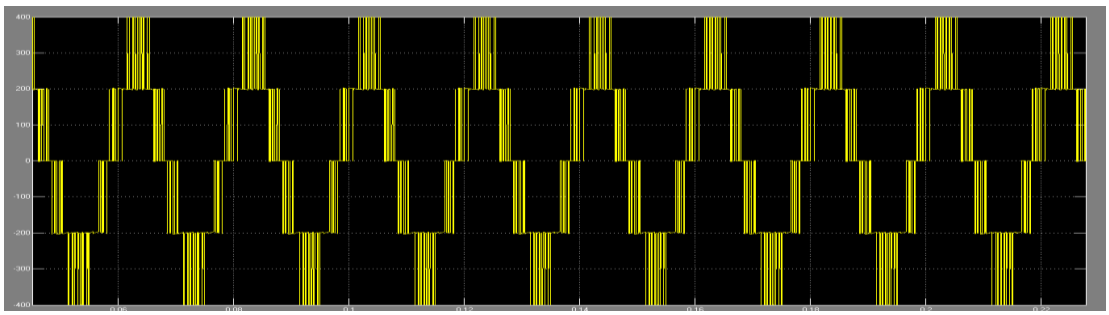


Fig 7: Multi level voltages

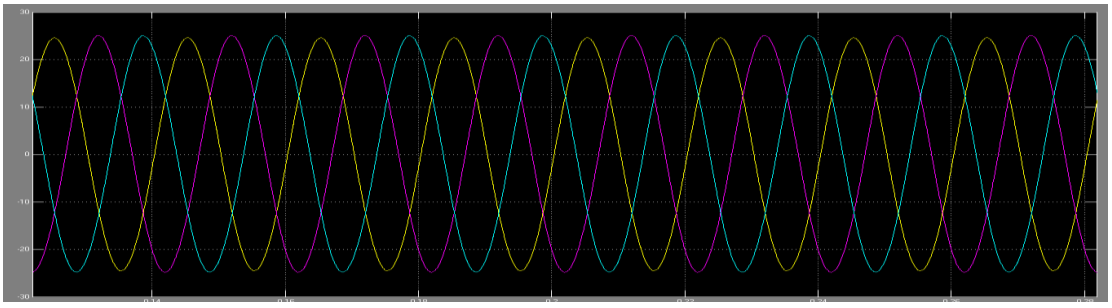


Fig 8: Current at the load

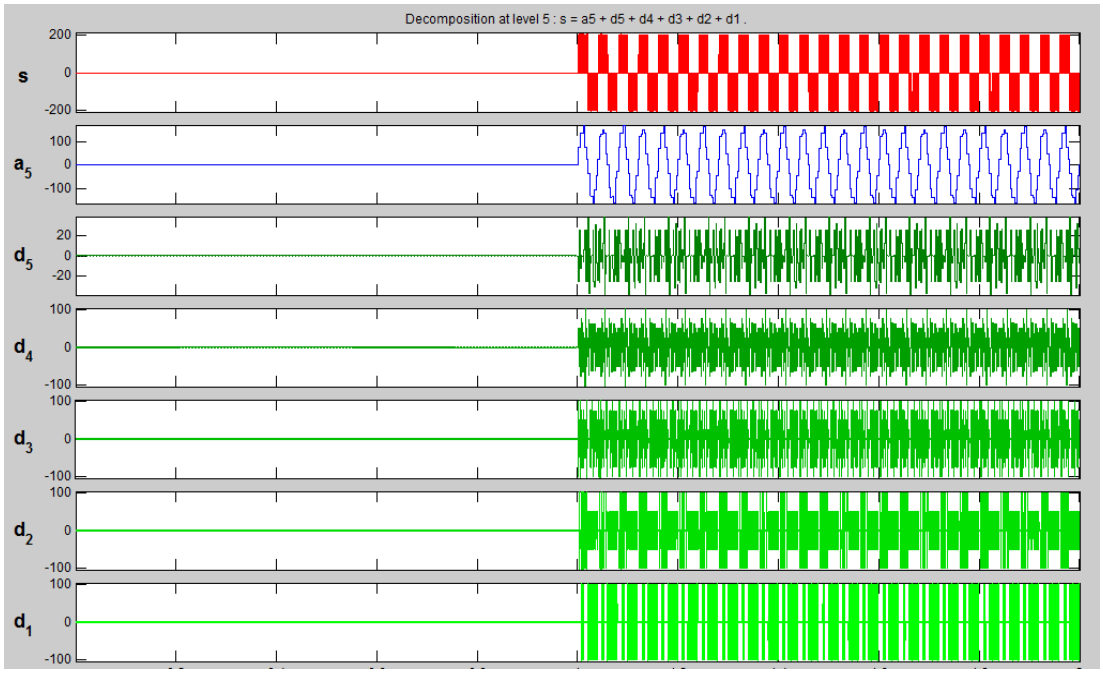


Fig 9: Analysis by wavelets

V CONCLUSION

In this paper, a new configuration has been proposed which not only improves the compensation capacity of the IDVR at high power factors, but also increases the performance of the compensator to mitigate deep sags at fairly moderate power factors. These advantages were achieved by decreasing the load power factor during the sag condition. In this technique, the source voltages are sensed continuously and when the voltage sag is detected, the shunt reactance's are switched into the circuit and decrease the load power factors to improve IDVR performance. Finally, the simulation and practical results on the CHB-based IDVR confirmed the effectiveness of the proposed configuration and control scheme.

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