

## **A 3.5 GHz Low Noise, High Gain Narrow Band Differential Low Noise Amplifier Design for Wi-MAX Applications**

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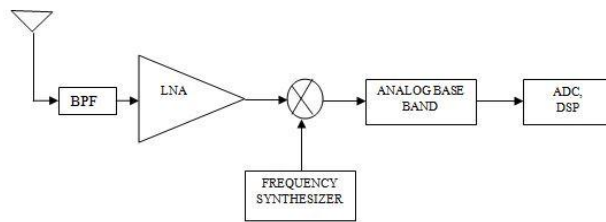
### **Abstract**

This paper represents a 3.5 GHz narrow band differential LNA novel design for the improvement and reliability in 180 $\mu$ m CMOS technology. A 3.5 GHz proposed LNA designed structure is a fully integrated 3GHz high gain narrow band LNA by using differential cascode technique with modified inductive degenerated topology. The low power high gain, less noise, CMOS LNA is designed for wimax applications with UMC 180 $\mu$ m RF CMOS technology. This differential LNA has a noise figure of 2.65dB, supply voltage of 1.8V. The LNA has input return loss of -20 dB, output return loss of -14.6 dB, and Forward gain (S<sub>21</sub>) of 32dB. And 18.37dBm of 1dB compression point for the received signals that are below compression point. For the testing of inter modulation IIP<sub>3</sub> is observed 4.16dBm. The designed LNA was simulated using 180 $\mu$ m RF spectre tool.

**Keywords:** RF CMOS, VLSI Design, Wireless Communications, Low noise amplifier, cascode, input return loss, WiMAX.

## 1. INTRODUCTION:

Over the past decade, many CMOS LNA'S, 802,11 / 6,802.11 / A and GSM standard has been reported at him from the standards specified by the WiMAX IEEE 802.16e wireless wideband technology. Developed for the existing Internet network facilities are inadequate, so that the greatest number of developers are trying to improve this problem The best solution for low cost, for high integration processing and analogy circuits to be mixed with digital one is CMOS technology.



**Fig. 1** RF Front end circuit diagram

From fig (1), the low noise amplifier is one of the most crucial blocks in a receiver section of communication systems. The performance of the LNA mainly determined with respect to noise figure and gain. LNA is first stage of receiver such that it provides better input impedance matching.

From the metropolitan area network access systems to cope NLOS (line of sight) and LOS (line of sight: sight) transmission conditions, WiMAX can provide coverage of 75mbps data Rate, Range 50 km. It can extent even 3G Modem, cable, wired by hand wide approach.

Basic LNA requirements:

1. Gain (10-20 db) to amplify the received signal and to reduce the input referred noise of the subsequent stages.
2. Good linearity: Handling large undesired signals without much distortion.
3. Low noise for high sensitivity
4. Maximum power gain  $50 \Omega$  termination for proper operation and can route the LNA to the antenna which is located an unknown distance away without worrying about the length of the transmission line.

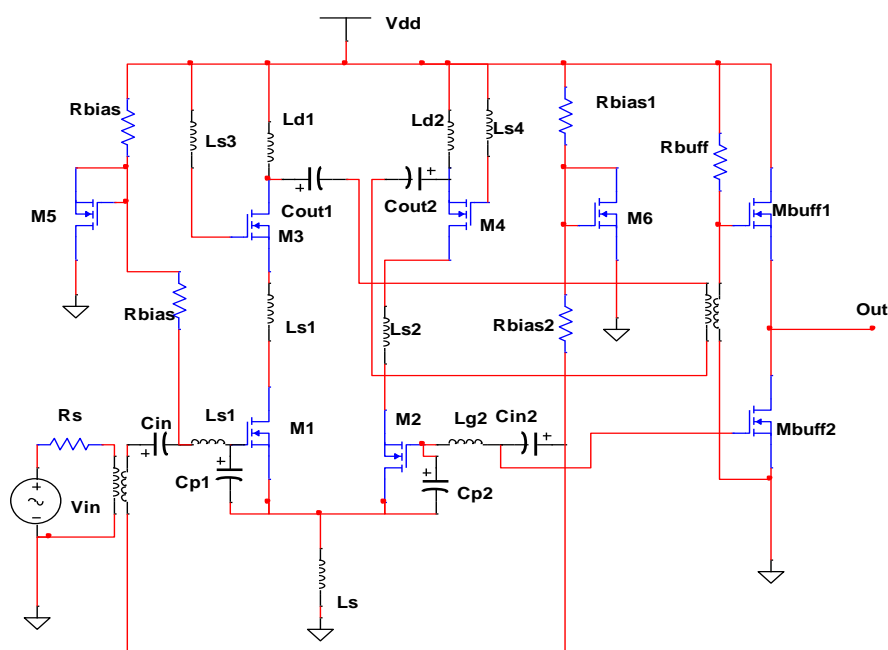
### 1.2 Basic Topologies

1. Wide band LNA input matching topologies (a) Resistive termination (b) common gate (c) resistive shunt feedback.
2. Narrow band LNA input matching topologies (a) inductive degenerated (b) resistive terminated.

This differential LNA design is most versatile technique among the different LNA topologies which is shown in Fig.2. This is improved version of inductively

degenerated Common Source LNA parameters of reverse isolation ,input and output matching network low power ,high gain ,less noise etc. The inductively degenerated cascade LNA

1. Enhance the noise performance in the 3.5GHz narrow band applications.
2. To improve the isolation between input and output .
3. To improve the performance of input and output matching of the circuit.
4. Output load matching can be obtained by variation of the load inductor  $L_d$  and capacitor  $C_{out}$ .



**Fig.2.** Architecture of designed Differential Low noise amplifier (LNA)

**Principle of operation of Differential LNA** This 3.5 GHz differential LNA is designed based on CS degenerative input matching cascade with the 180  $\mu\text{m}$  CMOS technology. The designed differential LNA is shown in Fig. 2. The designed characteristic of this circuit is described below:

1. The CMOS Cascode topology with CS degeneration..
2. An active current mirror circuit provided both input and output terminals biasing
3. This design enhances the two input double ended architecture.
4. An extra buffer circuit provided the output matching .

The Miller effect reduces and  $S_{12}$  parameters are improved by using this cascade architecture. The input matching ,less noise provide by the CS degeneration .To

reduces the further noise at biasing stages M4 and M5 transistors having current mirrors.  $R_{bais1}$  and must be chosen large enough to reduce the further noise from the biasing stages. The active bias circuit consists of transistor M5 and M6, impedance  $R_{bais1}$  and  $R_{bais2}$ , provides transistor M1 and M2 with gate current. By providing proper width for the transistor and also optimize M1 and M2 transistor without degrading the input and output by added buffer circuit it can provide. For proper gain the resonant inductors LS1, LS2, LS3, and LS4 added in this circuit. In order to cut the extra power added by biasing circuits, the width of transistors M5 and M6 has to be chosen a fraction of the M1 and M2 width, and bias impedance  $R_{bais2}$  should be large enough.  $C_{in1}$ ,  $C_{in2}$ ,  $C_{out1}$ ,  $C_{out2}$  are blocking capacitors. The value of series resonance inductors  $Ls1$ ,  $Ls2$ ,  $Ls3$ ,  $Ls4$  added in this circuit are to be chosen based on the iterative simulations until it reaches the proper gain without degrading the input and output match. The added buffer outside the circuit is helpful in attaining the best output match and load tuning.

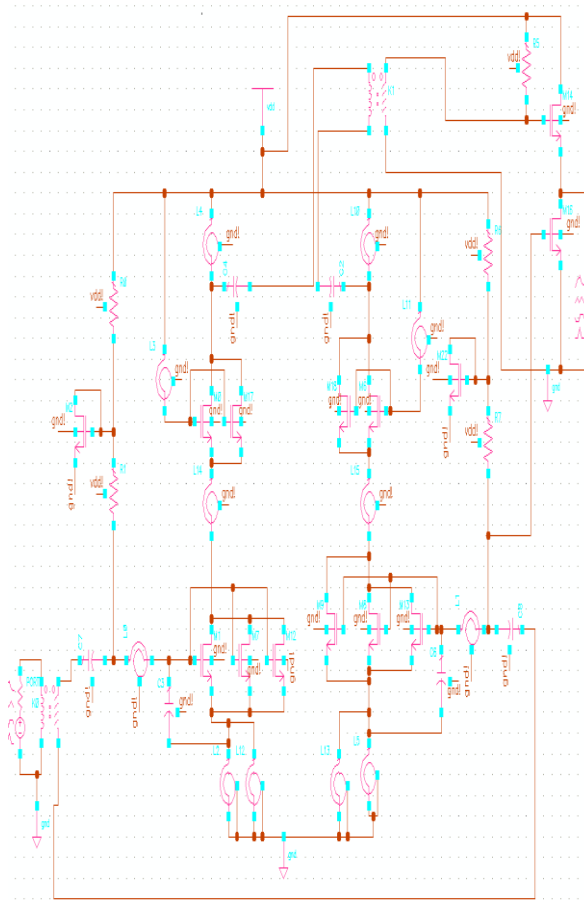
Next section shows the pre and post layout simulation results of the designed circuits. Fig 2. Shows the architecture of the Designed Differential LNA design.

**Table 1.** Performance comparison table

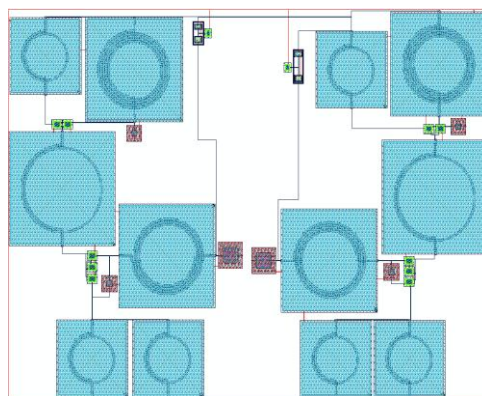
parameter	Schematic differential LNA	Post layout differential LNA
S11( dB)	-20.05	-9.42
S12( dB)	-51.72	-59.49
S21( dB)	32.72	29.66
S22 ( dB)	-14.65	-12.23
NF( dB)	2.668	4.423
NF min( dB)	2.221	3.396
1dBcompression (dB m)	-18.361	-19.346
IIP3(dB m)	-8.416	-10.298

## SIMULATION RESULTS

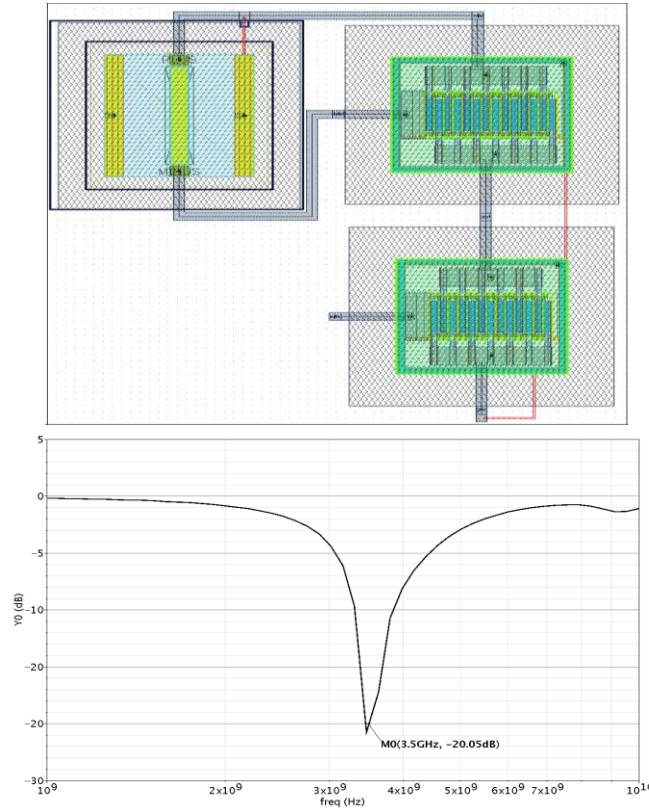
The designed LNA at 3.5GHz, shown in Fig. 2, Cadence RF spectre 180  $\mu$ m CMOS t Culatool was used to simulate is shown in fig 2. The Fig 3 and 4 respectively shows schematic and layout of designed LNA, Simulation results of designed LNA are shown in Fig.6 -18. From the above simulation results, we can observe a small difference between pre and post layout graphically, because of parasitic formed during the layout process.



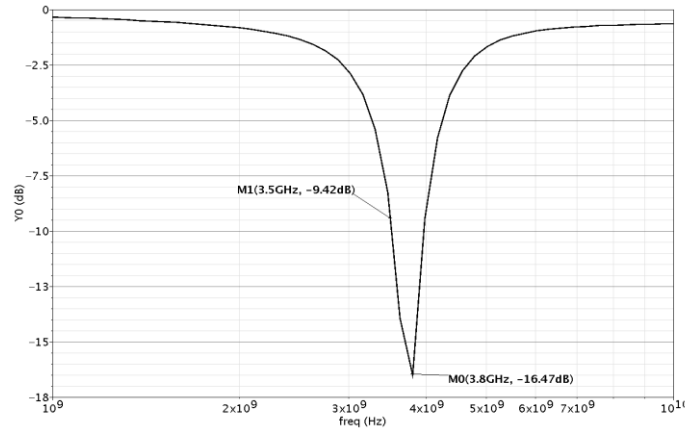
**Fig 3:** Schematic of 3.5GHz Differential cascode LNA.



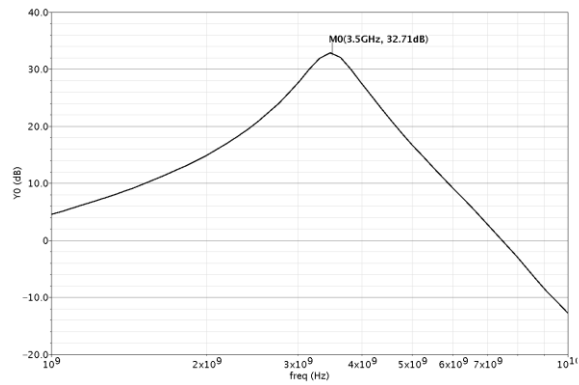
**Fig.4:** Differential LNA Layout of the (a) Double ended diff. LNA (b) Buffer



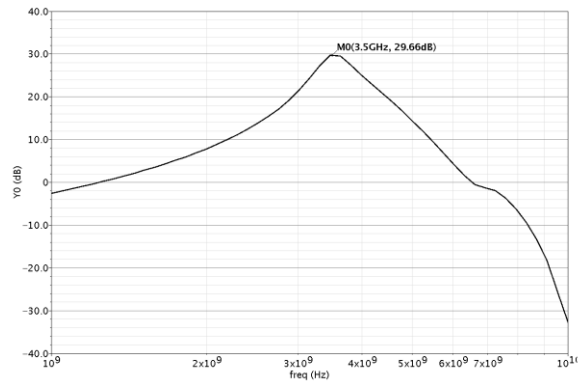
**Fig.5:** Input return loss  $S_{11}$ (schematic)



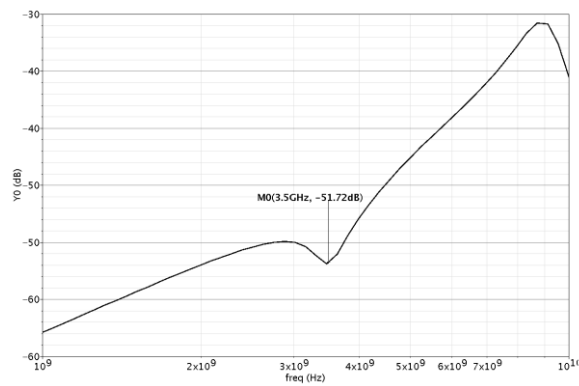
**Fig 6:** Post layout of input return loss  $S_{11}$



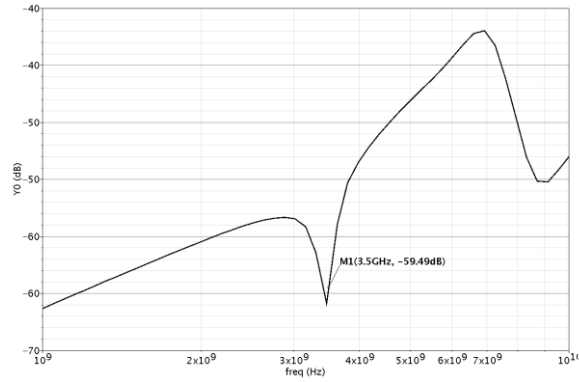
**Fig. 7:** Forward gain S21 (Schematic)



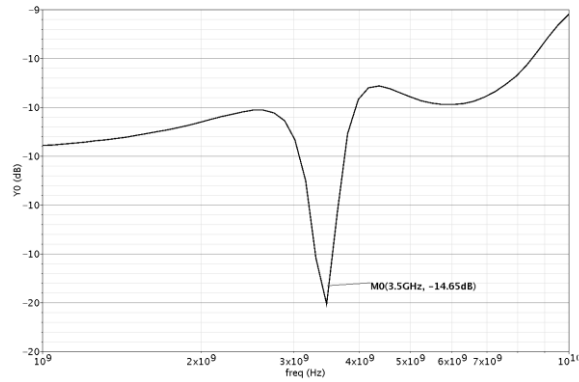
**Fig 8:** Forward gain S21 (Post layout)



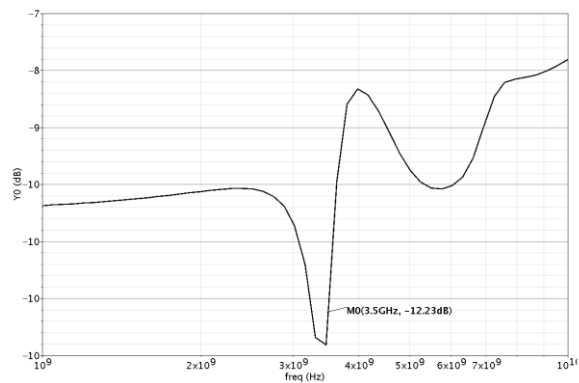
**Fig. 9:** Reverse Isolation S12 (Schematic)



**Fig. 10.:** Reverse Isolation S12 (Post layout)

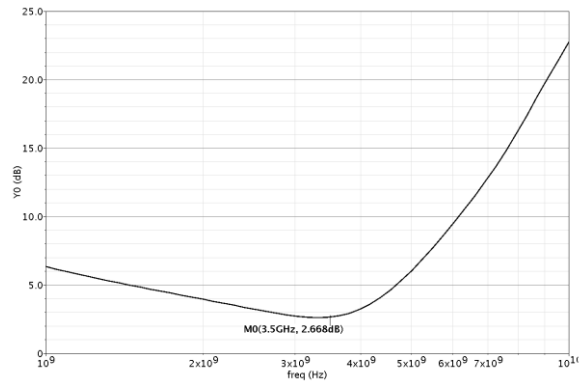


**Fig.11:** Output return loss S22 (Schematic)

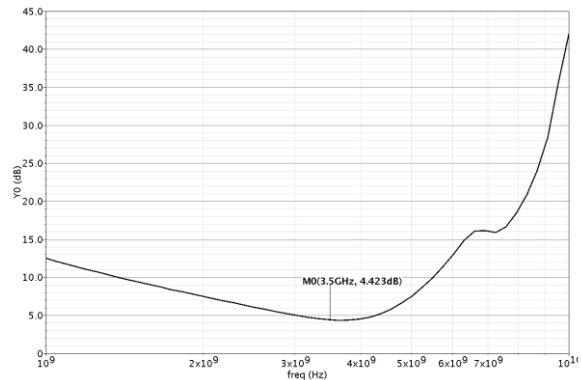


**Fig. 12:** Output return loss S22 (Post layout)

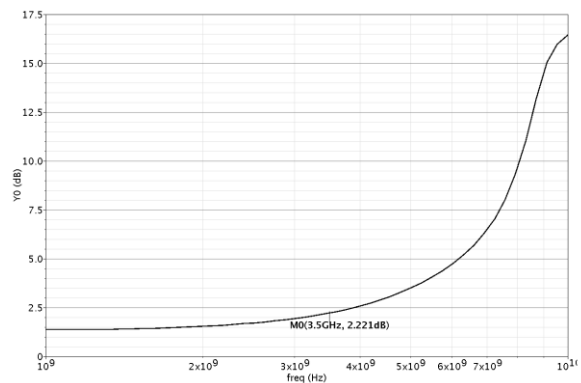




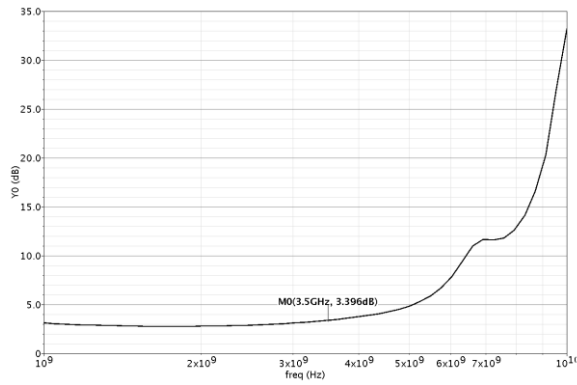
**Fig 13:** Simulation of Noise Figure (Schematic)



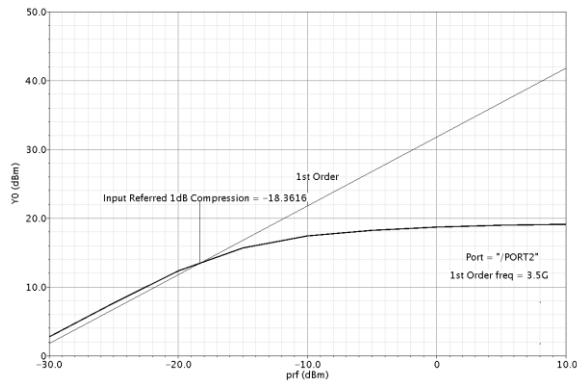
**Fig. 14:** Noise Figure (Post layout)



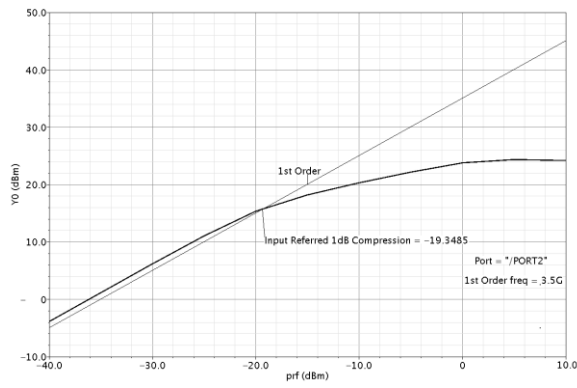
**Fig. 15:** Simulation of minimum NF (Schematic)



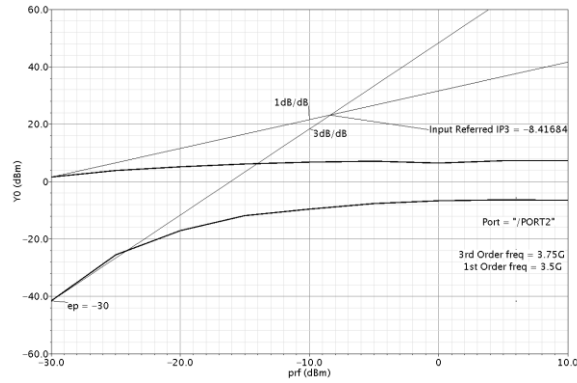
**Fig.16.** Minimum NF (Post layout)



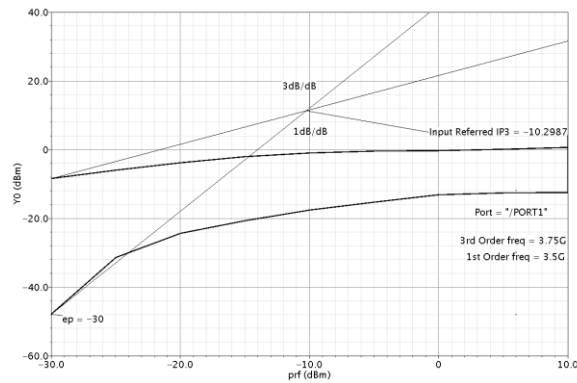
**Fig. 17:** 1 – dB compression point (Schematic)



**Fig.18:** 1 – dB compression point (Post layout)



**Fig.19:** Schematic Simulation of IIP3



**Fig. 20:** Post layout Simulation of IIP3.

**CONCLUSION**

This differential LNA design simulated by UMC 180µm by using supply voltage of 1.8v.cmos technology A 3.5 GHz differential LNA design using UMC 0.18µm CMOS process. This differential LNA requires a supply voltage of 1.8V. This LNA attains noise figure (NF) of 2.66dB, with input return loss of -20dB, output return loss of -14.65dB, and Forward gain of 32 dB, with Compression point 1dB This differential LNA performance represents high gain, with low noise figure. 1dB compression point of this design is -18.361dBm, means no gain compression for the received signals below compression point level. A two tone test is done to this LNA to observe the intermodulation, observed IIP3 is -8.6Bm. This LNA can be used in wireless applications for high gain. The performance summary is listed in Table 1 .

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