Survey on Stability of Low Power SRAM Bit Cells

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Abstract

Static random access memory (SRAM) blocks occupy major chip area and are the primary contributors to leakage power in many modern systems. Scaling the supply voltage of SRAM macros is an efficient method to reduce total chip power. It is difficult to achieve an SRAM cell with stable operation at low-voltage due to increasing variations in process, voltage and temperature. In the sub-threshold region, conventional 6-T SRAMs fail to deliver density and yield requirements due to reduced static noise margin (SNM), poor writability, limited number of cells per bit line, and reduced bit line sensing margin. This paper reviews state-of-the-art bit cell structures with good stability under sub-threshold condition in terms of technology parameters.

Keywords: SRAM, Static noise margin, Write margin (WM), Read margin (RM), Reliability

1. INTRODUCTION

SRAM occupies most of the system on chip (SoC) area and dominates the system performance and power. Especially in bioelectronics and other emerging applications, low supply voltage and low-power SRAMs are required to extend system operation with limited energy resource. Therefore, design of low-voltage and low-power sub-threshold SRAM circuit [1] has gained ever-increasing importance. Two aspects are important for SRAM cell design: the cell area and the stability of the cell. These two are interdependent since designing a cell for improved stability invariably requires a
larger cell area. As device size continuously scales down, the increasing leakage current, systematic process variations, and local random variation lead to read errors. Also, write errors can occur due to difficulty in maintaining the device strength ratio in sub-threshold region. The major approach for improving the read SNM is to decouple the cell storage nodes from the bit-line read current, thus making the read SNM equal to hold SNM. To improve WM and write performance, higher supply voltage for the write access transistors [2] and/or write assist circuits are used at the cost of extra supply voltage and extra control circuits.

Several SRAM cell structures that are reliable in sub-threshold operation have been proposed in literature. This paper reviews some of the recent SRAM designs that address stability and reliability issues. The rest of the paper is organized as follows. Section 2 reviews various SRAM designs. Section 3 comprehends the observations and Section 4 concludes the paper.

2. BIT CELLS WITH BETTER STABILITY

2.1 Differential 10T bit cell:

The differential 10T SRAM cells [1] provide isolation of read and write operations leading to improved noise margin. Dynamic differential cascade voltage switch logic (DCVSL) scheme is employed for read access to improve RM. 10T SRAM cell allows bit interleaving with column-wise write access control while having differential read path (Figure 1). It allows large bit line swing despite of extreme process and temperature variations.

![Figure 1: Structure of 10T SRAM cell](image1)

![Figure 2: 12T SRAM cell design](image2)

2.2 Bit–interleaved 12T SRAM cell:

A bit-interleaving 12T sub-threshold SRAM cell is proposed in ref [3] with data-aware power-cutoff (DAPC) with write-assist to improve write-ability to mitigate increased device variations at low supply voltage under deep sub-100nm processes. During write operation, depending on data-in, this bit-cell internally cuts off supply voltage for either the left or right half-cell to weaken the pull-up network, thus assisting the discharging of the storage node. This scheme improves write-ability
without employing additional peripheral write-assist circuits and related boosting and timing control circuits as shown in Figure 2. Furthermore, this bit-cell employs a cross-point write structure with a data aware column-based write word-line (WL) to eliminate write half-select (WHS) disturb.

### 2.3 Ultra low power 9T SRAM cell:

To mitigate the issue related to read SNM and sense margin, a differential read-decoupled 9T SRAM cell (Figure 3) with column bit-interleaving capability is proposed for ultralow-power application. For this 9T based architecture, the desired cell is selected during write operation by pulling up the WL and enabling the chip select line (CSL) to mitigate write-half-select issue. LP9T [4] also exhibits narrower spread in read current, read stability and hold power compared to other cells.

![Figure 3. Ultra low power 9T cell](image)

### 2.4 Differential sense amplifier based 8T SRAM:

An area-efficient sub-threshold SRAM where the cell array employs the conventional SE-8T SRAM [5] bit cell is shown in Figure 4 with bit-interleaving architecture. The read scheme exploits the reference-based sense amplifier to read data out. This two-port cell topology has a 6T storage cell and a 2T read-buffer which isolates the data-retention structure during read-accesses. Consequently, the read SNM limitation is eliminated. The other two prominent limitations, namely bit-line leakage and write ability in the presence of variation are dealt using the peripheral assists. In this work, the high-threshold PMOS is used for the cell core exclusively to enhance the write ability [6].
2.5 13T dual driven feedback mechanism bit cell:

This 13T bit cell is a pioneer solution for embedded memories in low-power space applications [7]. The dual-driven separated-feedback mechanism is introduced to improve the bit cell robustness. The 13T bit cell features single-ended readout through the read access transistor. However, due to the strong dual-driven feedback mechanism and the indirect write operation through the weak feedback nodes, the cell provides robust half-select stability.

![Figure 4. Basic 8T bit cell](image1)

![Figure 5. Schematic of 13T SRAM cell](image2)

3. SUMMARY

Table I compares key features of five sub-threshold SRAM bit cells with better stability compared to previous designs. Sub-threshold SRAM cells [5] used single-ended read paths improved in 10T. The DAPC12T cell exhibits better write stability than single-ended disturb-free (SEDF9T) cell [2] and bit-interleaving 10T (BI10T) cell [1] due to the power-cutoff write technique. The mean value of WSNM of the 12T cell is 1.38 and 2.2 of the conventional 8T [5] and 10T cell respectively. LPT9T cell provides 1.6X improvement in read delay and achieves 3.9X read SNM during read operation compared to fully differential 8T[6]. Implementation of SRAM arrays based on the proposed 13T bit cell provides average leakage power consumption less than 5pW per bit at 300mV with highest area.

![Figure 6: Area overhead with reference to 6T cell](image3)
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Figure 7: Supply voltage of bit cells

Table 1: Comparison of bit cells

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<td>180</td>
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<tr>
<td>Half select stability</td>
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<td>Yes</td>
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<td>4.05; N.A</td>
<td>3.4;2.2</td>
<td>&lt;5pW</td>
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Figure 7: Comparison of frequency of operation
From Figure 6, it is observed that SE-8T consumes less area compared to other bit cells. Figure 7 shows that the differential 10T has the minimum operating voltage, but operating under 300mV needs additional circuitry to optimize the read stability resulting in area overhead. 13T and 12T structures have high operating frequency; however it results in area overhead due to more number of transistors.

4. CONCLUSION

Voltage scaling is an effective strategy for minimizing the power consumption of SRAMs. Further, as SRAMs continue to occupy a dominant portion of the total area and power in modern ICs, the resulting total power savings is significant. Unfortunately, conventional SRAMs, based on the 6T bit-cell, fail to operate at voltages below approximately 700mV because of reduced signal levels and increased variation. This paper presented a survey on stability of SRAM bit cells comparing various parameters such as operating voltages and frequencies. From this study it may be concluded that the 8T SRAM cell has good stability compared to 9T SRAM cell since both layout under same 65nm technology in terms of leakage power, area with considerable operating frequency and voltage.

REFERENCES


