

A Comprehensive Analysis of Design and Simulation of Area Efficient CRC Algorithm for ZIGBEE Application

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Abstract

In this paper, the design of area efficient ZigBee Digital Transmitter is proposed. Several researchers have designed the ZigBee transmitter using a Matlab or Simulink, a Schematic and also using VHDL which implemented through Spartan and Virtex FPGA family. The Digital Transmitter is designed using Verilog, which uses less number of slices, LUTs, etc. The paper is aimed in designing ZigBee transmitter for PHY & MAC layer of IEEE 802.15.4 standard using Verilog is to be analyzed with the simulated results which are obtained through Xilinx in order to reduce the cost and complexity. During the process, both the physical and MAC layers are studied and configured accordingly to the power constraints and surrounding environment. The evaluation of simulation mainly confirms in fixing the errors. The error detection techniques which are most commonly used are redundancy check, checksum, longitudinal redundancy check, and cyclic redundancy check which are done during the proposed research work. Using the CRC the proposed work attempts to detect 99.99% errors during transmission. The block check sequence uses the 16 bit width in CRC-16 to generate the continuous binary number with the data stream. The 20% of reduced area is achieved for proposed system when compared to existing system.

Keywords: ZigBee, CRC, LUTs, occupied slices, Xilinx, Verilog, MAC, PHY.

1. INTRODUCTION

The power of wireless communication is rapidly progressing towards a newer direction in establishing personal wireless networks built on low power systems. Evolutionary communication technologies like WIFI, bluetooth, and ZigBee predominantly play a major role in the life of a common man. Of the late, ZigBee is slowly getting its popularity in establishing personal wireless networks which is built on small and low-power digital radios. Conceptually ZigBee can be viewed as a specification for a suite of advanced communication protocols which are primarily used to establish personal area networks. The technology is developed based on an IEEE 802.15.4. Despite of its low power consumption bounds transmission distances to 10–100 meters line-of-sight, still ZigBee devices based on input power and surrounding environment, can transmit data over long distances by passing data through the help of a mesh network which is comprised of intermediate devices to reach more distant ones. Applications of ZigBee include wireless electrical switches, electric meters with in-home-displays, traffic management systems, industrial equipments and other consumer products which requires short-range low-rate wireless is aimed to be simpler and economically cheaper than transfer of data. The technology which was defined by the ZigBee specification and other contemporary wireless personal area networks (WPANs), such as Bluetooth or Wi-Fi. The technology has been developed during late 1990's and got standardized in the year 2003. Several revisions in the suite of ZigBee protocols are still going on done to establish effective and efficient personal wireless networks.

ZigBee can be used as a wireless networking standard that is primarily aimed at remote control and a sensor based applications which are suitable for operation in the environment of sever radio. It was builds on IEEE standard 802.15.4, which would define the PHY and MAC layers. The specification also defines the application and security layer specifications enabling interoperability between products from different manufacturers. Such enhancement makes ZigBee as a superset of the 802.15.4 specification. NetSim, NS2, and OPNET are some network simulators which can be used to simulate IEEE 802.15.4 ZigBee networks. These simulators are developed using open source C or C++ libraries and have been released for users to modify the simulators. In this way the users can be able to determine the validity of new algorithms prior to hardware implementation.

2. OBJECTIVE OF THE WORK

Numerous procedures, methods and tools available with the theory of electronics concepts that drive in developing resulted hardware components. Real-time operational evaluation to assess the nature of hardware component, process or method in an embedded circuit sometimes could not deliver the expectations because of their criticalness. After a thorough survey of literature, it is found that several researchers have designed the ZigBee transmitter using a Mat lab/Simulink, a Schematic and also using VHDL targeted for Spartan and a Virtex FPGA family. The Digital Transmitter is to be designed using Verilog which would use less number of Slices, LUTs, etc. The problem is to evaluate by simulation of the underlying nature of ZigBee transmitter with respect to its MAC and PHY layer using the widely accepted and

advanced hardware description language Verilog. Thus, the proposed research work is aimed in designing of ZigBee transmitter for PHY & MAC layer of IEEE 802.15.4 standard by using Verilog and to be analyzed with the simulated results obtained through Xilinx in order to reduce cost and complexity. The proposed design operation performance should satisfy the specifications mentioned in theory and must be verified with the simulation results.

To accomplish the objectives, compatible algorithms or procedures have to be developed using Verilog HDL. During the process, both the physical and MAC layers are studied and configured accordingly to the power constraints and surrounding environment. The evaluation of simulation mainly confirms in fixing the errors. The error detection techniques which are most commonly used are redundancy checking, checksum, longitudinal redundancy checking, and cyclic redundancy checking which are done during the proposed research work. Using the CRC the proposed work attempts to detect 99.99% errors during transmission. The block check sequence uses the 16 bit width in CRC-16 to generate the continuous binary number with the data stream. The proposed transmitter is assumed to be working at the ISM frequency 2.4GHz and the modulation technique adopted is Offset quadrature phase-shift keying (*OQPSK*) with half sine pulse shaping. The proposed system is designed with a data rate of 250 Kbps over a 16 channel medium operating on a 2.4GHz. The channel spacing is fixed with 5MHz working with direct sequence spread spectrum at a chip rate of 2 Mega chips per second.

3. ZIGBEE TRANSMITTER

3.1 Specifications

ZigBee [13] is a high-level communication specification suite based on an IEEE 802.15.4 is meant for establishing Personal Area Networks based on low-power digital radios. Normally ZigBee devices have the transmission capacity of 10 – 100 meters due to its low power consumption. However, these devices could also transmit data to long distances with the help of intermediate boosting devices. ZigBee networks are potentially secured by 128-bit symmetric encryption keys and are widely used in low data rate applications. Applications of ZigBee include domestic electric meters, wireless light switches, traffic management systems, industrial data exchange systems etc. ZigBee chips are integrated with microcontrollers and radios that work in the range of 60 – 256 KB flash memory. ZigBee is the simpler and cheaper than other wireless personal area networks like WIFI and Bluetooth. The concept ZigBee was designed in the year 1998, standardized in 2003, and enhanced for revision in the year 2006. The name has been coined representing the waggle dance of honey bees after their return to the beehive.

ZigBee chips are typically integrated with radios and with microcontrollers that work in the frequency range 60-256 KB flash memory. Table 1.5 lists the worldwide operational frequency range of ZigBee. The minimum data range is 20 kbit/s (868 MHz band) and can work up to 250 kbit/s (2.4 GHz band of Frequency). The

network supports star, tree and mesh topology. A network coordinator device is to be dedicated to the network for controlling and maintenance.

The PHY and MAC layers of ZigBee are defined in IEEE standard 802.15.4 for low rated WPANS. Four (4) additional key components via application layer, network layer, a *ZigBee device objects* (ZDOs) and also manufacturer defined application objects for user specific customization are included in the ZigBee network. The specifications are given in the Table 2.

Table 1. Worldwide operating frequency range of ZigBee

Geography	Standard Regulatory frequency Range
China	784 MHz
Europe	868 MHz
USA and Australia	915 MHz
Other Nations	2.4 GHz

Table 2. Specifications

PARAMETER	SPECIFICATION
Data rate	250 Kbps
No. of channels	16
Operating frequency	2.4 GHz
Channel spacing	5 MHz
Spread spectrum	Direct Sequence Spread
Chip rate	2 Mega chips per second
Modulation	OQPSK with Half sine Pulse
Spectrum	shaping

The frame structure of 802.15.4 MAC is depicted in the figure 1. The MAC frame composed of MAC header (MHR), MAC payload or service data unit (MSDU) and MAC footer or FCS. The basic MAC frame has frame control field of 2 octets. This indicates the type of frame, source and destination addresses.

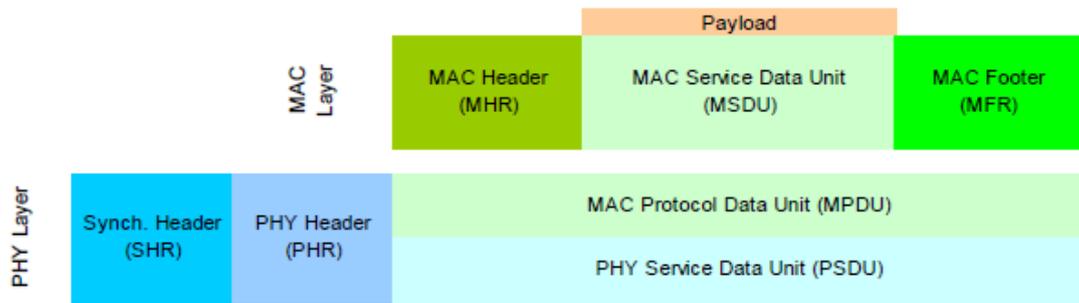


Figure 1. MAC basic frame structure

The IEEE 802.15.4 defines four MAC frame structures: beacon, data, acknowledgement and MAC command frames. The beacon frame is transmitted by a coordinator. The beacons are used for synchronizing all the device clocks within the same network and for transmitting the data a data frame is used. Meanwhile, the acknowledgment frame is used to confirm successful frame reception. The MAC commands are transmitted using a MAC command frame.

3.2 Architecture

The super-frame specification in the Beacon frame manages in synchronizing the associated devices, publicizing the existence of PAN, and informing the pending data between coordinators. The super-frame is composed of two parts i.e., active and inactive (refer figure 1.21). Again, the active component is comprised of 16 slots, can further be divided into two subcomponents namely contention access period (CAP) and contention free period (CFP). Inactive part holds the slept devices.

Devices use the slotted CSMA/CA for the usage of the channels in a beacon enabled network. Unslotted CSMA/CA channel mechanism is employed in non-beacon enabled network. Also, network coordinators could provide guarantee time slot (GTS) to the FFDs based on the requisition for fixed rate transmission. The PAN coordinator can be allocated upto 7 GTSs simultaneously. Two parameters control the structure of super-frames. They are beacon order (BO), provide the length of a super-frame and super-frame order (SO), and gives the length of the active portion of the super-frame. A relationship has been developed and evaluated between BO and SO in a beacon enabled network. The relationship is given in the equation 1.

$$0 \leq SO \leq BO \leq 14 \quad \dots 1$$

Duty cycle deals could be the ratio of active period to the whole frame duration and is represented in the equation 2. This indicates that the each device gets active for $2^{-(BO-SO)}$ duration of time and goes to sleep for $2^{-(BO-SO)}$ portion of time.

$$\text{Duty Cycle} = 2^{-(BO-SO)} \quad \dots 2$$

In the 802.15.4 standard, the association parameters are informed in an indirect fashion. Coordinator receives the association request raised by the devices and responds by appending the *long address* of devices in the beacon frames. Thereafter devices are required to send a data request to the coordinator to fetch the association result. Once association is established, each device will be assigned with a 16-bit *short address*. Figure 2 illustrates the procedure of establishing the associated with the coordinator.

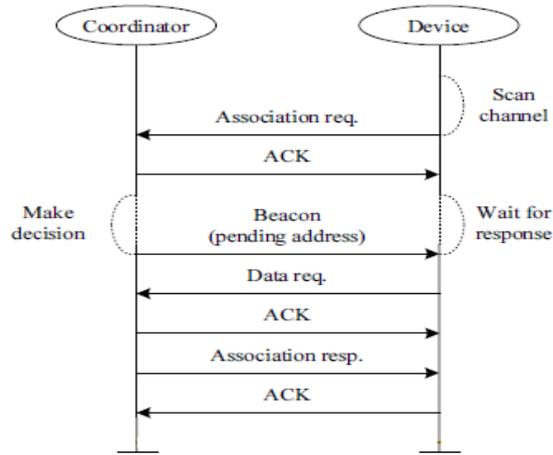


Figure 2. Association Procedure

In the data transfer process for a Beacon enabled network, device locates the beacon to synchronize its super-frame specification. Here CSMA/CA protocol is employed to transmit the data. In a non-beacon enabled network, data transfer is performed by device using unslotted CSMA/CA. Figure 3 illustrates both the data transfers in the ZigBee MAC.

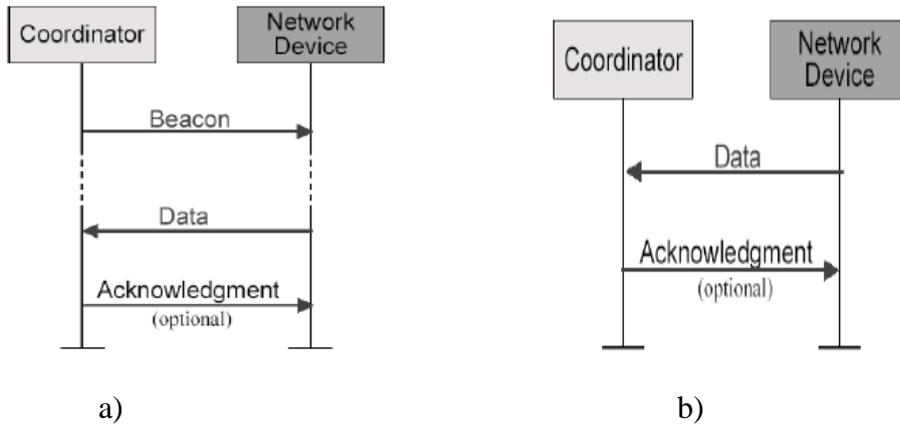


Figure 3. Data Transfer in a) Beacon network enabled b) non-beacon network enabled ZigBee MAC.

3.3 Existing system

The ZigBee digital transmitter is designed for an acknowledgment frame which is shown in Figure 3 based on IEEE 802.15.4 standard. In existing work, the resultant signal from the general architecture will be amplified and then transmitted. This will undergo inter symbol interference. This would result in erroneous information transmission.

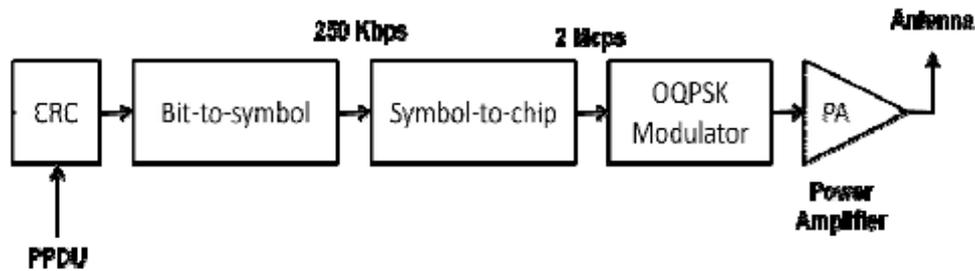


Figure 4. Transmitter Architecture

3.4 Proposed system

A ZigBee transmitter is to be designed for PHY and MAC layer for an acknowledgement frame. This design (Refer figure 4) is going to be modeled using Verilog HDL and simulated through Xilinx. The performance in terms of power utilization of operation of the proposed design should satisfy the theoretical specifications and is evaluated with the simulation results.

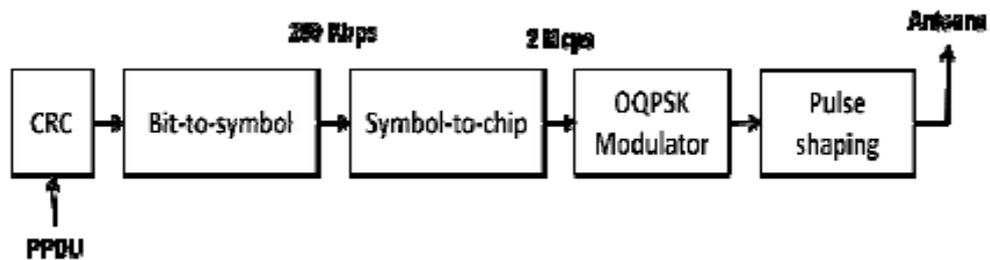


Figure 5. Proposed Transmitter Architecture

Since the output of the modulator is not assured to be transmitted without error. So, in order to avoid such distortions, at the output of OQPSK Modulator a Pulse shaping Block has to be added. This would avoid some transmission noises and Inter Symbol Interferences.

4. DESIGN METHODOLOGY

4.1 Proposed method algorithm:

The design algorithm defines the frame structure generated by ZigBee MAC layer as follows in Figure 6. Generic MAC layer frame has frame control field with 2 octets. The frame control field carries the useful information like frame type, source and destination addressing modes. The Frame type specifies if the frame is beacon frame, data frame, ACK frame of data, MAC command frame etc. The same is outlined with

Frame type subfield in the table with 3 bits. The Sequence number describes the frame sequence order. Destination address is sent first to indicate the target device which is ready to receive the data. Source address is sent after to indicate from which device data is received to the target. Security control field indicates whether outgoing frame is security enabled or not. The Actual data is sent on a payload field. At last the frame check sequence is sent to tell the receiver whether the data is received correctly at the destination or it may collided with unknown data. The receiver also calculates the frame check sequence according to the same polynomial used by the transmitter to calculate the frame check sequence.

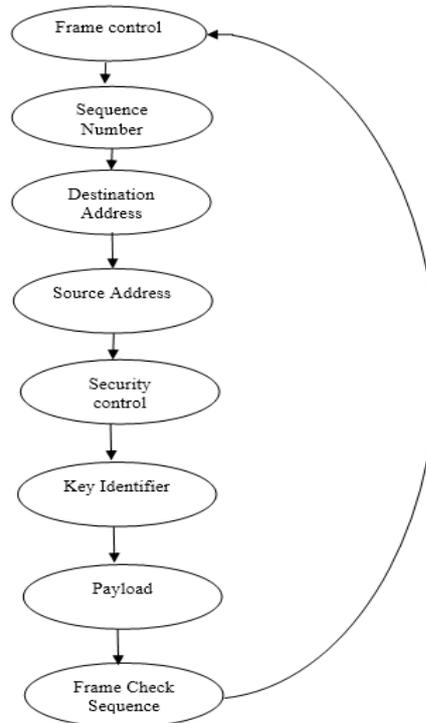


Figure 6: Algorithm used for ZigBee MAC transmitter design

4.2 Frame check sequence

4.2.1 Cyclic Redundancy Check

An Error detection is defined as a process to generate the redundant bits using the CRC polynomial with respect to data transmission and identifies the error occurred by comparing the CRC generated with the receiving CRC. Error-detection techniques, only detects whether an error occurred in the transmitted signal but will not correct any errors nor identifies the error position. The main purpose of error detection technique is not preventing errors from occurring but prevents undetected errors from occurring.

The error detection techniques which are most commonly used are redundant bit check such as vertical redundancy check, checksum, longitudinal redundancy check, and cyclic redundancy check.

4.2.2 CRC polynomial

The most reliable redundancy checking technique for error detection is a convolutional coding scheme which is called as cyclic redundancy check (CRC), with CRC, approximately 99.999% of all errors that occur during transmission can be detected. In CRC-16, 16 bits are used for the block Check sequence. Here the complete data stream is treated as a long continuous sequence of binary digits. The Block Check Sequence is being transmitted separately from the message and CRC is considered a Systematic Code. Cyclic Block Codes are more frequently written as (n, k) cyclic codes where n = bit length of transmission and k = bit length of the Message. Therefore, Block Check Length Character (BCC) in bits is

$$BCC = n - k \tag{1}$$

A CRC-16 BCC is the process of binary division to obtain the remainder. P(x) is the generator polynomial is used to divide the message polynomial G(x) to obtain the remainder and append to the BCS message. The generator polynomial must be a prime number. With CRC generation, the division is not accomplished with standard arithmetic division. In the proposed system the division logic is obtained by using modulo-2 division and the remainder is obtained by XOR operation. Whereas in the data stream which includes CRC code, received at the receiver side is being divided by the Generating polynomial function P(x). Remainder will be zero if no transmission errors are present in the received data.

Mathematically, a CRC can be expressed as

$$\begin{array}{l} G(x) \\ \text{-----} \\ P(x) \end{array} = Q(x) + R(x) \tag{2}$$

Where

- G(x) = Message Poly,
- P(x) = Generator Poly,
- Q(x) = Quotient,
- R(x) = Remainder,

The generator polynomial for CRC-16 is

$$P(x) = x^{16} + x^{15} + x^2 + x^0$$

4.2.4 Results and discussion

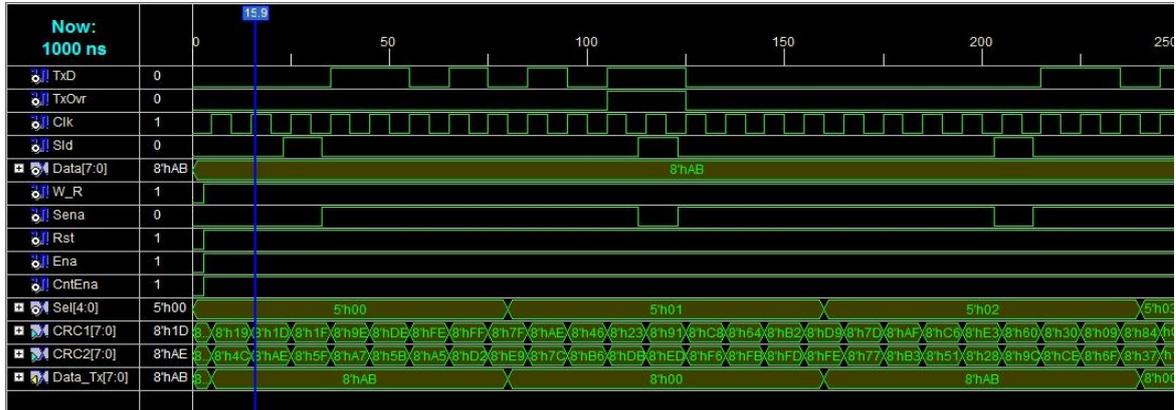


Figure 8. Transmitter Simulation Waveform

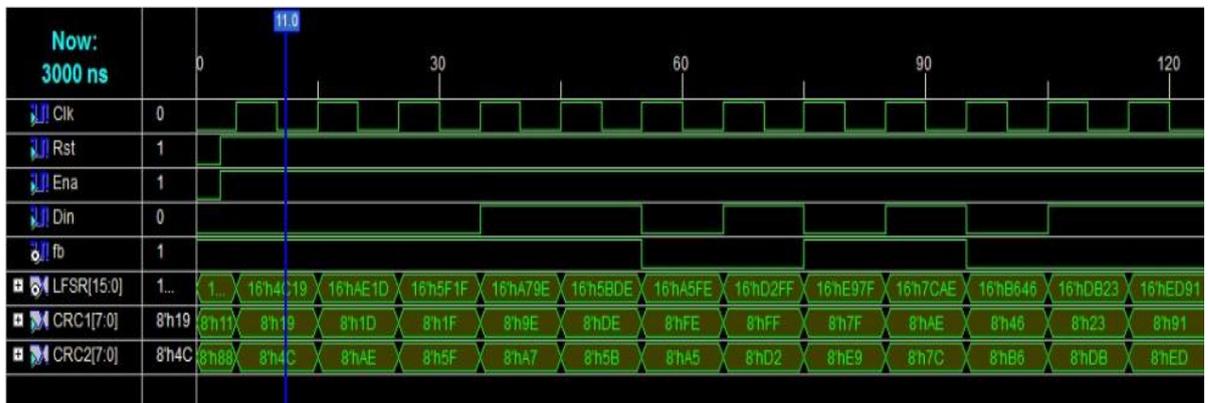


Figure 9. CRC Simulation Waveform

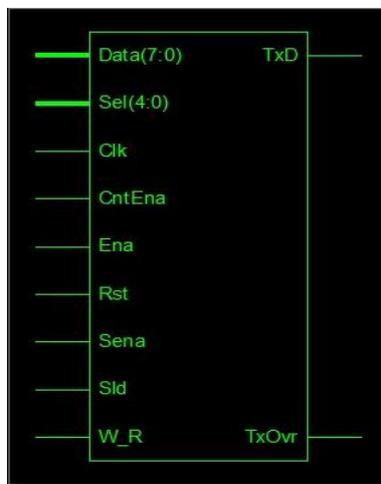


Figure 10. RTL schematic of ZigBee transmitter

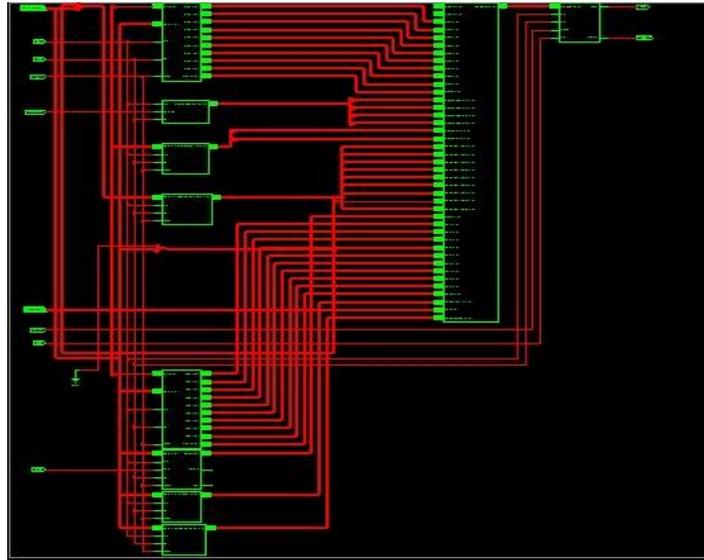


Figure 11. RTL schematic of ZigBee Transmitter

ZIGBEE_CRC Project Status			
Project File:	zigbee_crc.ise	Current State:	Synthesized
Module Name:	TOP_existing	• Errors:	No Errors
Target Device:	xc3e500e-5cp132	• Warnings:	387 Warnings
Product Version:	ISE 9.1i	• Updated:	Sun Nov 13 02:57:05 2016

ZIGBEE_CRC Partition Summary	
No partition information was found.	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	71	4656	1%
Number of Slice Flip Flops	83	9312	0%
Number of 4 input LUTs	138	9312	1%
Number of bonded IOBs	23	92	25%
Number of GCLKs	1	24	4%

Figure 12. Area Report of Existing ZigBee Transmitter

ZIGBEE_CRC Project Status			
Project File:	zigbee_crc.isc	Current State:	Synthesized
Module Name:	TOP_proposed	• Errors:	No Errors
Target Device:	xc3s500e-5cp132	• Warnings:	447 Warnings
Product Version:	ISE 9.1i	• Updated:	Sun Nov 13 03:03:47 2016

ZIGBEE_CRC Partition Summary	
No partition information was found.	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	56	4656	1%
Number of Slice Flip Flops	53	9312	0%
Number of 4 input LUTs	111	9312	1%
Number of bonded IOBs	21	92	22%
Number of GCLKs	1	24	4%

Figure 13. Area Report of Proposed ZigBee Transmitter

The area comparison is shown in the pictogram representation in figure 12.

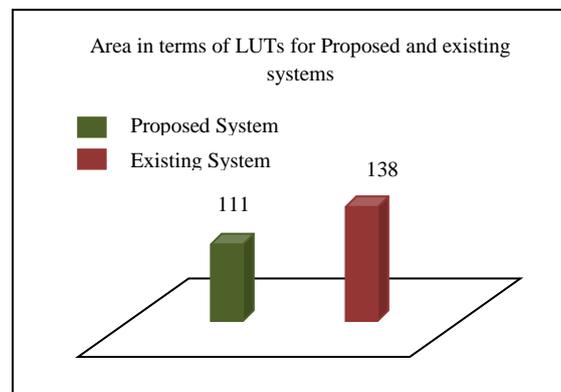


Figure 14. Area representation in terms of LUTs for Proposed and existing System

The digital transmitter was partially designed and synthesized for Spartan 3E with a speed grade of 5. The change in the data transmitter block has reduced the LUT count. This is achieved by replacing the one hot encoding finite state machine to binary with 5 bit width of each present state. The state transition is made between 28 states so instead of using the one hot encoding, the binary encoding has reduced the area in terms of LUT count of a targeted SPARTAN 3E XC3S500E FPGA with a speed grade of 5. From the synthesis results area in terms of slices and LUTs obtained for the proposed ZigBee transmitter is reduced when compared to the existing ZigBee transmitter. As the LUT count reduced the power consumption of a design also reduced.

From the synthesis results area in terms of slices and LUTs obtained for the proposed ZigBee transmitter is reduced when compared to the existing ZigBee transmitter. The 20% of reduced area is achieved for proposed system when compared to existing system.

4. FUTURE WORK PLAN

In order to feed the next block in the Digital Transmitter Architecture the Bit-to-Symbol block output has to be verified. If not this block has to be synthesized and number of slices are to be utilized. Future plan is to study and design Symbol-to-Chip Mapper. This part has to be designed with the help of Direct Sequence Spread Spectrum Technique and further to study and design again the modulation technique i.e., O-QPSK. The O-QPSK modulation technique alone is best suitable for 2.4GHz frequency band of ZigBee Digital Transmitter. Last work plan is to study and design Pulse shaping block for modulated output, which shall reduce all the Inter Symbol Interferences (ISI).

6. CONCLUSION

The Design of Digital Transmitter in 2.4GHz band for ZigBee Applications based on Verilog is clearly discussed in this paper. The CRC behavior and Bit-to-Symbol blocks have been characterized using Verilog. It can be concluded that only a part of the ZigBee Digital Transmitter has been characterized and synthesized. The synthesis is done by using XILINX ISE and targeted for SPARTAN 3E FPGA. The synthesis results obtained for the proposed method shows reduced slices and LUTs when compared to existing method. Hence the proposed method proves the more efficient in area.

REFERENCES

- [1] Khalifa. O, Islam. MDR and Khan. S, "Cyclic redundancy encoder for error detection in communication channels", RF and Microwave Conference, 2004.
- [2] Matloff .N, "Cyclic redundancy checking", Department of Computer Science, University of California, 2001.
- [3] Rafidah Ahmad, Othman Sidek, Wan Md. Hafizi Wan Hassin, Shukri Korakkottil Kunhi Mohd, and Abdullah Sanusi Husain, "Verilog-Based design and implementation of Design Tansmitter for ZigBee Applications", International Journal of Emerging Sciences, 723-724, December 2011, ISSN: 2222-4254, © IES.
- [4] Rahmani.E, "ZigBee/IEEE 802.15.4", University of Tehran, 2005.
- [5] Shuaib.K, Alnuaimi.M, Boulmalf.M, Jawhar.I, Sallabi.F and Lakas.A, "Performance evaluation of IEEE 802.15.4:Experimental and simulation results", Journal of Communications, 2, 4(2007): 29-37.

- [6] Sunil Shukla, Neil W.Bergmann, “Single bit error correction implementation in CRC-16 on FPGA”, Proceedings of IEEE International Conference on Field-Programmable Technology 2004.
- [7] Ting Ting Meng, Chen Zhang, Peter Athanas, “An FPGABased ZigBee Receiver on the Harris Software Defined Radio SIP”, SDR Forum Technical Conference, Denver, Colorado, 2007.
- [8] Wayne Tomasi, “Advanced Electronic Communication System”, 6th Edition, Pearson Education.
- [9] ZigBee Alliance, available at: www.ZigBee.org.

