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March Test Compression Technique on Low Power Programmable Pseudo Random Test Pattern Generator

A. Madhuri
M.tech – Scholar

Bantupalli Kishore Babu
Associate Professor

R Sambasiva nayak
HoD

Department of E.C.E, Sri Chundi Ranganayakulu Engineering College
Ganapavaram (Po), Nadendla (Md) Near Chilakaluripet, Guntur,
Andhra Pradesh 522619, India.

Abstract

In this paper, Memories of Flash are another type of memory of non-volatile on floating-gate transistors. The use of commodity and embedded memories of flash has rapid growth while we are entering in the system-on-chip era. Conventional tests for flash memories are usually ad hoc is the test procedure which is developed for a specific design. As there is a large number of possible failure modes for memories of flash, algorithms of long test that is automatic test equipment (ATE) which is complicated are commonly seen. Production row and column address bit cell as basis to probe for any possible weaknesses of the process or design in SRAM. There may be occurrence of sa0 and sa1 faults in any chip design, these faults are overcome by using row and column address cells we make perfect location to store the data and no cross sections of SRAMS.

Keywords: System-on-Chip, Automatic Test Equipment, Pseudo Random Test Pattern Generator, Process Control and Monitoring

I. INTRODUCTION:

The important role play of SRAM increased in SOC applications. Statistics shows that on average the total area of the chip exceeded 50% by SRAM. In, reported by us on the development of the smallest high-density 6T-SRAM cells for SOC using standard

CMOS processes (3.87um2 for 0.18um technology node and 1.87 um2 for 0.13um technology node). And these particular cells are the most suitable in the applications of SOC to meet the demand for high-density and high-performance, and are vastly manufacturable. To make sure their manufacturability, robustness and reliability, ordinary PCM structures of test aren't adequate to monitor the process for the high density SRAM, due to specific interactions between the SRAM design and the process. PCMs of ordinary are more generic in nature and are aimed at supporting the process module of robust development characteristics and robust generic design rules that can be used in any possible combinations and design environments. Therefore, these structures may not always allow us to test for the robustness of the chosen design of SRAM rules of their environment of the specific SRAM array. For example, a structure of conventional poly bridging is designed that the robustness of the minimum poly-to-to-poly spacing design rule to be proved for very long and parallel poly lines. This structure may not be suitable for providing feedback for our SRAM, as typically the poly layer features of SRAM are more complex. The metal bridging also may be applied same, where the SRAM pattern is more complex in nature than that of a simple collection of metal lines of parallel and spacing of uniform. A conceptual change in designing and using electrical test structures for SRAM-driven process development is thus needed: test structures need to be process-development driven as well as product driven. The set of the structures of the test is used for developing and characterizing the process needs to be complemented with a set of suitable structures that prove the robustness of the high density SRAM design and help quickly be identified and related yield issues to corrected the process and to be designed in SRAM during the development phase.

II. PRPG SYSTEM:

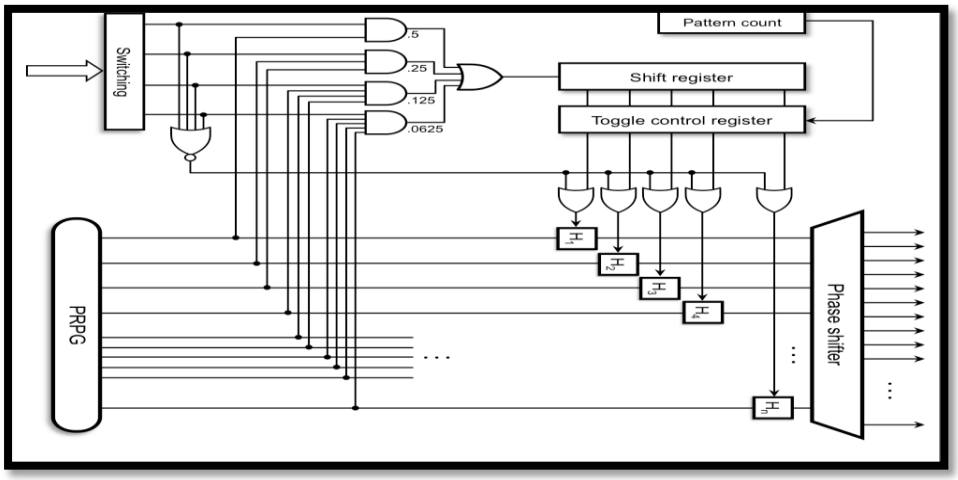
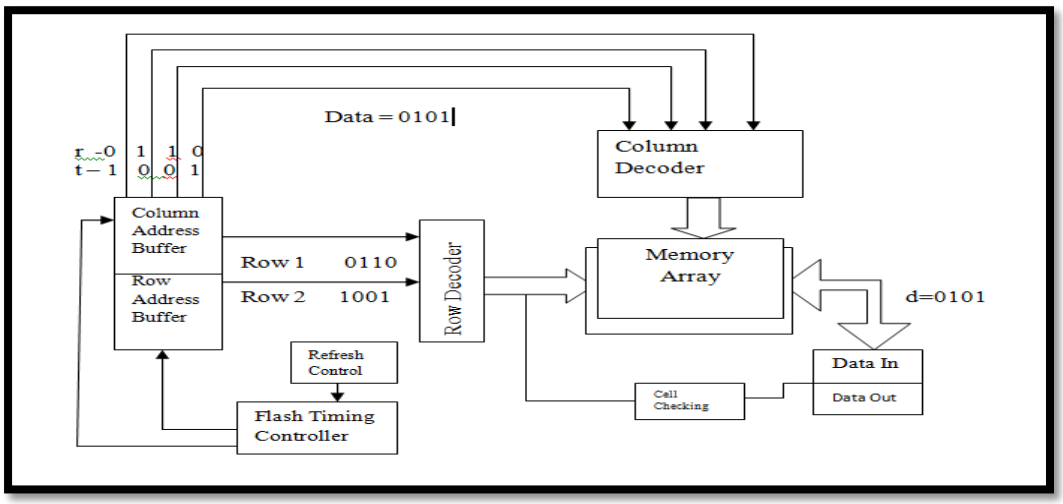


Figure: PRESTO Generator

The basic structure of a PRESTO generator. An *n*-bit PRPG connected with a phase shifter feeding scan chains forms a kernel of the generator producing the actual pseudorandom test patterns. A linear feedback shift register or a ring generator can implement a PRPG. More importantly, however, *n* hold latches are placed between the PRPG and the phase shifter. Each hold latch is individually controlled via a corresponding stage of an *n*-bit toggle control register. As long as its enable input is asserted, the given latch is transparent for data going from the PRPG to the phase shifter, and it is said to be in the toggle mode. When the latch is disabled, it captures and saves, for a number of clock cycles, the corresponding bit of PRPG, thus feeding the phase shifter (and possibly some scan chains) with a constant value. It is now in the hold mode. It is worth noting that each phase shifter output is obtained by XOR- outputs of three different hold latches. Therefore, every scan chain remains in a low-power mode provided only disabled hold latches drive the corresponding phase shifter output. The selection of memory may be effected by S.A0 and S.A.1 faults. So, to overcome this we proposed a design as shown below.

III. LOW POWER DESIGN



There are two locators i.e., column address and row address buffer which are send the files to the column decoder and row decoder respectively. Further, they will be sent to the memory array which is indicated as columns and rows as 0110 & 1001 respectively.

Column Address Buffer: An address buffer circuit for a semiconductor memory device wherein an address buffer is enabled (to output an internal address signal) in response to a first level of a control signal and, but is disabled in response to a second level of the control signal. An address buffer control unit generates the control signal at the second level in 'no operation' state (NOP command) in which the semiconductor memory device does not perform data accessing operations and generates the control

signal at the first level while the semiconductor memory device performs data accessing operations, thereby reducing or minimizing the output of an internal address buffered and output by the address buffer at and thus reducing power consumption during no-operation states of the semiconductor memory device.

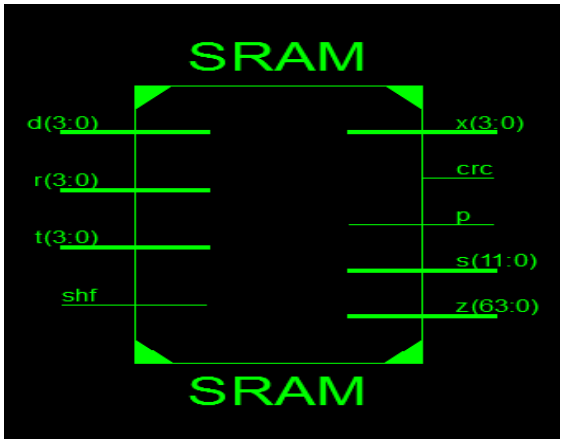
Column Decoder: A memory having multiplexed address inputs uses a column decoder which is deactivated during row address time and becomes activated during column address time. Access time and power dissipation are reduced since the column decoder need not be fully recovered after row address information has terminated and column address information is available.

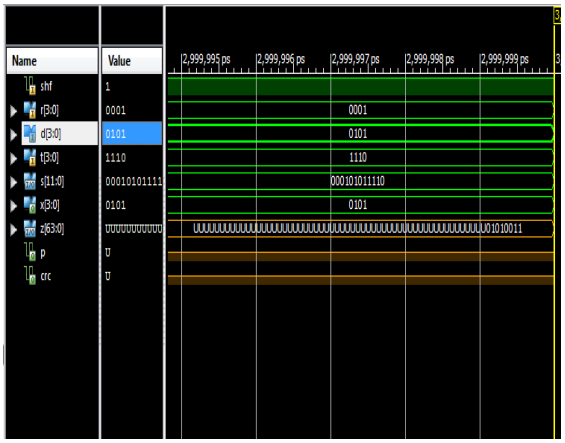
Row Address Buffer: Traditionally, RAM, or Random Access Memory, was used to describe a memory which offered the same access latency for all its memory locations. This is barely the case with modern DRAM systems. In this post, I describe a ten thousand foot view of how modern DRAMs work with the hope that it can help the programmers in choosing their algorithms and data structures wisely.

Memory Array: The data came from column decoder and row decoder will be stored at the Memory Array and further it will be transferred to data out. Typically want an aspect ratio that is not too far from square assertion of word line accesses all cells in a row not all bits that are read from a row may be used. Loading on word line is high! Sense Amp function is to detect bit line change and produce a full '0' or '1' for output latch.

IV. RESULTS

RTL Schematic and OUTPUT Waveform





V .CONCLUSIONS:

Modern VLSI design is moving towards a system on chip to integration of different transistor designs. This proposal presents a current mode interface circuit with calm (content adiabatic logic memory selection). The proposed architecture is based on new sparse clustered SOC using logical connections that eliminates the parallel comparisons during a search. By using different logic sensing to applicable for memory location selection to get a hybrid cluster. The hybrid cluster is consists of different memory locations with different address. Production row and column address bit cell as basis to probe for any possible weaknesses of the process or design in SRAM. There may be occurrence of sa0 and sa1 faults in any chip design, these faults are overcome by using row and column address cells we make perfect location to store the data and no cross sections of SRAMS.

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