# High Performance and Low Power D Flip-Flop using Pulsed Latch Technique

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## Abstract

The traditional ASIC design majorly comprises of flip-flops and latches as the basic elements of any sequential circuit. But due to the miniaturization of VLSI circuits there is a need of reducing the effective power dissipation and overall time consumption. The Pulsed Latch is introduced to enable a significant reduction in the area without compromising the performance of the sequential circuits. Tanner EDA has been used to implement a Pulsed D-Latch which is triggered using pulse from a pulse generator. Analysis shows reduction in power dissipation and overall delay in the circuit with increased performance.

**Keywords***:* D-Latch, Pulse generator, Pulsed Latch.

## Introduction

Flip Flops and latches are the basic elements of any sequential circuit. In order to enhance the performance of any sequential circuit, flip flops and latches have to be optimized. Edge-triggered flip flops are most preferred sequential elements because its timing model is simple. Timing considerations in a traditional flip flop are given by the following equation:

Time Period <= $T_{cq} + T_{su} + \delta$ [6]; where

$\delta$ = Delay of the combinational circuit

$T_{cq}$ =Clock to Q delay of the flip flop

$T_{su}$ =Setup time of the flip flop

The Figure of Merit (timing parameter) of the flip flop is given by $T_{cq} + T_{su}$ and $\delta$ is independent of the circuit. Since the time for combinational blocks which lie between flip flops is fixed, therefore flip flops have reduced timing uncertainties.

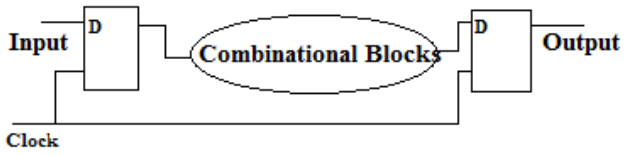


**Figure 1**: Basic sequential circuit

For reliable sampling by the clock, the input data needs to arrive before the clock edge in a flip flop, therefore set up time ($T_{su}$) is positive. As a result $T_{cq} + T_{su}$ (Figure of Merit) is much higher in traditional flip flop based sequential circuit. Apart from that the time for clock distribution is high, thus the total power consumption and the area coverage is increased.

For better performance, designers moved on to level-sensitive latches as basic sequential element. Latches have low timing overhead of the range 2 to 4 Fan Out of 4 delays [1] which is quite less compared to flip flops that have upto 6 to 10 Fan Out of 4 delays [1].The level sensitive latch becomes transparent in the time interval only when the clock is high. This protects the circuit from clock skew and jitter [3]. However, the realization of ASIC designs using latches is difficult due to the complexity of timing model. Moreover, latch based designs may have greater hold-time violations due to large switching time periods. Overall latches and flip flops may employ a large amount of power in any VLSI designs. The total power dissipation may go as high as 80% of the total clock power [4].

As compared to the conventional sequential circuits, Pulsed Latches have been observed to be more efficient .These latches act as alternative sequential elements ruling out the gaps between latches and flip flops. Pulsed latches can be operated from short pulses. These short pulses are obtained from a Pulse Generator (also termed as a Pulser circuit) which is fed directly with an input clock signal. Pulsed Latches are also termed as Spinner cells. Such circuits are robust, more reliable and consume lesser power [12]. It also helps in minimizing the timing delays and figure of merit.

## Pulsed Latch Technique

In a Pulsed Latch, the input clock is replaced by a pulse generated from a Pulse Generator circuit, which drives the subsequent circuit elements. It reduces the load by a factor of 2-3 which yields better performance [8]. Complex Pulsed Latch based circuit can be implemented by Implicit or Shared manner. In the Implicit structure [11], the pulse generator is implicitly available within the latch to be driven. Because of the short distance between the pulse generator and latch, such implementation causes lesser distortion of the pulse. While the Shared structure has a pulse generator circuit present explicitly and the pulse hence generated can be shared by all the latches to be driven. This structure increases effective area utilization of the circuit but consumes greater power. [5]

## Pulse Generator

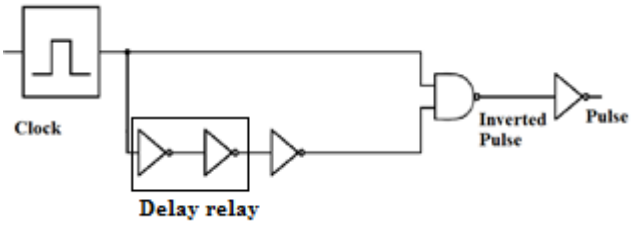


**Figure 2:** Pulse generator

Pulse Generator circuit is used to generate short pulses by introducing Delay relay. A Delay relay can be implemented by a series of inverters as shown in figure 2. The components of the circuit itself set the duration of each pulse. In this circuit, the input clock is logically ANDed with delayed clock from a series of inverters to obtain a pulse. The output of the NAND is low when both the inputs that is the clock and the delayed clock are set high. In this brief time window the short pulse is obtained. This is the inverted pulse. An inverter is employed at the final stage to obtain the required pulse wave. The delay width of hence obtained pulse can be altered by changing the number of inverters in the delay relay, which is used for delaying the input signal. The output of the latch is enabled by either rising or falling edge of the input pulse signal.

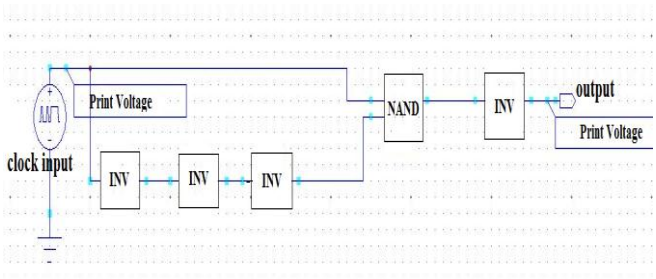


**Figure 3**: Schematic of pulse generator

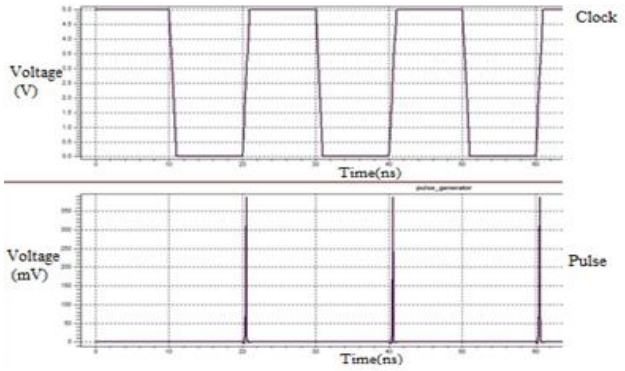


**Figure 4**: Pulse generator waveform

Figure 3 shows the schematic implementation of the pulse generator used for generating a pulse of 1ns. The resultant waveform is shown in figure 4.

## D-Latch

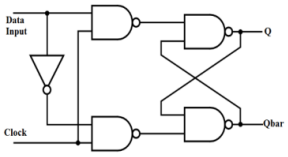


**Figure 5**: D-Latch using NAND

D-Latch is used to remove the undesirable indeterminate state condition in SR latch when S and R is equal to 1. It has two inputs D(data) and En(enable). D Latch holds data in internal storage. It temporarily stores the binary information. This binary information is transferred to the Q output when the enable is high. This means the output follows the input data until the En is high. Hence, D Latch is also known as Transparent Latch and as soon as the enable goes low, data input again gets stored or held. The Characteristic Equation is given by $Q_{t+1} = D$ [2]. The Truth Table is given below.

| D | $Q_{t+1}$ | State |
|---|---|---|
| 0 | 0 | Reset |
| 1 | 1 | Set |

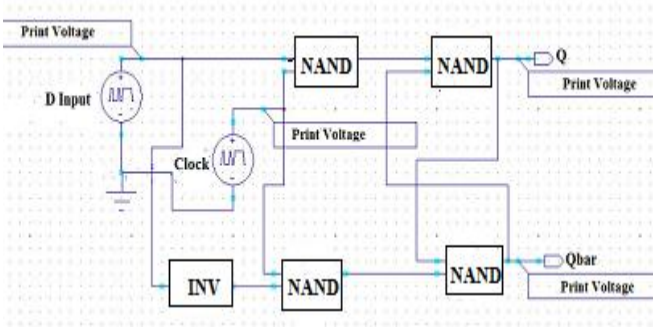


**Figure 6**: Schematic of D Latch using Clock

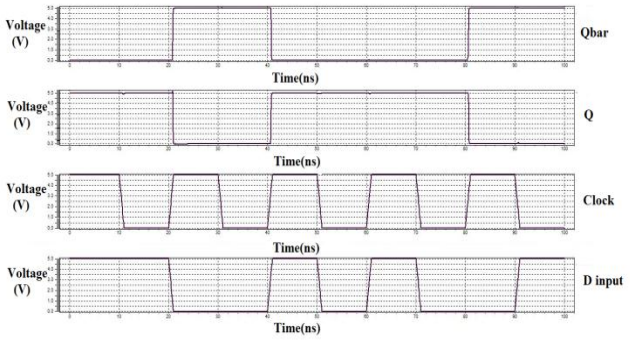


**Figure 7**: D Latch waveform

Figure 6 shows the schematic implementation of the D Latch using Clock and figure 7 depicts its waveforms.

## D Latch using Pulsed Clock

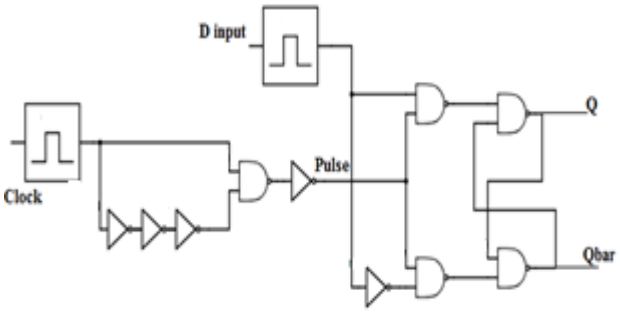


**Figure 8**: D Latch using Pulsed Clock

The circuit aims to drive the D latch using pulsed clock in place of normal clock signal. The clock is provided as an input to the pulse generator that generates the pulsed clock. This generated pulse is now used to drive the D latch instead of normal clock signal. This is done so as to yield better performance in terms of power dissipation and timing overhead as compared to clock triggered flip flops.

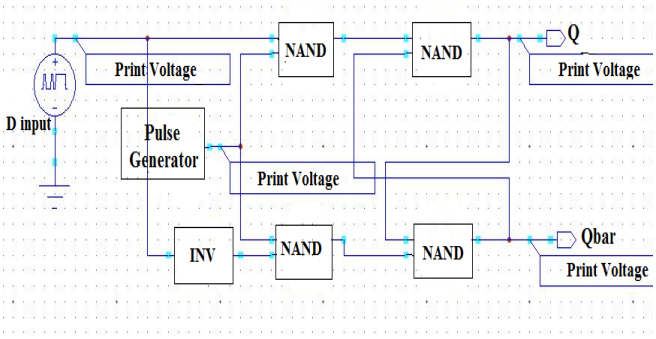


**Figure 9**: Schematic of Pulsed D-Latch

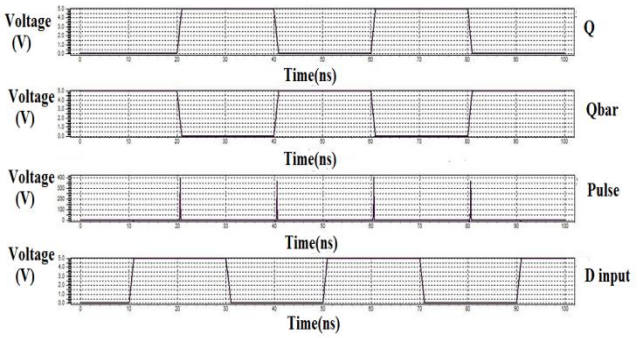


**Figure10**: Pulsed D-Latch Waveform

Figure 9 depicts the schematic of Pulsed D- Latch and the Figure 10 shows its resultant waveforms.

## Results

The implementation of circuits such as D-Latch, inverter, NAND gate and D-Latch using Pulsed clock have been done on Tanner EDA 14.11 using 250 nanometer CMOS technology at 5V power supply. The clock of time period 20 nanoseconds at 150 MHz frequency is given to the pulse generator as input which generates the required pulse of pulse-width 1 nanosecond.

The following table summarizes the power and time delay calculations as obtained from simulations.

| Circuit | D-Latch | Pulsed D-Latch | Percentage Reduction |
|---|---|---|---|
| **Power Dissipation (mW)** | 228.6 mW | 190.2mW | 16.79% |
| **Overall Time Delay (ps)** | 58.9ps | 53.5ps | 9.16% |

The overall power dissipation of basic D-Latch using a clock signal is 228.6 microwatts and a delay of 58.9 picoseconds. The Pulsed D-latch using a pulse clock has a power dissipation of about 190.2 microwatts and a delay of 53.5 picoseconds.

## Conclusion

The Pulsed Latch circuits have been implemented and have been compared with the previous works. It is found that by using Pulsed Latch technique the power dissipation and overall time delay of the D-latch is reduced by 16.79% and 9.16% respectively. The performance of the circuit has improved considerably. Hence, this technique can be employed as a modern approach in designing larger VLSI circuits where the timing complexity at higher abstraction levels of designing are declined.

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