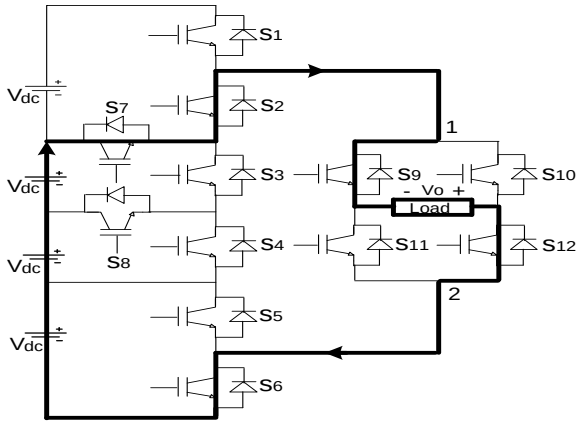

Fig. (g)

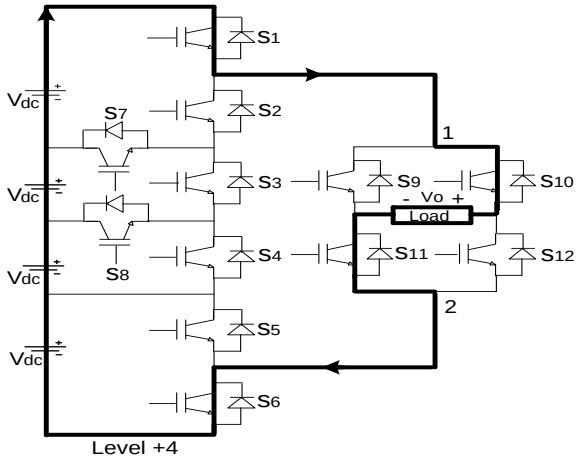

Fig. (h)

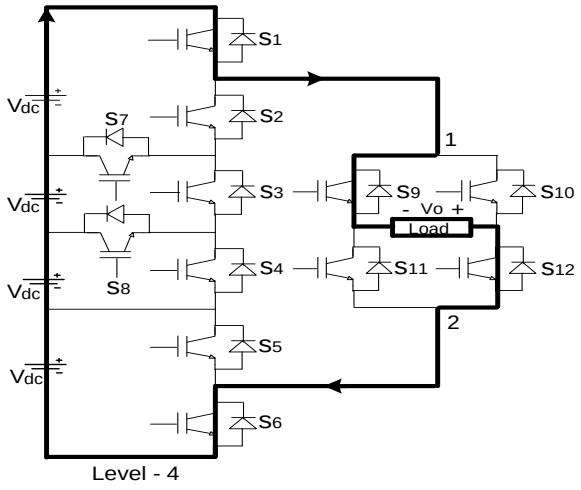

Fig. (i)

Fig. 3.1 are Switching pattern of a N-level Inverter

IV. MODULATION METHODOLGY:-

Various (PWM) pulse width modulation strategy with various relations .of phases are

- PD PWM: This technique is known as phase deposition PMW method:-In phase disposition pulse width modulation strategy, where various carrier waveforms are in same phase shown in fig 4.1 for Five-level MLI. For Nine-level MLI, Eight triangle carriers are required.

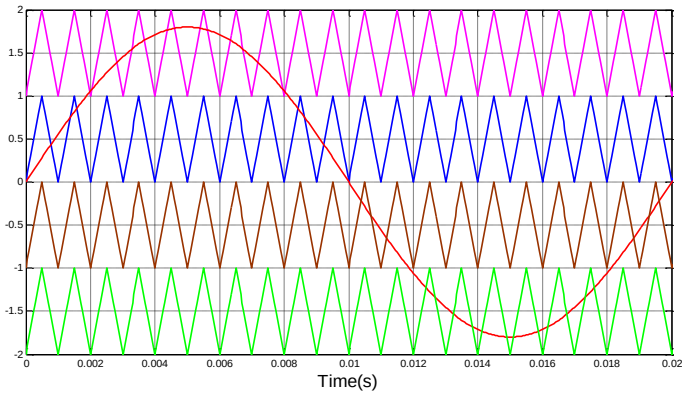

Fig. 4.1: Carrier understanding for PDPWM strategy (ma=0.9 and mf=20)

- POD PWM Shown in fig 4.2 (Phase opposition disposition pulse width modulation) :- In phase resistance disposition PWM policy, In which various carrier wave below a particular reference(which is zero) are 180^0 out of phase and above a particular zero reference are in phase.

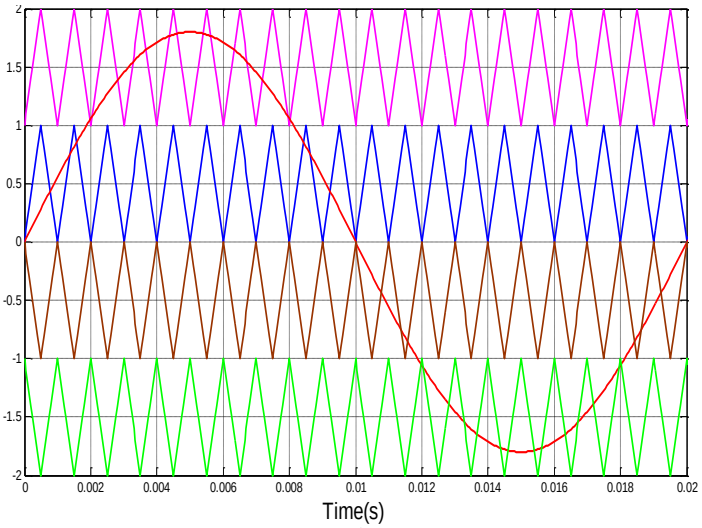

Fig. 4.2: Carrier agreement for PODPWM topology

- (APOD PWM) Shown in fig 4.2 alternating phase resistance temperament pulse width modulation :- In alternating phase resistance a particular PWM scheme each waveform is in out of phase sequence with its fellow carrier waveforms by 180 degree.

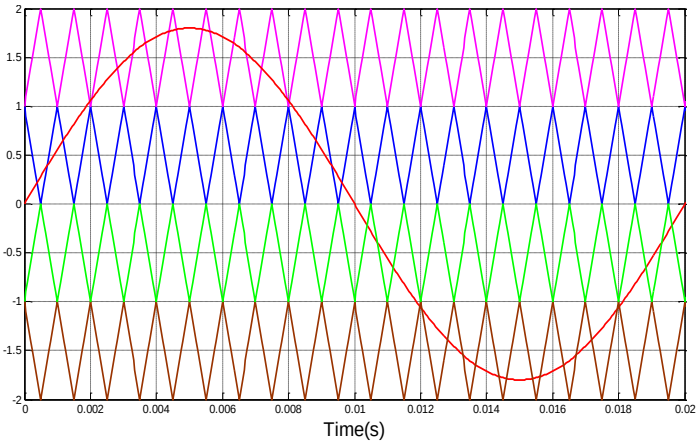

Fig. 4.3: Carrier planning for APODPWM topology

- PS PWM (Phase-shifted pulse width modulation) :- In Fig.4.4 carrier waveform Phase-shifted pulse width (PW) modulation policy.

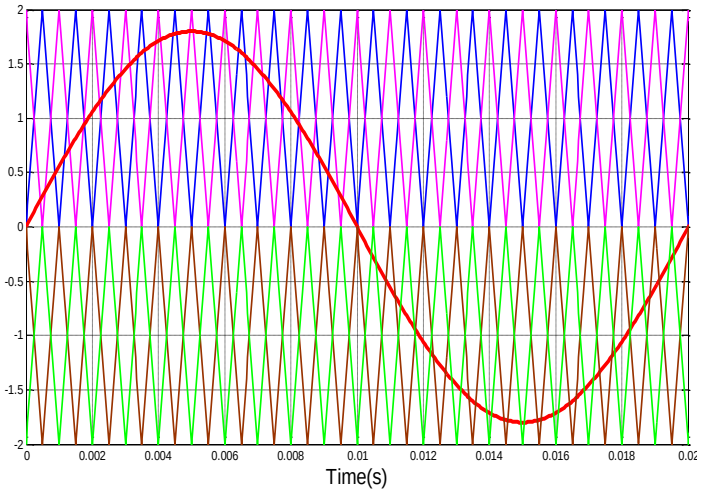

Fig. 4.4: Carrier waveforms planning for topology

V. SIMULATION RESULTS

A MATLAB /Simulink model has been simulated and results are compared simulated

The parameters of the simulated model are selected from the literature

- Frequency of switching signal is 1 KHz
- Resistance = 10 ohms
- Inductance = 10mH
- DC voltage source = 400V

Based on the simulation and model harmonic results are analyzed in FFT window.

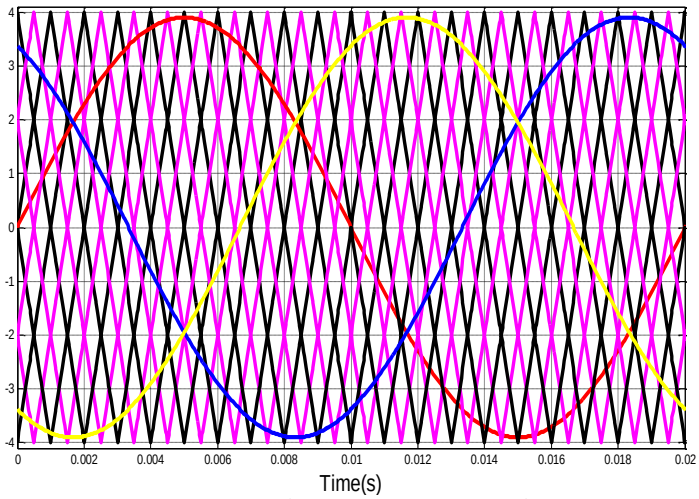

Fig. 5.1 Carrier waveform Modulation Signals of MLI.

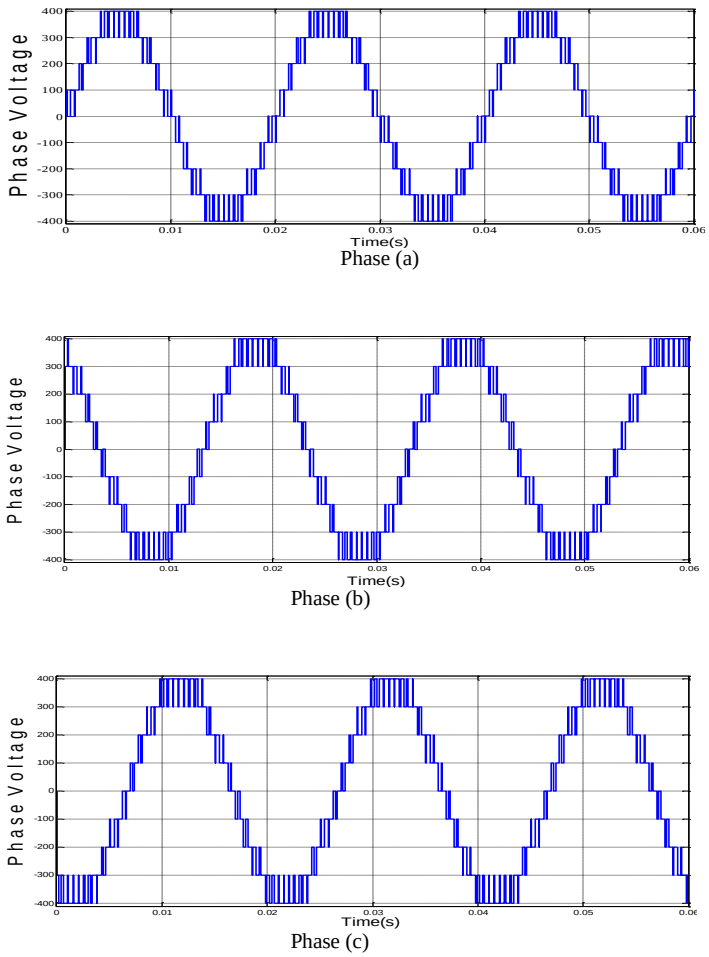

Fig. 5.2 Simulated Phase-shifted pulse width modulation for R-L Load

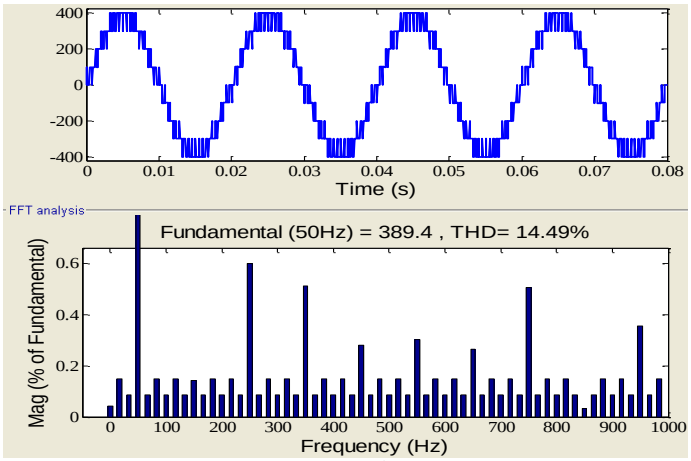

Fig. 5.3: Phase output voltage by Phase-shifted pulse width modulation

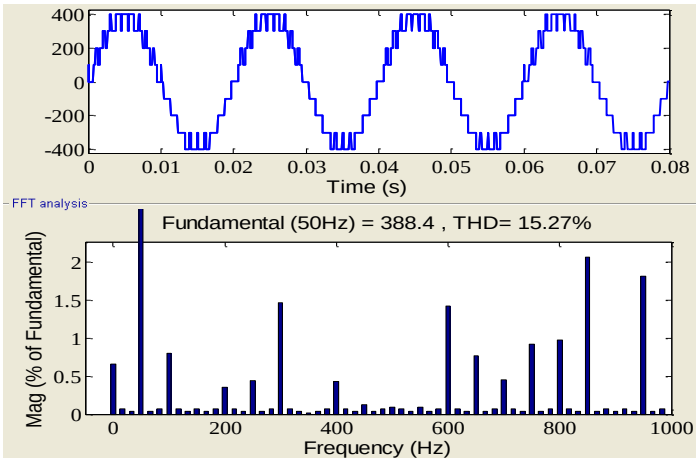

Fig. 5.4: Phase output voltage by Phase disposition pulse width modulation

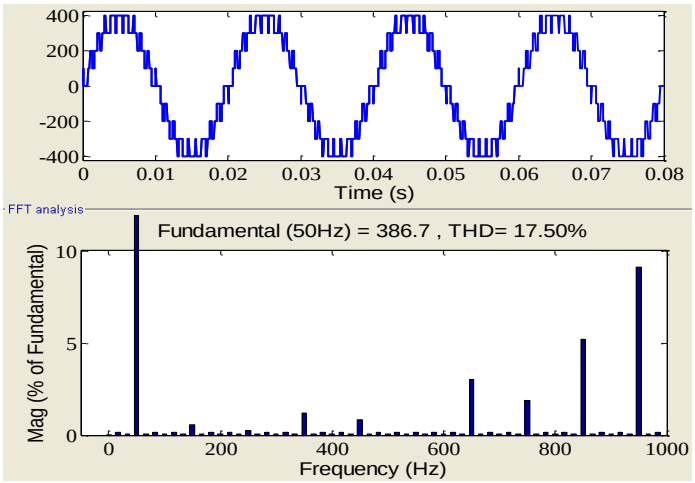

Fig 5.5: Phase output voltage by POD modulation

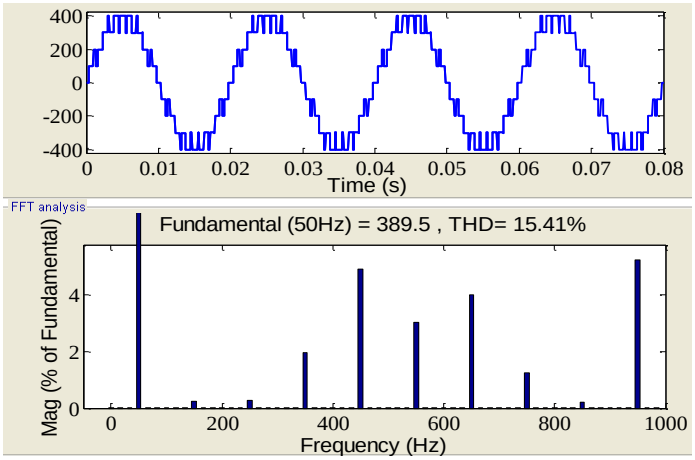

Fig. 5.6 Phase output voltage by APODPWM for R-L load (Ma=0.9, Mf=20).

The number of required components for three-phase 9- level MLI is shown in Table II.

TABLE-II
Comparison of different multilevel (N-LEVEL) inverter topologies

Inverter type	NPC	Flying capacitor	CHB	Proposed
Main switches	6(n-1)	6(n-1)	6(n-1)	3((n-1)+4)
Main diodes	6(n-1)	6(n-1)	6(n-1)	3((n-1)+4)
Clamping diodes	3(n-2)(N-1)	0	0	0
DC bus Capacitor/ Isolated supplies	(n-1)	(n-1)	3(n-1)/2	(n-1)/2
Flying capacitors	0	3(n-1)(n-2)/2	0	0
Total numbers	(N-1)(3N+7)	(N-1)(3N+20)/2	27/2(N-1)	(13N+35)/2

VI. CONCLUSION

This paper introduced a Nine-level inverter topology named as Reverse Voltage methodology is introduced along with various Pulse Width Modulation techniques and reported MLI topology with different Pulse Width Modulation techniques is use to produce a new Nine-level output phase voltage. So the above work of single and three phase Nine-level the total harmonics distortion is reduced in comprision to the other traditional .

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