Performance Analysis of Low Power and High Speed one-bit Full Adder Circuit

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Abstract

Adders are digital circuits that perform addition of numbers in processors and other kinds of computing devices. This paper presents performance comparison of a one-bit full adder circuit in 130nm technology at a temperature of 27 ^{0}C. The circuit is designed and simulated by using various techniques. Performance analysis of the full adder circuit is done in terms of power, delay and power delay product (PDP). All simulations are performing by Mentor Graphics Pyxis schematic EDA tool.

Keywords: GDI technique, Mod-GDI technique, SERF technique, Power dissipation, Delay, PDP

I. INTRODUCTION

Full adder (FA) is the basic combinational digital logic circuit for performing numerous arithmetic operations. The design criterion in any energy efficient full adder circuit involves the transistor count. It is a prominent component in the designing of integrated circuit that performs arithmetic operations. This circuit that executes the addition of three input bit augends (A_i), addend (B_i) and carry input (C_{in}) from the previous adder and the output contain the sum and carry. Figs. 1 and 2 show the block and circuit level diagram of a one-bit FA circuit. Table 1 shows the truth table of a one-bit FA circuit.

Fig (1). Block level diagram

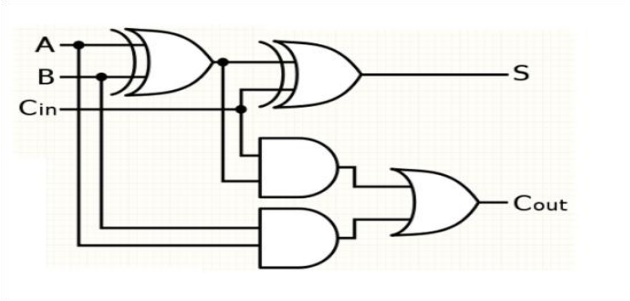

Fig (2). Circuit level diagram

Table 1. Truth table

INPUT			OUTPUT	
A	B	C_{IN}	C_{OUT}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The Characteristic equation is given by:

$$Sum = ABC + AB'C' + A'B'C + A'BC' \quad (1)$$

$$Carry\ out = AB + AC + BC \quad (2)$$

The chip complexity is continuously increasing by virtue of some important issues in VLSI design in terms of power, circuit delay, and power delay product (PDP) [1-2]. The circuit is designed and simulated in 130nm CMOS technology at a temperature of 27 ^{0}C. The designed full

adder circuit is analysed and compared on the basis of performing parameters by using Static energy recovery technique, Gate diffusion input (GDI) technique, and Modified Gate diffusion input (Mod-GDI) technique.

A. Static energy recovery full adder (SERF) design

In this FA SERF circuit, energy is recovered by reuse of charges which causes minimum power dissipation as compared to non recovery logic circuits [3]. Fig. 3 shows a designing of 1- bit full adder using Static energy recovery technique. This logic circuit consists of two XNOR modules and it requires four transistors for its realization. Sum is achieved by XNOR circuit of the 2_{nd} stage and carry out is obtained by multiplexing A and C_{in}. At the output node of the first XNOR circuit. has a load capacitance. Initially, if A and B are equal to 0, then load capacitor starts charging upto the supply voltage V_{DD}. B achieved high voltage level and A low voltage level, therefore, capacitor getting discharged through A. However, few charges are still stored in A. Due to this; A does not charge it fully for high voltage level, so that less energy is consumed. The advantage of this circuit is not providing a direct path to the ground. The charges which are already stored in load capacitor are reused; therefore, this technique is energy efficient [3-5]. However, the main disadvantage is increased in propagation delay in the circuit.

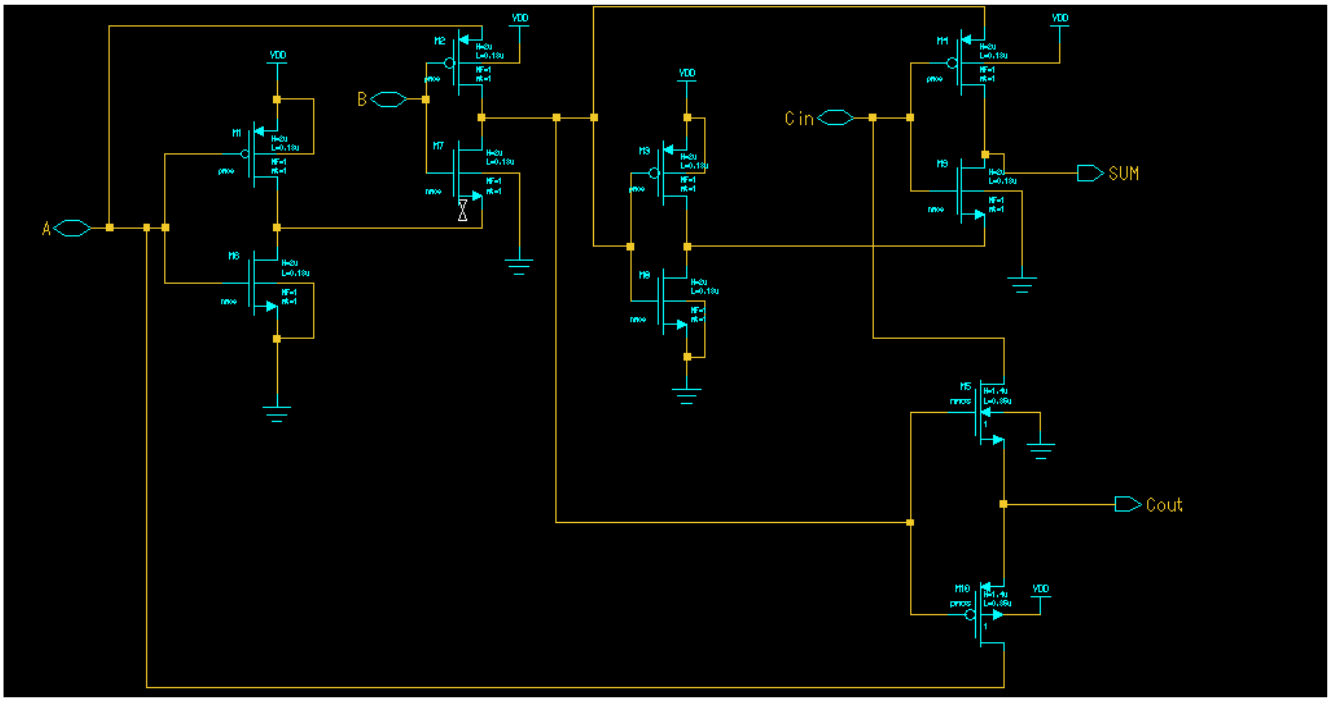

Fig (3). SERF FA Circuit

B.Gate diffusion input (GDI) full adder design circuit

GDI technique [6-10] is used to overcome the drawback of conventional CMOS circuit technique in form of parameters such as delay, power dissipation, number of transistor and area. A basic GDI cell consists of four terminals (G, N, D, and P).

- G - (nMOS & pMOS transistor having common gate input)
- P - (External diffusion node in pMOS transistor)
- N - (External diffusion node in nMOS transistor)
- D - (Both transistor having common node of diffusion)

Fig. 4 presents the circuit diagram of a one-bit full adder by using GDI technique. This technique uses two extra input nodes which makes the circuit more flexible. Circuit designed by using this technique has lesser number of transistors as compared to CMOS technique [8]. Hence, that affects the performance parameters. The main problem associated with this circuit technique lies in the twin-well CMOS process and lack of driving ability is also a major problem in chip realization [10].

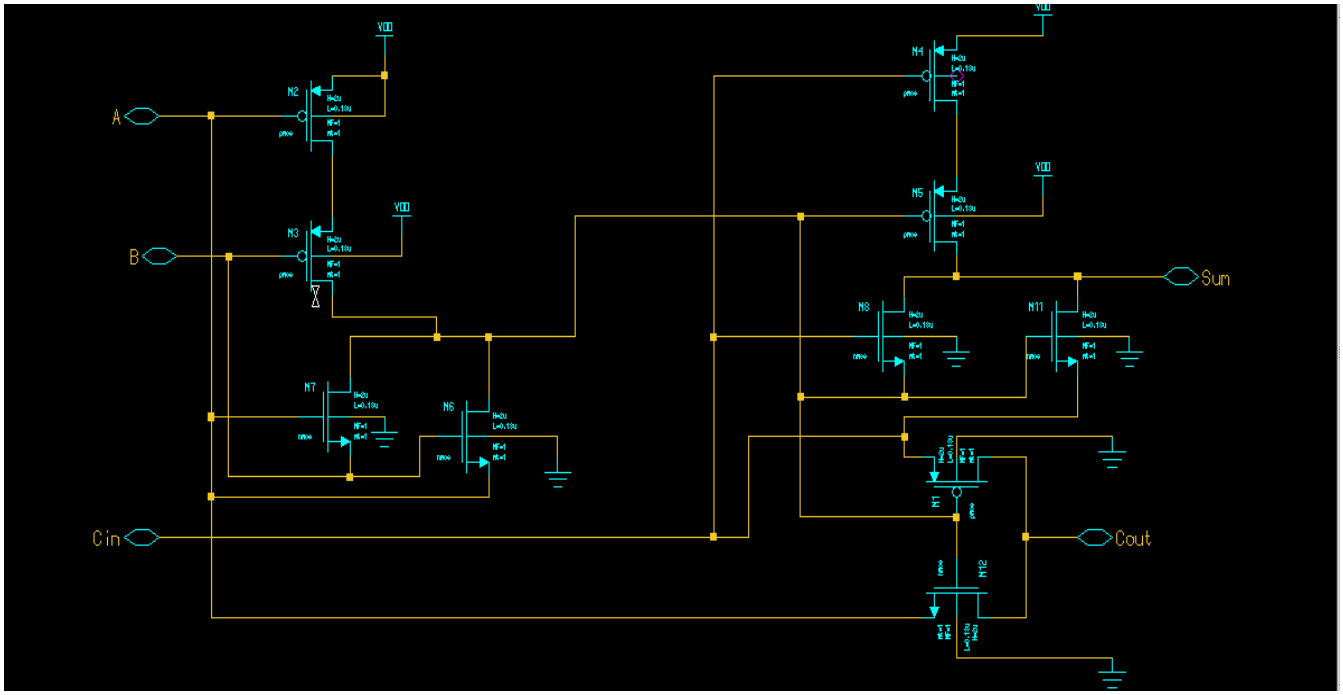

Fig (4). GDI FA Circuit

C. MOD-GDI full adder

This full adder design is implemented by using the XOR/XNOR gate. This technique enhances the performance. Fig. 5 presents the circuit diagram of a one-bit full adder by using this technique. This technique provides an overcome to Gate diffusion technique in terms of circuit delay, power and PDP [11]. This technique provides full swing and by virtue of that the average power reduces.

The basic Modified GDI [11] cell consisting:

- A low voltage terminal S_p is connecting to V_{DD}(higher voltage constant).
- A high voltage terminal S_N configuration is to be connecting to the ground.

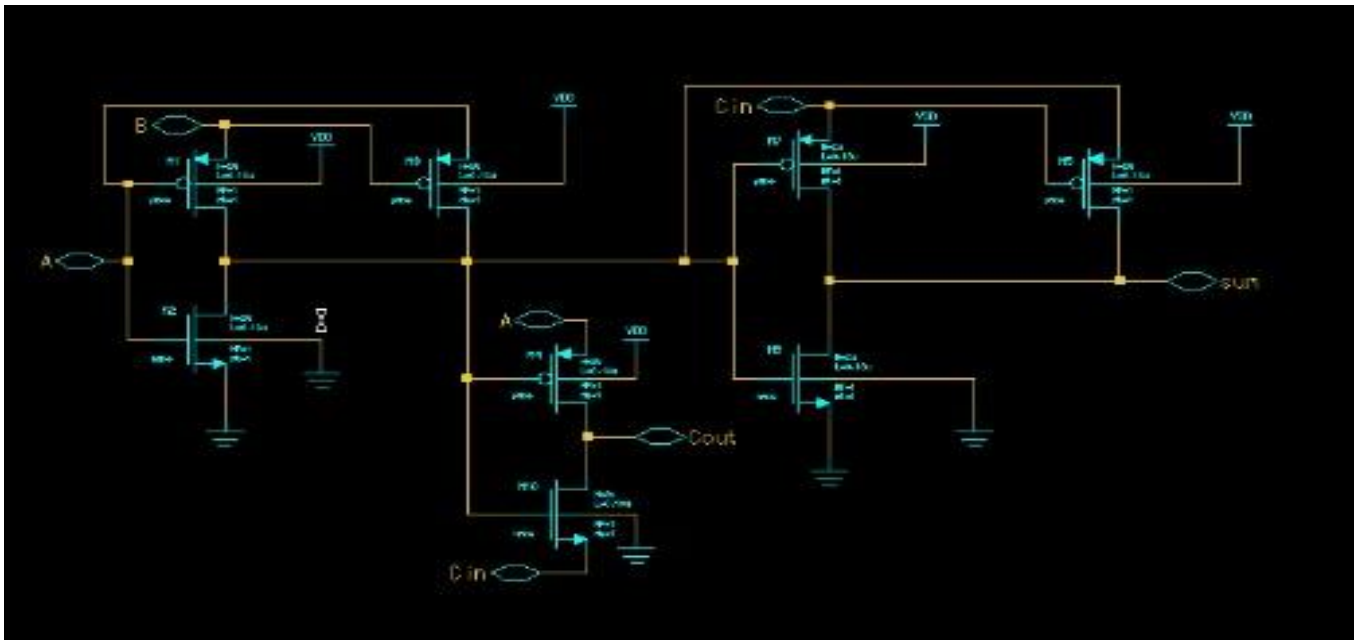

Fig (5). MOD-GDI FA Circuit

II. RESULTS AND OBSERVATIONS

One- bit FA circuit is designed with the help of Static energy recovery, Gate diffusion input (GDI), and Modified-GDI techniques. 130 nm CMOS technology is used for the designing and simulations of these circuits at a temperature of 27 ^{0}C. The designed circuit is analysed and compared on the basis of power, propagation delay, and power delay product (PDP) by using Mentor Graphics Pyxis schematic EDA tool. Tables 2-6 show the performance of a 1-bit FA circuit designed by using various techniques at different supply voltages. Figs. 6-8 show the output waveform of a one-bit full adder circuit designed by using Static energy recovery, GDI, and Mod GDI techniques respectively. It is observed from Tables 2-6 that the full adder circuit designed by using Mod-GDI technique provides the better performance as compared to SERF and GDI full adders.

Table 2. Performance comparison at V_{DD} = 1V

Parameters	SERF full adder	GDI Full adder	MOD-GDI Full adder
Power dissipation	29.346 nw	2.579 nw	10.023 pw
Delay	15.558 ns	12.675 ns	15.954 ns
PDP(10^{-17} Ws)	45.659	3.269	0.159

Table 3. Performance comparison at V_{DD} = 2V

Parameters	SERF full adder	GDI Full adder	MOD-GDI Full adder
Power dissipation	2.338 uW	10.324 nw	39.996 pw
Delay	19.812 ns	13.683 ns	9.505 ns
PDP(10^{-17} Ws)	47.017	14.275	0.380

Table 4. Performance comparison at V_{DD} = 3V

Parameters	SERF full adder	GDI Full adder	MOD-GDI Full adder
Power dissipation	71.554 uw	32.040 nw	89.995 pw
Delay	31.998 ns	16.182 ns	12.801 ns
PDP(10^{-17} Ws)	228.959	52.441	1.152

Table 5. Performance comparison at V_{DD} = 4V

Table.5 output at V_{DD}= 4 V			
Parameters	**SERF full adder**	**GDI Full adder**	**MOD-GDI Full adder**
Power dissipation	**560.796 uw**	**366.368 nw**	**159.989 pw**
Delay	**19.981 ns**	**16.168 ns**	**14.079 ns**
PDP(10^{-17} Ws)	**1120.523**	**592.373**	**22.525**

Table 6. Performance comparison at V_{DD} = 5V

Parameters	SERF full adder	GDI Full adder	MOD-GDI Full adder
Power dissipation	1.886 mw	776.380 nw	244.670 pw
Delay	31.583 ns	29.454 ns	15.959 ns
PDP(10^{-17} Ws)	5956.572	2286.819	39.0471

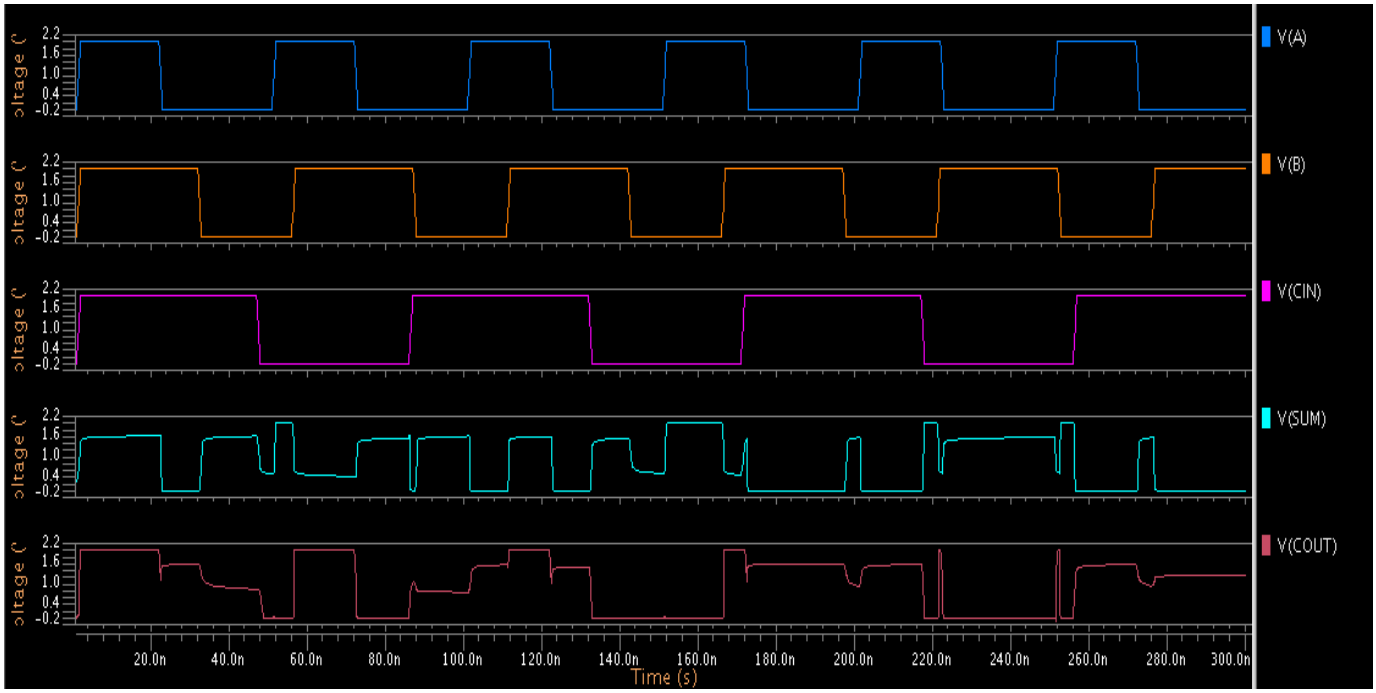

Fig (6). Waveform of a one-bit SERF FA circuit

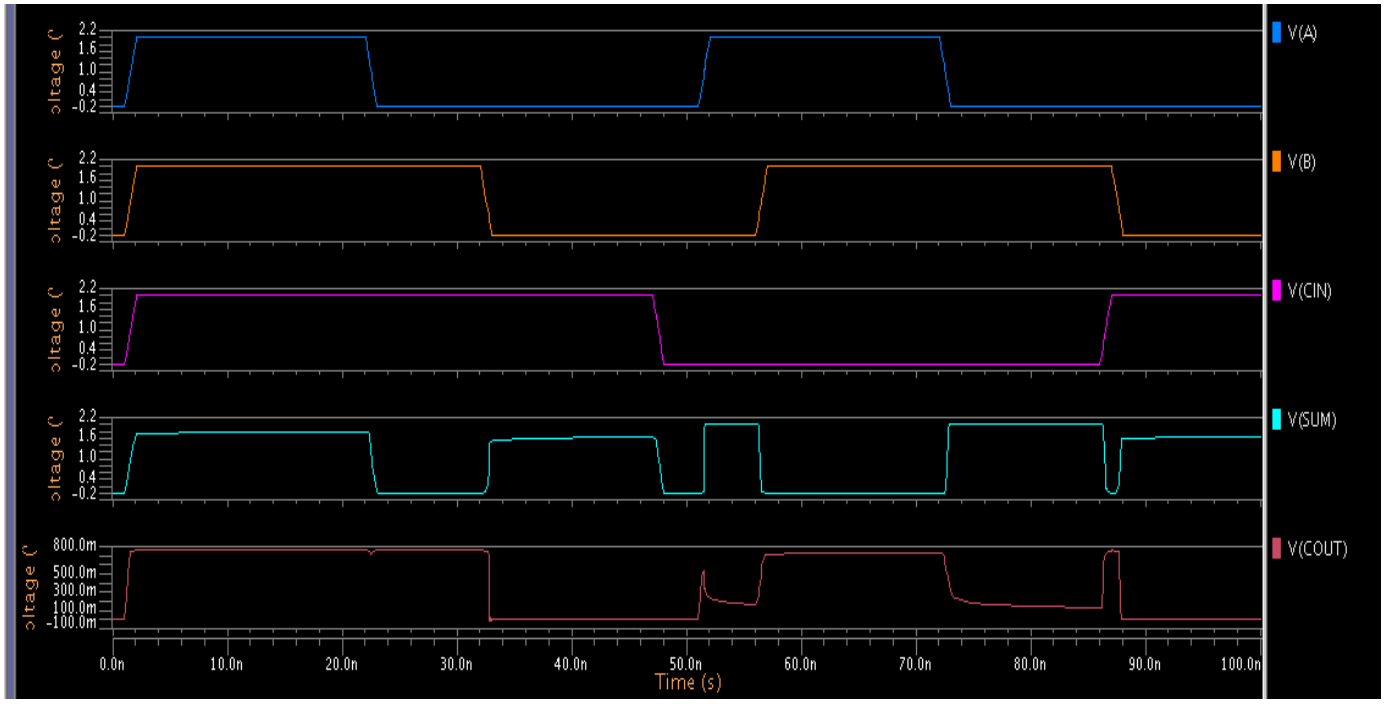

Fig (7). Waveform of a one-bit GDI FA circuit

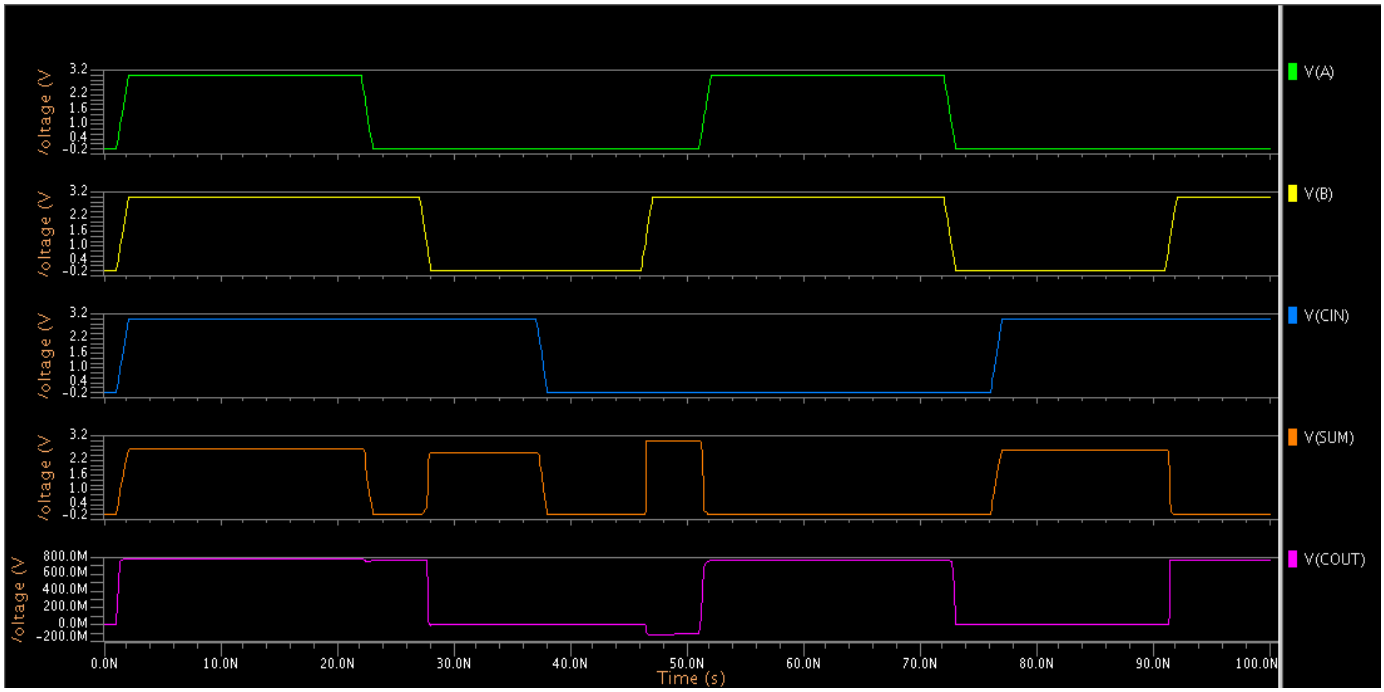

Fig (8). Waveform of a one-bit Mod-GDI FA circuit

III. Conclusion

Mod-GDI full adder circuit provides better performance in forms of lesser power consumption, lesser delay, and lesser power-delay product (PDP) in comparison to SERF and GDI FA circuits. Mod-GDI circuit technique can be used for designing the full adder to achieve low power and high speed in digital circuits.

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