Design and Performance Analysis of Compressors using Different Logic Styles

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***Abstract* – Compressors are the combinational circuits that are used in multipliers to lessen the operands at the time of adding partial products terms. In this paper, design and performance comparison of compressors using different logics are carried out using performance parameters like delay, total power dissipation and power delay product (PDP) in 130nm technology. A 3:2 compressor is designed by using different logic styles such as conventional CMOS, 16T and 14T logic styles. The most energy efficient compressor obtained on comparison is further extended to design a 4:2 compressor. All simulations are performed using Mentor Graphics Pyxis schematic tool.**

Keywords– Compressors, Delay, Total Power Dissipation, CMOS, 4:2 Compressor.

I. INTRODUCTION

The field of digital signal processing is quite vast, is used to implement convoluted operations such as filtering, Discrete Fourier Transform (DFT), convolution [1], and Fast Fourier Transform [2]. In all these aforesaid, signal processing operations, the multiplier is the main building block. Multipliers [3] are used to perform multiplication which is a cumbersome process and therefore it consumes a lot of processing time and power. The whole task of multiplication consists of three steps [4], [5]. These are: Generating the partial products, reduction of partial products, and finally carry propagation addition. Among all these steps, reduction of partial products is carried out by compressors. This process consumes much processing time and power and therefore, it is a challenge to design a compressor that consumes relatively low power and have less delay. Compressors are the combinational circuits that are used in multipliers to lessen the operands while adding partial products terms [6], [7]. Typical x:y compressor accepts x equally weighted input bits and provides y output bits where $y<2^x$.

Literature in the last few years gives various studies explaining various techniques and technology used in designing compressors. Since then, compressors have gone tremendous improvement in terms of propagation delay and power dissipation. Traditionally, CMOS compressors were designed by utilizing XOR-XNOR gates which were composed of 28 transistors [8], [9]. These compressors were reliable and simpler. However, these compressors have large transistors count, therefore issues such as greater power dissipation [10], slow switching speed, area consideration, noise immunity and larger delay in the output have been investigated. In order to improve the performance of 28T CMOS compressor, a modification has been brought and the 16T compressor has been developed. A 16T compressor requires only 16 transistors and therefore has advantages over traditional CMOS compressor such area reduction, low power dissipation and delay [11]. To further enhance the performance of the compressor, 14T compressors were designed to further reduce the delay and power dissipation.

This paper is arranged into 5 sections: Section I discussed the role of multipliers and need of a compressor. Section II enumerates an overview of pre-existing compressors based on 28T conventional CMOS compressor, 16T, 14T. Section III presents performance analysis and the simulation result of all compressors aided with performance metric table and graph. The performance parameter includes propagation delay, total power dissipation, and power delay product. In comparison, the compressor with better performance is used to design a4:2 compressor and discussed in Section IV. Finally, interferences and conclusion are described in Section V.

II. OVERVIEW

Compressors are generally designed by employing XOR gates and multiplexers (MUX). Thus, the performance of a compressor is greatly influenced by the performance of these basic building blocks. Therefore, to enhance the performance, XOR gate is replaced by XOR-XNOR gate. Fig. 1 shows the basic

architecture of a 3:2 compressor. A 3:2 compressor is the elementary compressor which consists of one XOR-XNOR gate and two MUX. It takes three inputs namely M1, M2, and Cin; and it generates two outputs SUM and Carries. Some of the common 3:2 compressors are designed by using conventional CMOS logic, 16 transistors (16T) and 14 transistors (14T).

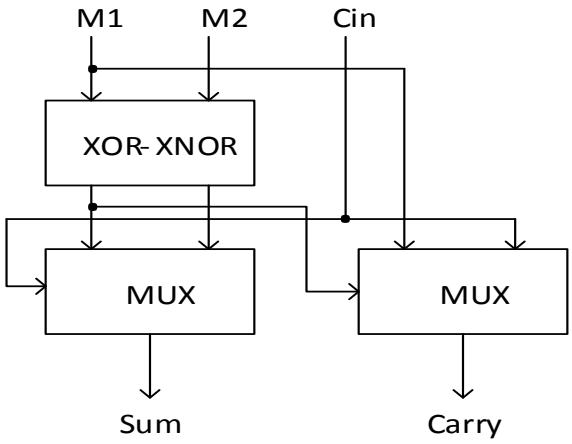

Fig. 1 Architecture of a 3:2 compressor

A. CONVENTIONAL CMOS 3:2 COMPRESSOR

A 3:2 conventional CMOS compressor [6, 7] utilizes 28 transistors. Large PMOS transistors count in the pull-up network results in high input capacitances which eventually led to delays in the circuit and high power consumption. However, this compressor has large noise margins and therefore suitable for low voltage operations. Fig. 2 shows the schematic diagram of a 3:2 conventional CMOS compressor.

B. 3:2 COMPRESSOR USING 16T

A 3:2 compressor using 16T [8] consists of XOR-XNOR gates and passes transistors and transmission gates. The XOR and XNOR modules do not produce output for full swing and therefore the transistors connected to this module are turned on or off slowly. There are in total 16 transistors which have relatively less delay and consume less power. Fig. 3 shows the schematic diagram of a 3:2 compressor using 16T.

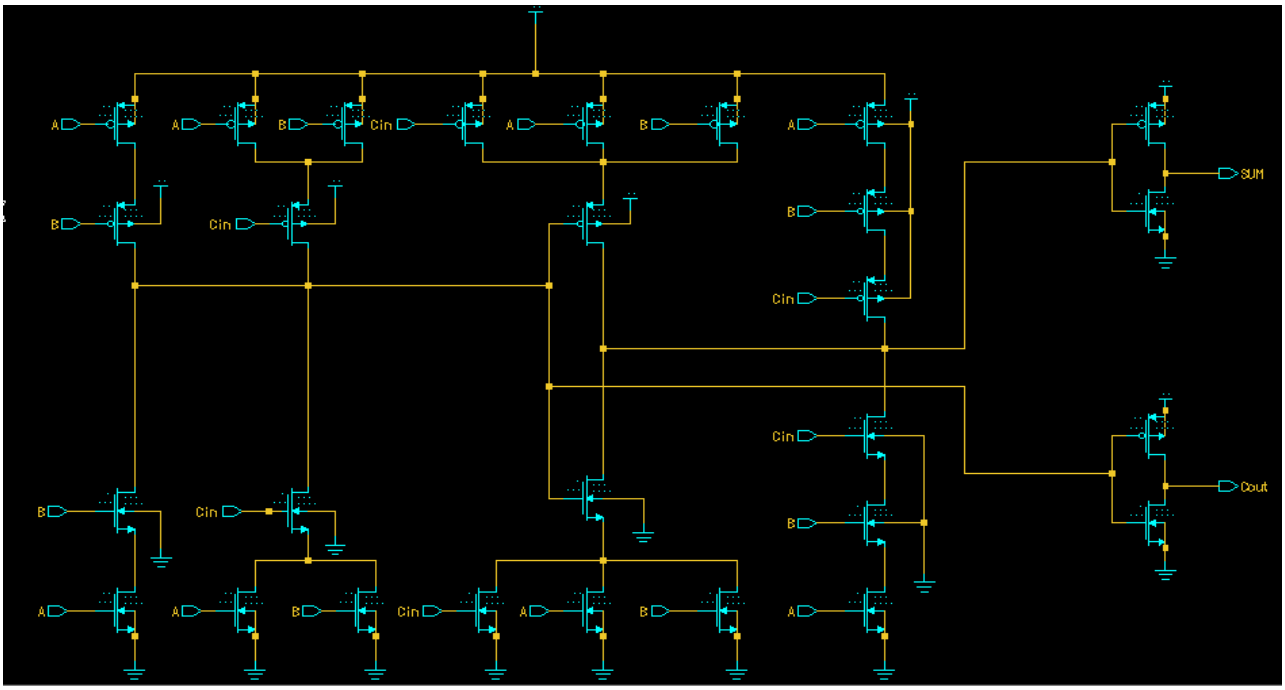

Fig. 2 Conventional CMOS 3:2 compressor

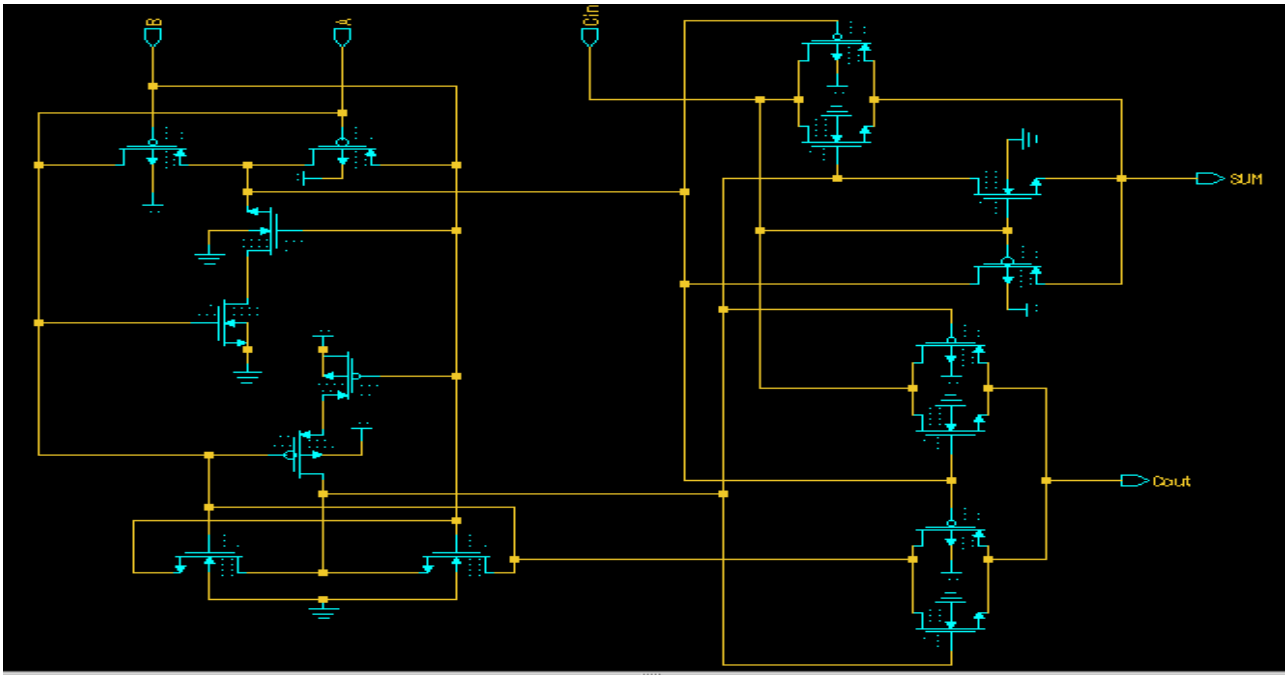

Fig. 3 3:2 Compressor using 16T

C. 3:2 COMPRESSOR USING 14T

3:2 compressor using 14T [9] comprises of XOR gate, an inverter, and the multiplexer. It has 4 XOR gates which are inverted in the next stage to produce XNOR gate. 14T compressors are generally used in high-performance multipliers since it has less delay and low power consumption. Fig. 4 shows the schematic representation of a 3:2 compressor using 14 transistors.

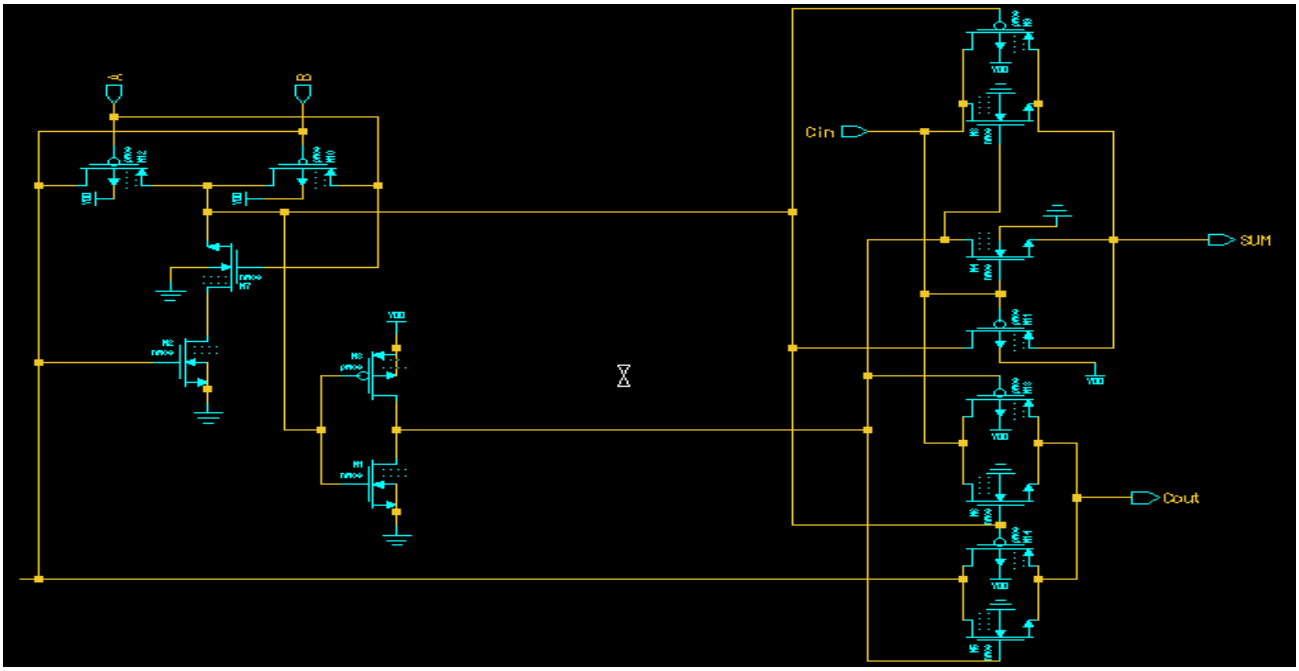

Fig. 4 3:2 Compressor using 14T

III. PERFORMANCE ANALYSIS AND SIMULATION RESULT

Mentor Graphics Pyxis schematic tool has been employed for performing the simulation of all the compressor circuits. The channel length is 0.13µm for both NMOS and PMOS whereas channel widths for NMOS and PMOS transistors are 1.56µm and 3.9µm respectively. All compressor circuits are simulated in 130nm technology with supply voltages of 1V, 2V, 3V, and 4V. Performance analyses of a 3:2 compressor using different logics in terms of propagation delay, total power dissipation, and power delay product are tabulated in tables 1-4. It can be clearly inferred from Tables 1-4 that with the increase in the total transistor count, performance parameter such as total power dissipation and delay of a compressor are increased. When supply voltage was varied from 1V to 4V, propagation delay, total power dissipation and power delay product also increased.

TABLE 1. 3:2 Compressor Assessment using various Performance metric with V_{DD} = 1V

Logic Styles	Transistor Count	Total Power Dissipation (nW)	Delay (nS)	Power Delay Product (Ws x 10^{-18})
Conventional CMOS	28	3.511	6.309	22.155
16T	16	2.059	1.808	3.723
14T	14	1.387	3.229	4.481

TABLE 2. 3:2 Compressor Assessment using various Performance metric with V_{DD} = 2V

Logic Styles	Transistor Count	Total Power Dissipation (nW)	Delay (nS)	Power Delay Product (Ws x 10^{-18})
Conventional CMOS	28	11.977	6.150	73.660
16T	16	7.780	1.704	13.259
14T	14	5.288	1.745	9.231

TABLE 3. 3:2 Compressor Assessment using various Performance metric with V_{DD} = 3V

Logic Styles	Transistor Count	Total Power Dissipation (nW)	Delay (nS)	Power Delay Product (Ws x 10^{-18})
Conventional CMOS	28	31.2612	6.1387	191.9056
16T	16	22.863	1.697	38.798
14T	14	15.658	1.755	27.485

TABLE 4. 3:2 Compressor Assessment using various Performance metric with V_{DD} = 4V

Logic Styles	Transistor Count	Total Power Dissipation (nW)	Delay (nS)	Power Delay Product (Ws x 10^{-18})
Conventional CMOS	28	76.1874	6.1328	467.2431
16T	16	62.106	1.700	105.608
14T	14	42.868	1.759	75.394

Fig. 5-7 shows the input-output waveform of a 3:2 compressor by using different logic styles. Among the presented 3:2 compressors, compressor using 14T showed best results in terms f performance. Hence a 4:2 compressor is designed by using 14T.

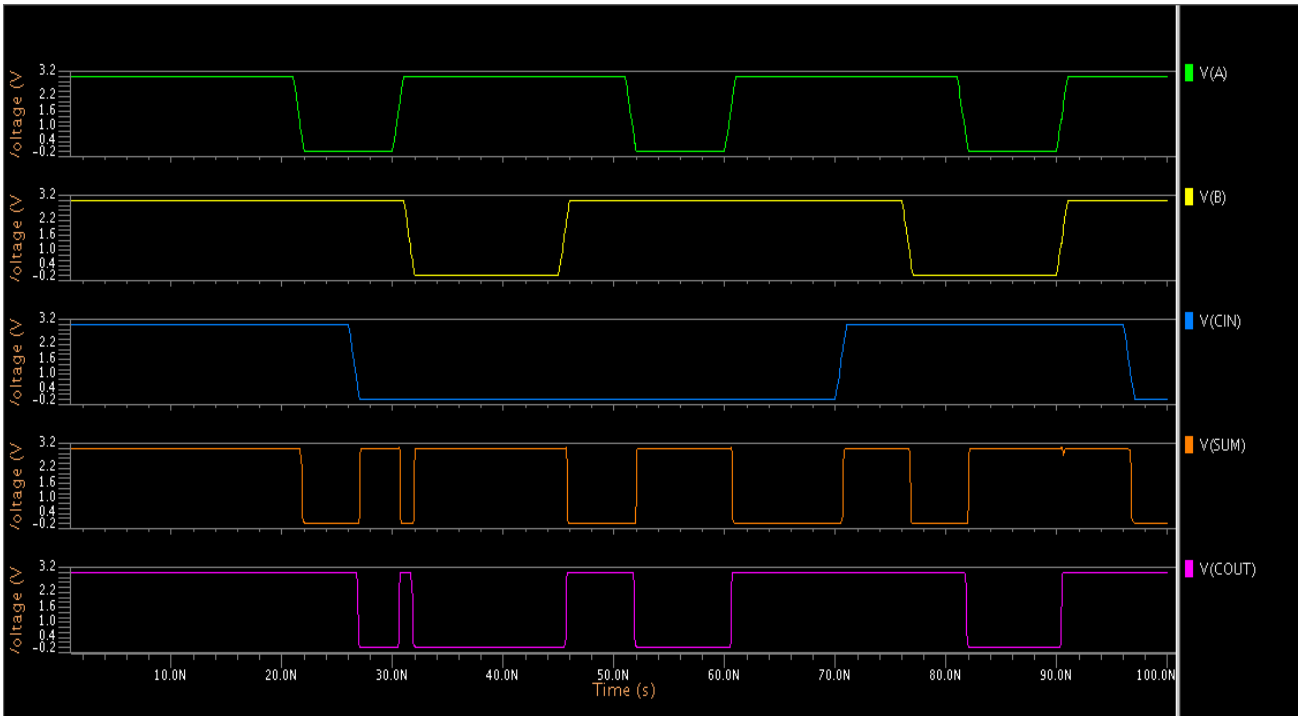

Fig. 5 Input-Output waveform of a conventional 3:2 CMOS compressor.

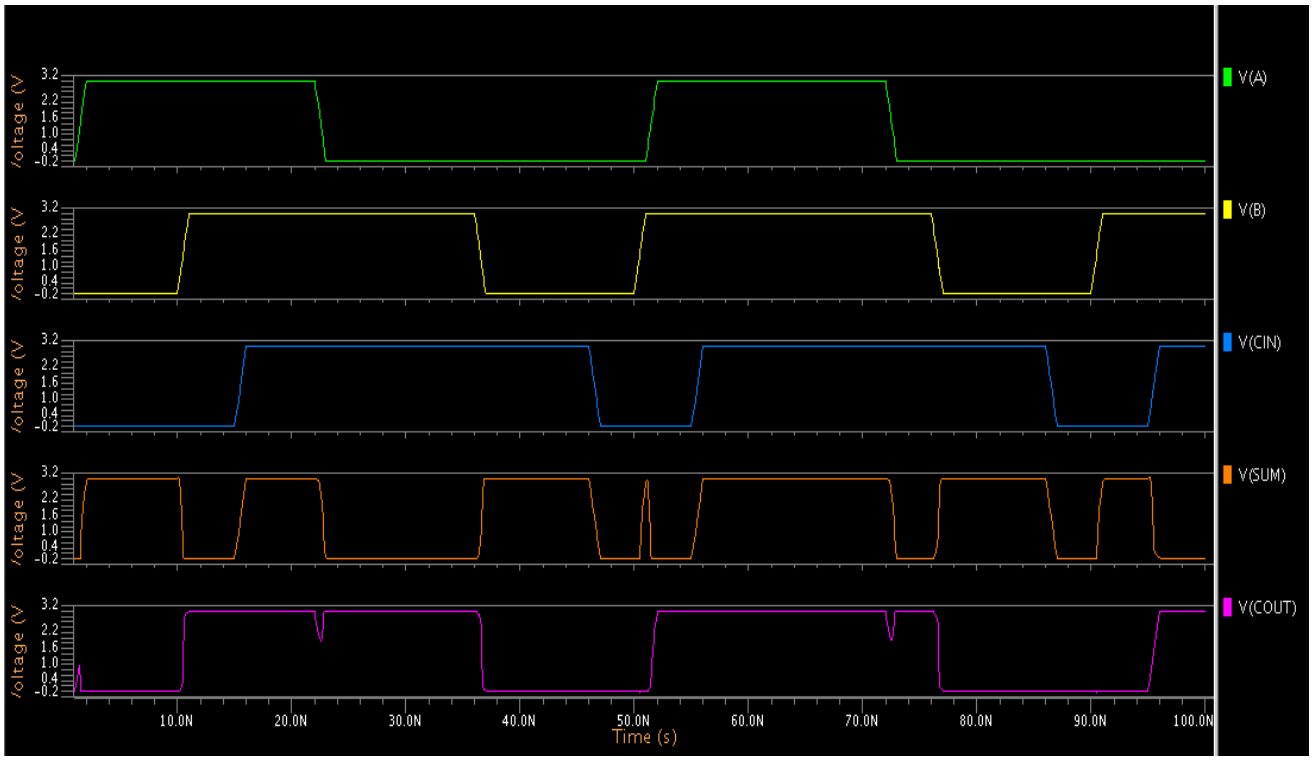

Fig. 6. Input-Output waveform of a 16T 3:2 compressor.

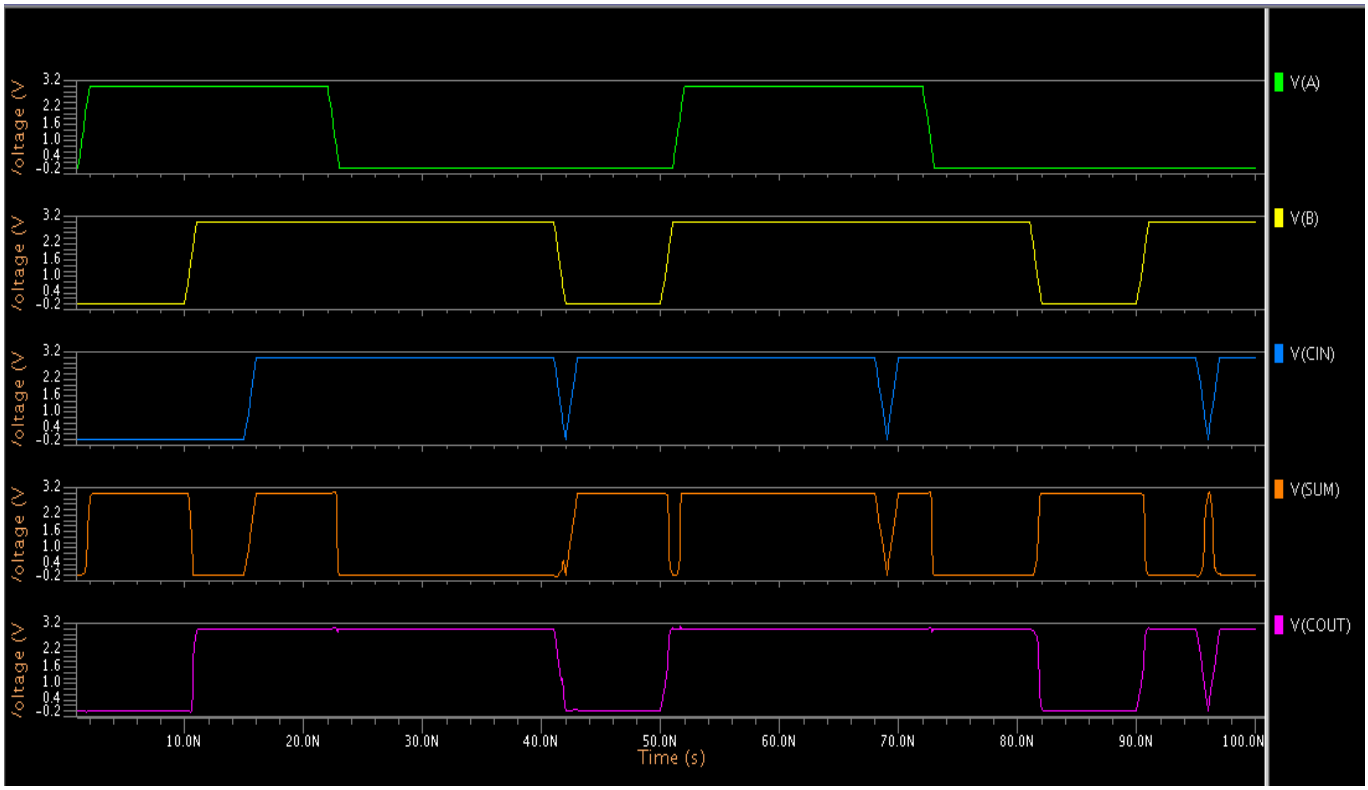

Fig.7 Input-Output waveform of a 14T 3:2 compressor.

IV. 4:2 COMPRESSOR

A 4:2 compressor compresses 4 partial products into 2 partial products. Fig. 9 shows a 4:2 compressor design by using two 3:2 compressors.

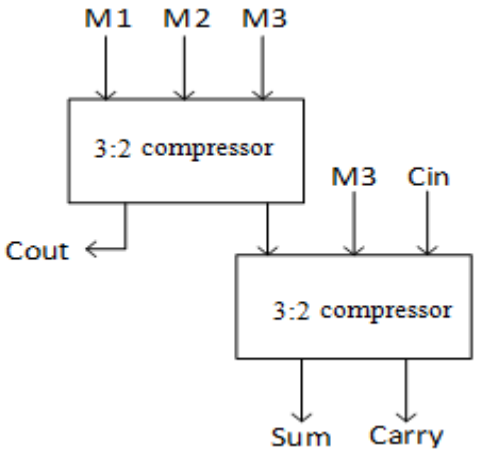

Fig. 8 4:2 compressor design using two 3:2 compressors

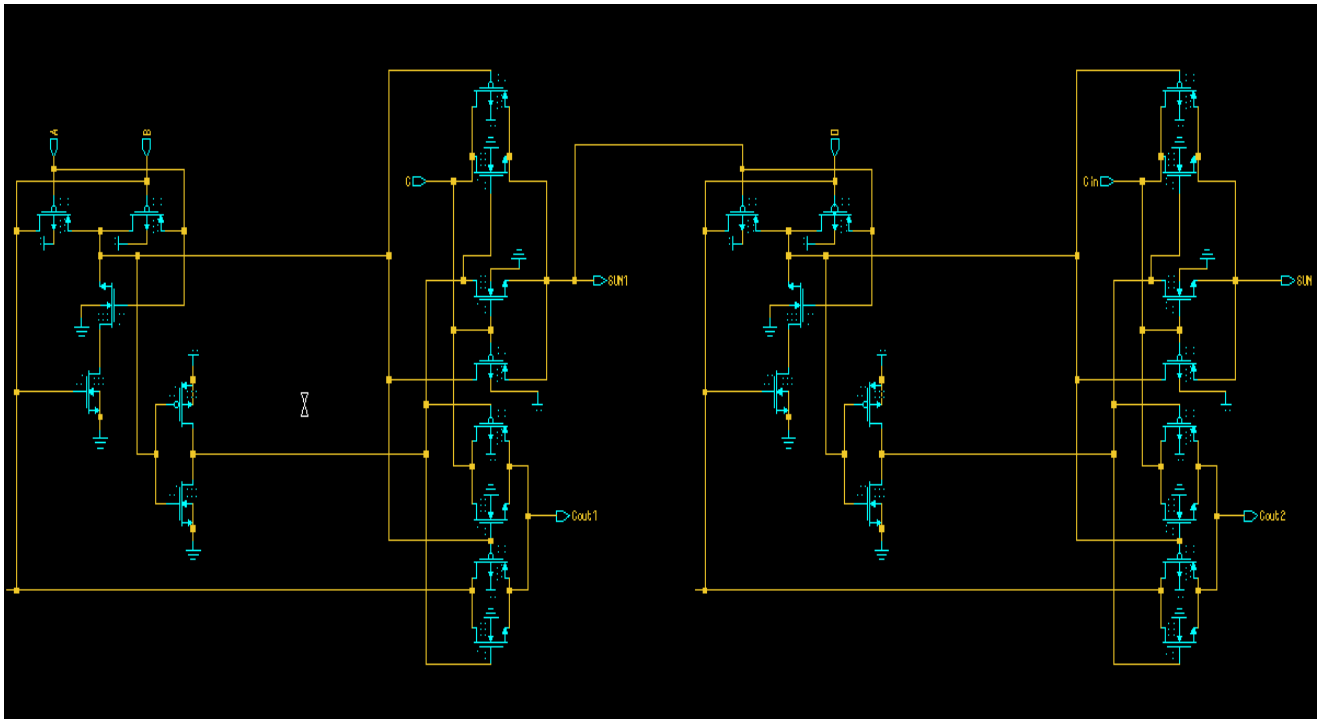

Fig. 9 . Schematic diagram of 4:2 compressor

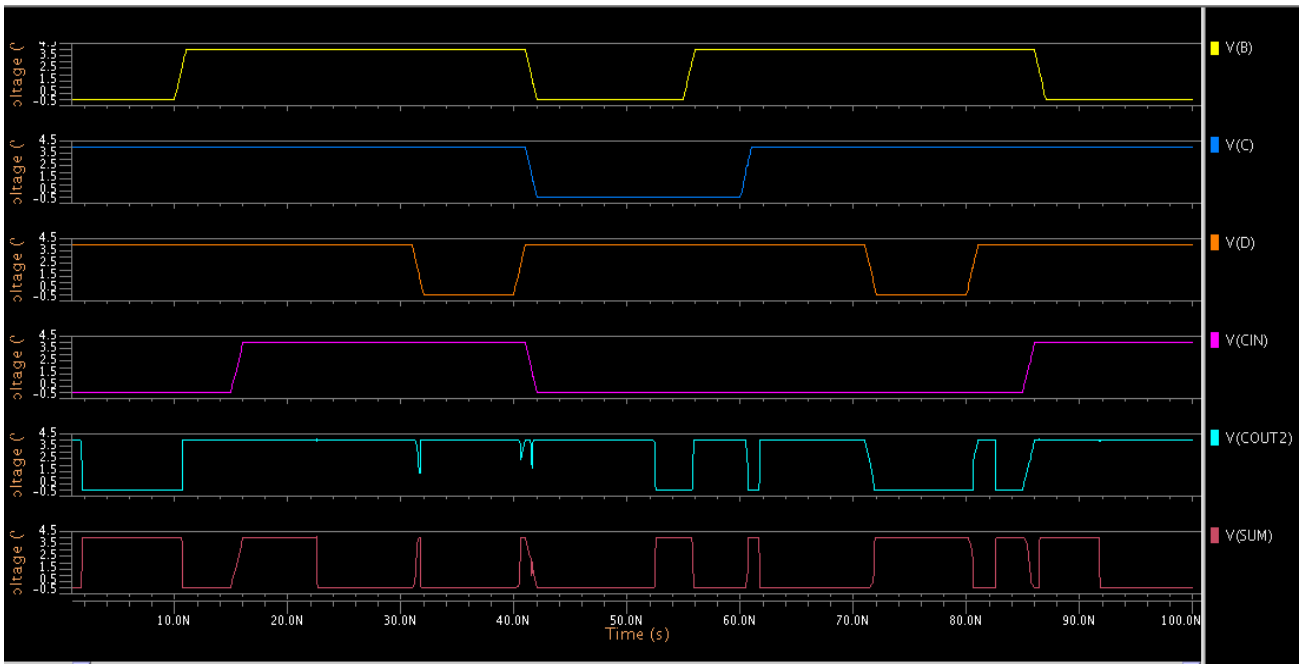

Fig. 10. Input and output waveform of a 14T 4:2 compressor

The power dissipation, delay, and power-delay product are calculated for input voltage 1V to 4V and obtained results are mentioned in Table 5.

TABLE 5. 4:2 Compressor Assessment using various Performance metric.

V_{DD} (in V)	Total Power Dissipation (nW)	Delay (nS)	Power Delay Product (Ws x 10^{-18})
1	2.775	2.917	8.0958
2	10.576	2.733	28.902
3	31.317	2.416	75.665
4	85.736	2.706	232.070

The schematic diagram and input and output waveform of a 14T 4:2 compressor are shown in Fig. 9 and Fig. 10 respectively

V. CONCLUSION

Energy efficient compressors are required in order to have low power and low delay in the multiplier. Moreover, as multiplier operation increases, higher compressor circuit is needed to have faster output. The basic compressor circuit is a 3:2 compressor which is designed by using different logic styles such as conventional CMOS, 16T and 14T. 3:2 compressor designed by using 14T showed superior performance in terms of power delay product. Further, it can be used in designing higher order energy efficient compressors.

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