Design and Analysis of Low Power Digital Circuits

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Abstract

Scaling down feature of CMOS technology makes it enormously popular and demanding to get the high performance with less power dissipation. The power dissipation is directly proportional to the square of the supply voltage. When the supply voltage is scaled down, it results in reduction in power dissipation but it influences the performance in terms of speed of the device. To compensate the delay, the threshold voltage is reduced. But leakage current increases due to the lower threshold voltage. To solve the problem of subthreshold leakage current, MTCMOS (Multi threshold CMOS) and Stack techniques and MTCMOS plus Stack are used. All simulations are performed by using Mentor Graphics Pyxis schematic tool in 130nm technology.

Keywords*: MTCMOS, Stack, power dissipation,*
leakage current.

I. Introduction

In recent years, power dissipation is a big issue for the VLSI designers. According to the Moore's law, number of transistors increases in approx. every two years. The result is increase in integration density with the increase in power dissipation. Low power digital circuits are useful in battery operated portable devices such as mobile computing, notebook processor and communication devices. So managing power dissipation in digital circuit is essential for VLSI engineers. Power dissipation mainly consists of dynamic and static power [1]. Dynamic power component is switching power plus short circuit power. Dynamic power is consumed when the circuit is in active mode. Total power can be expressed as:

$$P_{total} = P_{dynamic} + P_{short\,\text{circuit}} + P_{leakage} \quad \text{..... (1)}$$

$$P_{dynamic} = fC_L V_{dd}^2 \quad \text{..... (2)}$$

Where term f is clock frequency

When input and output are switching, power is drawn from the circuit in the form of heat. For example we take an inverter circuit at the input side transition of logic 1 to 0. The load capacitance is charged from the constant power supply from 0 to V_{dd}. During charging of load capacitor, half of the power is stored in the load capacitor and other half of the power is wasted in the form of heat. At the output side when the transition of logic is from 0 to 1. During the discharging half, the power which is stored in the load capacitor is discharged.

$$P_{avg} = n.\alpha.f.\tfrac{1}{2} C_{avg} V_{dd}^2 \quad \text{..... (3)}$$

Where n is number of gates in a circuit, α is the switching activity [2].

Short circuit current flows in the direct path from supply voltage (V_{dd}) to GND. The magnitude of the current depends upon the small amount of finite interval of time, when the transition of input voltage is from high to low logic and low to high logic. In a CMOS inverter circuit, when the input logic is at 0, then PMOS transistor is conducting and when the input voltage rises and reaches above the threshold voltage of NMOS transistor then NMOS transistor also conducts. At the same time both the transistors are concurrently conducting for a short period of time during switching, so the short circuit current flows through it. Short circuit power dissipation can be expressed as [3]:

$$P_{short-circuit} = \tfrac{1}{12}.K.\tau.F_{clk}(V_{dd} - 2V_t)^3 \quad \text{.... (4)}$$

Where τ is a rise time and fall time, k is the transistor gain

Static power dissipation is due to the leakage current flow from supply voltage to ground in CMOS circuits in the absence of switching activity. The leakage current increases with the scaling down in technology and increasing the integration density of transistors in a chip.

$$P_{static} = V_{dd} I_{leakage}$$

Subthreshold leakage current in CMOS circuits is a leakage current between the source to drain region due to the diffusion of the carrier concentration. This current flows in transistor because of weak inversion region that means gate to source voltage is less than the threshold voltage. The leakage current is exponentially influenced by the gate voltage. The quantity of weak inversion current is same as the switching power dissipation in short channel MOS transistors. The leakage current flows when the circuit is in inactive mode or standby mode. Subthreshold leakage current is the prime component of power dissipation with the scaling down in technology generations.

1. MTCMOS (Multi threshold CMOS) Technique

Power dissipation reduces by reducing the subthreshold leakage current by using the MTCMOS technique. In MTCMOS technique, CMOS circuit consists of two different transistors (NMOS & PMOS) with different threshold voltages: low and high threshold voltage. Standard CMOS circuit has low threshold and sleep transistor has high threshold voltage[4]. In active mode operation, sleep input is at logic 0 and sleep bar input is at logic 1. So, both the transistor is turned on and CMOS transistor derives with low power dissipation.

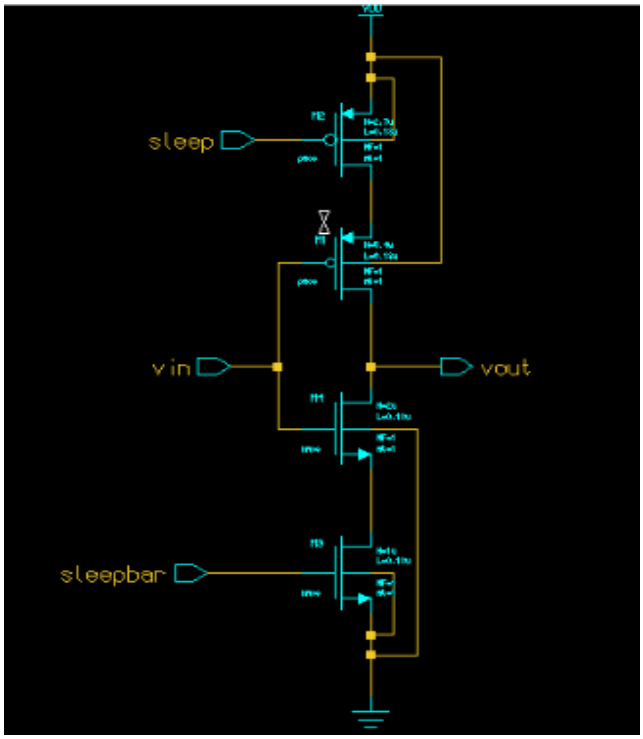

Fig. 1. INVERTER using MTCMOS

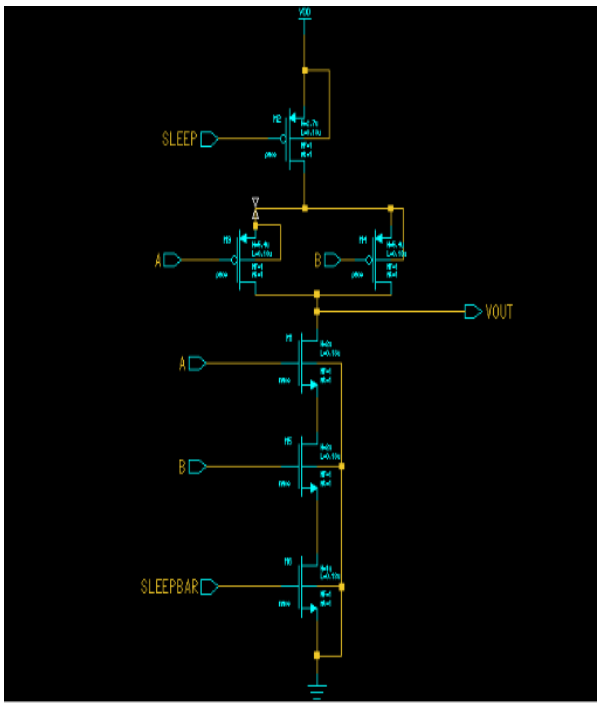

Fig. 2. NAND using MTCMOS

In the standby mode both sleep transistors are turned off and leakage current which is due to the use of low thresholdvoltage MOS transistors, is reduced. So the power dissipation also reduces. Low threshold voltage transistor is used to design the standard CMOS logic circuit and high GND from the logic circuit in the standby mode[5-7]. A CMOS inverter, CMOS two input NAND circuit, and CMOS two input NOR circuit has been implemented by using MTCMOS technique which is shown in Fig. 1, 2 and 3 respectively.

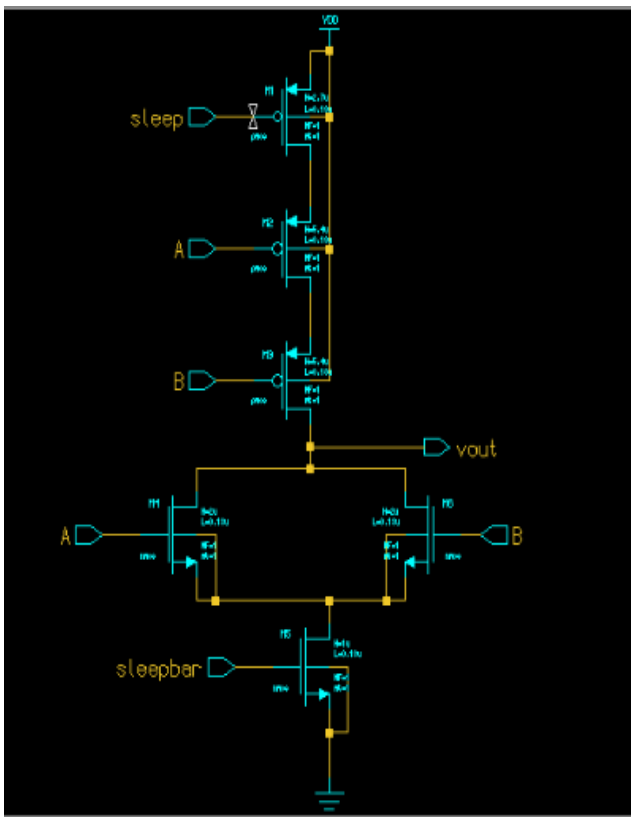

Fig. 3. NOR using MTCMOS

2. STACK TECHNIQUE

When two or more off transistors are connected in series during standby mode, then the leakage current reduces. The leakage current of these off transistors reduces by stacking technique [5]. The NAND gate has naturally affected by stacking effect, leakage current in single off transistor is more as compared to two or more off-transistors. During the standby mode, leakage current reduces by applying appropriate input vector in stack technique. If only single NMOS transistor is turned off, source voltage of this NMOS transistor becomes virtually zero. Thus, self-reverse biasing effect is negligible. If two or more NMOS off transistors are connected in series then source voltage become higher than zero, so leakage current is minimized by the negative effect of self reverse biasing effect[6-7]. The logic gates that are implemented by using stack technique are shown in Fig 4, 5 and 6 respectively.

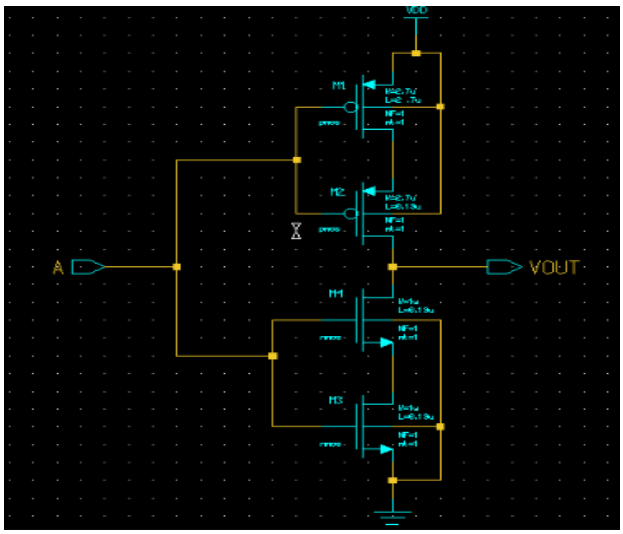

Fig. 4. Stack Inverter circuit

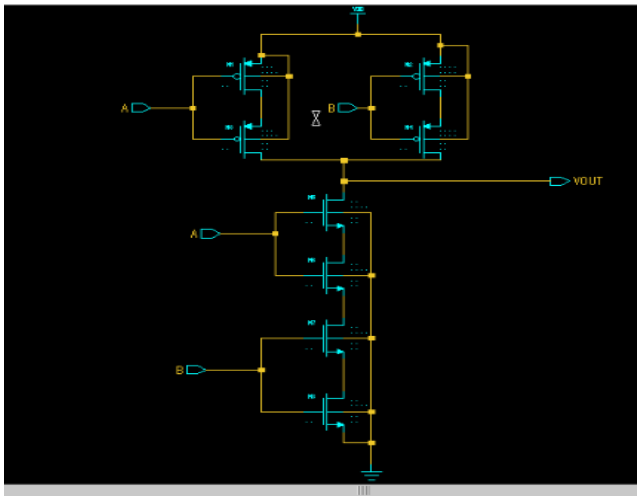

Fig. 5. Stack NAND circuit

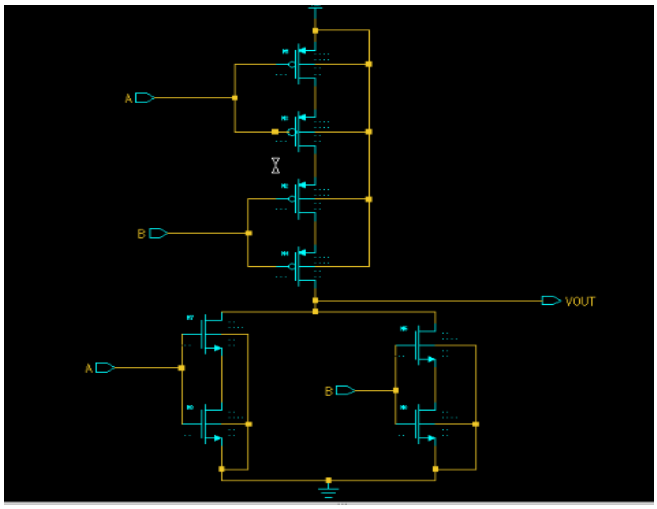

Fig. 6. Stack NOR circuit

3. MTCMOS PLUS STACK TECHNIQUE

Inverter, NAND, NOR gate are implemented with the help of MTCMOS and Stack technique. This is shown in Fig 7, 8 and 9 respectively.

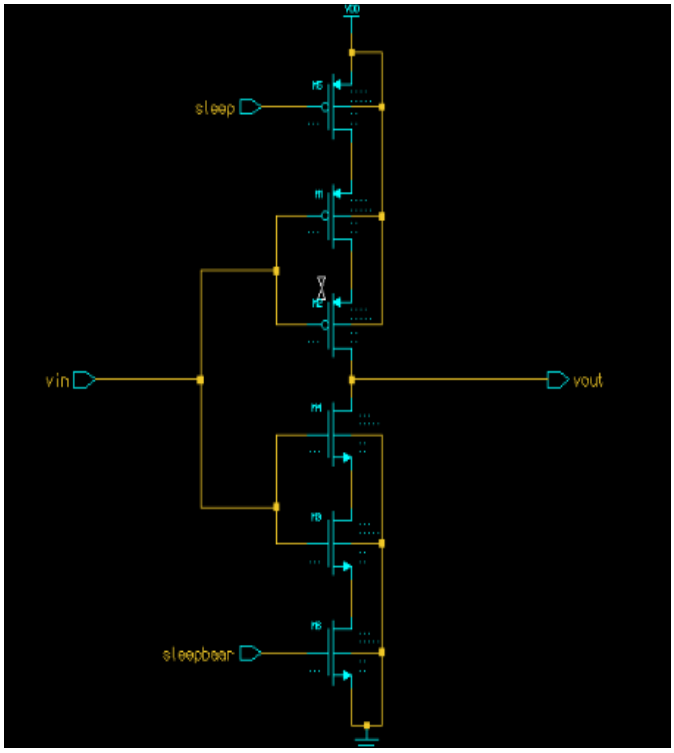

Fig. 7. Inverter circuit using MTCMOS plus Stack technique

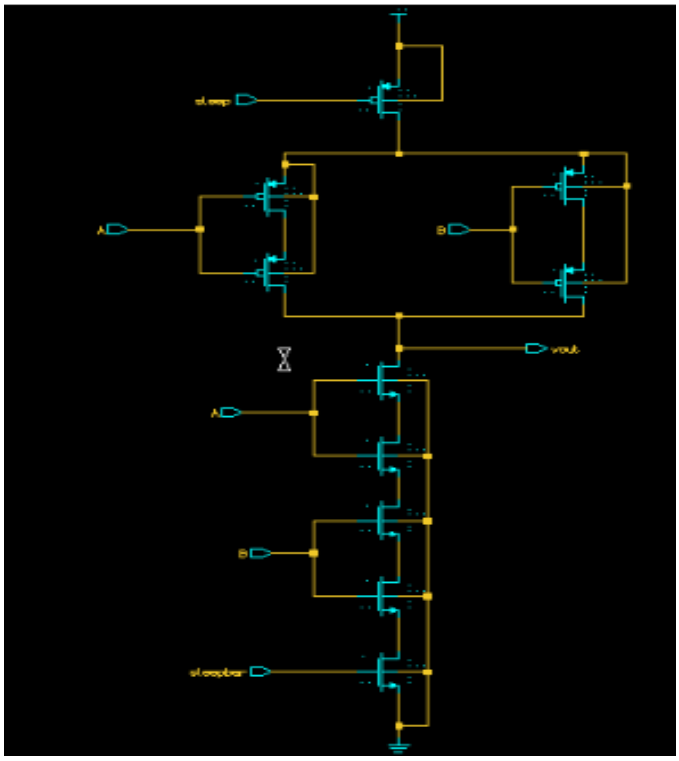

Fig. 8. NAND circuit using MTCMOS plus Stack technique

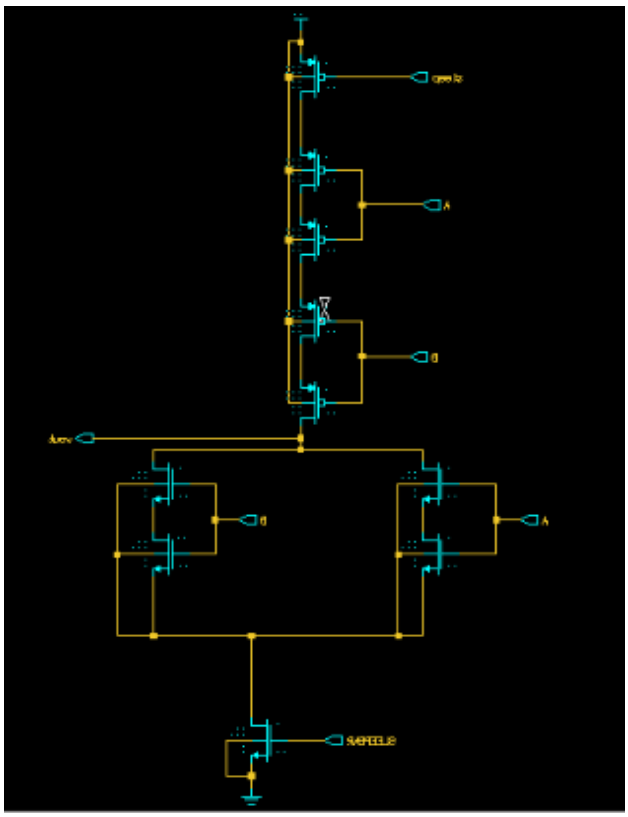

Fig. 9. NOR circuit using MTCMOS plus Stack technique

4. SIMULATION RESULTS

Figs. 10-15 show the input-output waveform of different logic circuits by using stack and MTCMOS plus stack techniques. Tables I-IV show the power dissipation of logic circuits by using CMOS, MTCMOS, Stack, and MTCMOS plus stack techniques.

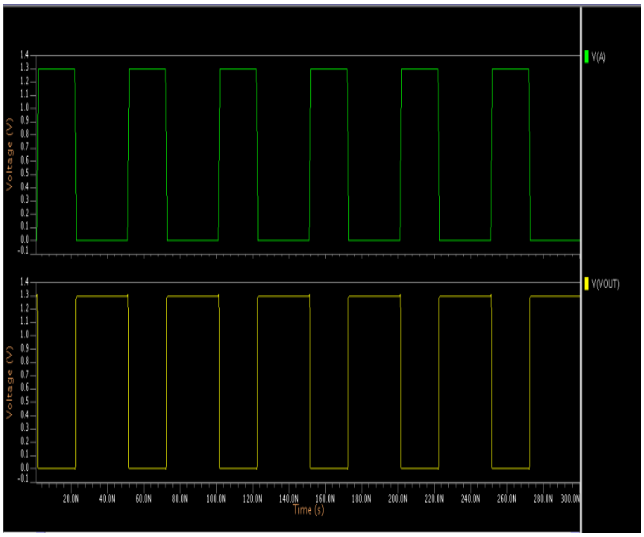

Fig. 10. Input-Output waveforms of Inverter circuit using Stack technique

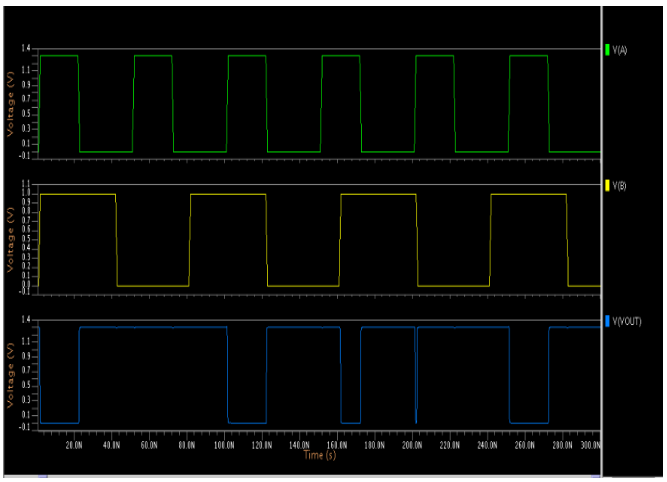

Fig. 11. Input-Output waveforms of NAND circuit using stack technique

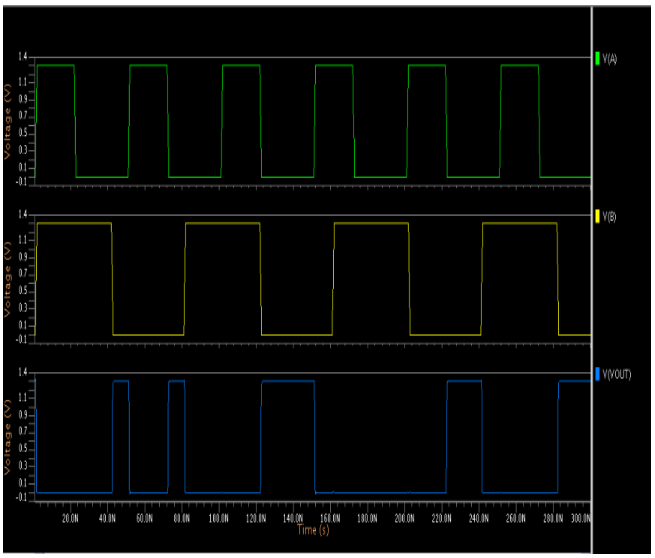

Fig. 12. Input-Output waveforms of NOR circuit using stack technique

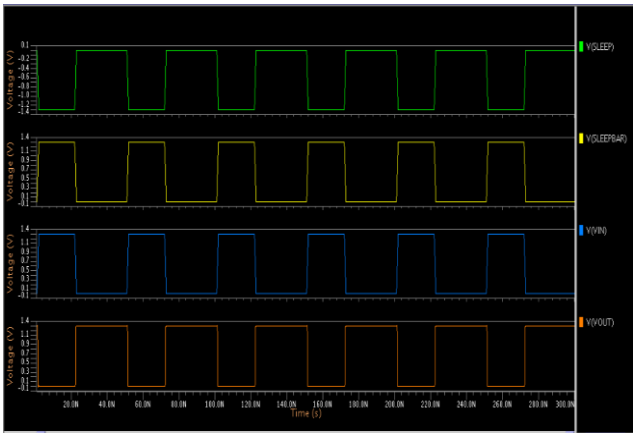

Fig. 13. Input-Output waveforms of Inverter circuit using MTCMOS plus Stack technique

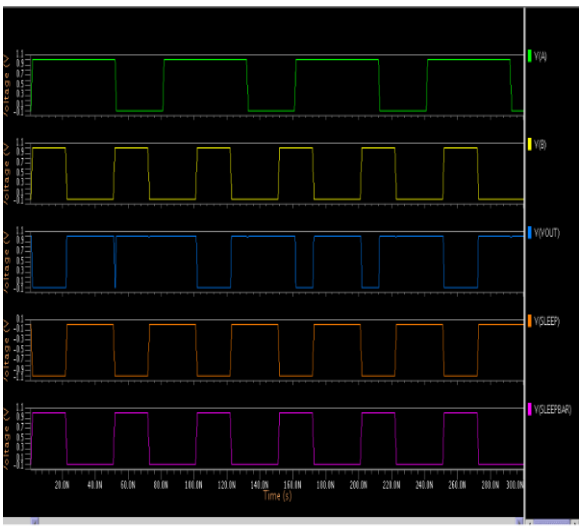

Fig. 14. Input-Output waveforms of NAND circuit using MTCMOS plus Stack technique

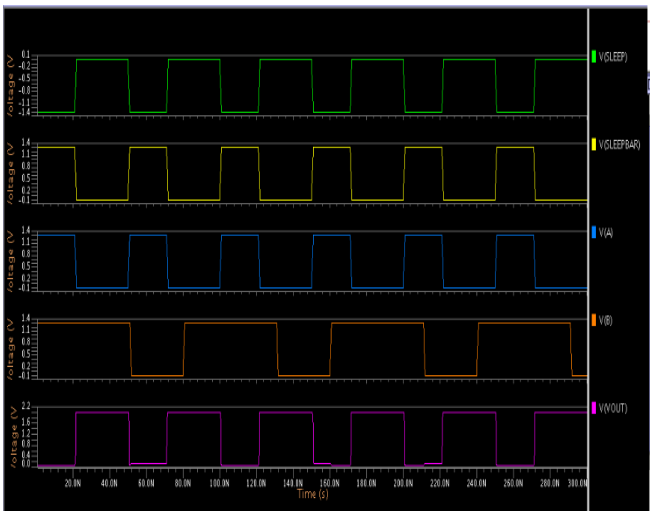

Fig. 15. Input-Output waveforms of NOR circuit using MTCMOS plus Stack technique

TABLE I. POWER DISSIPATION OF LOGIC GATES USING CONVENTIONAL CMOS

Supply voltage(volt)	**Power dissipation(pW)**		
	Inverter	*NAND*	*NOR*
0.5	267.5308	103.2014	535.0604
1	774.1977	236.4169	1548.4
1.3	1238.9	327.0542	2477.8

TABLE II. POWER DISSIPATION OF LOGIC GATES USING MTCMOS

Supply voltage (volt)	**Power dissipation(pW)**		
	Inverter	*NAND*	*NOR*
0.5	102.1113	63.2109	135.6386
1	233.4988	137.8392	290.3088
1.3	322.6583	186.1875	388.5120

TABLE III. POWER DISSIPATION OF LOGIC GATES USING STACK

Supply voltage (volt)	**Power dissipation(pW)**		
	Inverter	*NAND*	*NOR*
0.5	99.4745	44.9671	198.9489
1	224.3936	95.5184	448.7873
1.3	308.5320	127.5942	617.0640

TABLE IV. POWER DISSIPATION OF LOGIC GATES USING MTCMOS PLUS STACK

Supply Voltage(volt)	**Power dissipation(pW)**		
	Inverter	*NAND*	*NOR*
0.5	62.0091	35.2621	98.1574
1	134.1440	74.1721	207.9353
1.3	180.6984	98.6543	277.2136

V. CONCLUSION

Among the circuit techniques such as CMOS, MTCMOS, Stack, and MTCMOS plus stack, the logic circuit designed by using MTCMOS plus Stack proved to be more efficient in terms of power dissipation. In Inverter circuit MTCMOS dissipates 26% power, Stack dissipates 24.9% power MTCMOS plus stack dissipates 14.58% power as compared to CMOS, In NAND circuit MTCMOS dissipates 56.92% power, Stack dissipates 39.01% power MTCMOS plus stack dissipates 30.16% power as compared to CMOS and In NOR circuit MTCMOS dissipates 15.67% power, Stack dissipates 24.90% power MTCMOS plus stack dissipates 11.187% power as compared to CMOS. Hence MTCMOS plus stack technique can be used for effective reduction of power dissipation in different logic circuits.

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