power and small offset is proposed in [9] to reduce the mismatch caused by the conventional system.

CONVENTIONAL SYSTEM

PMOS transistors are used at the input of the preamplifier and latch stage of the comparator. The conventional arrangement let us establish the peerless delay for pre-amplification and keep out abundance power usage. The comparator gives a lateral input Vcm range in f_{clk}=500micro Hertz. CMOS amplifiers were used as passive comparator, despite they undergo very high power consumption. In two-stage dynamic comparators the kick back noise is enhanced by fading the capacitive path. A special controller for the comparator and PMOS latch with PMOS preamplifier are used to achieve low power and high speed. It works at high input common-mode voltages close to V_{DD}. The pre-amplification delay can be set to its flawless value to have better speed and power.A PMOS latch is used in the latch which is activated with a predetermined delay during evaluation phase (tamp). At the reset phase, the clk, clkb1, clkb2 hold a logic "1" to discharge output voltages of both preamplifier and latch to GND.
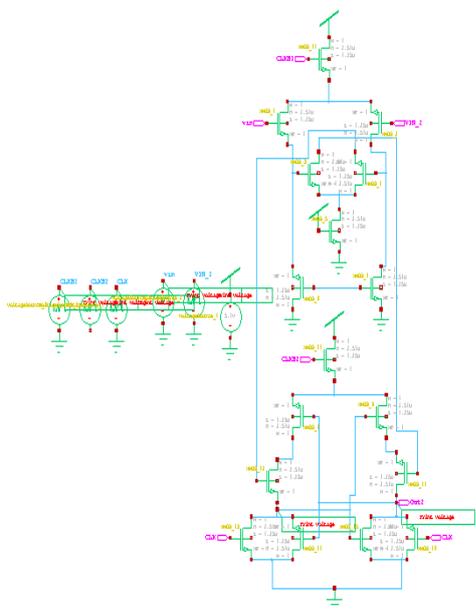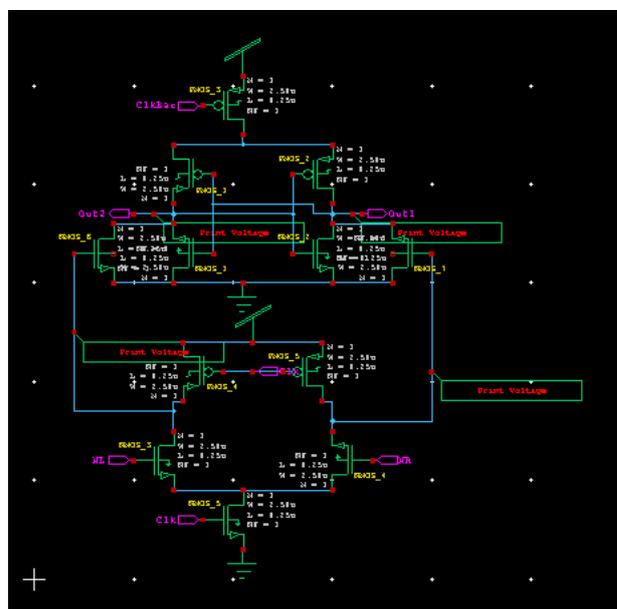

Fig.1 Prevailing dynamic comparator

At the evaluation, first the clk and clkb1 are toggled to logic "0" to start pre-amplification. During this phase, the cross coupled circuit increases differential voltage (V_{id1} = [$V_{01}+-V_{01}-1$]) slowly and reduces the common mode voltage (V_{cm1}=0.5*[$V_{01}+V_{01}-$]). Finally clkb2 is toggled to logic "0" to activate. The latch and clkb1 is changed to logic "1" to turn off the current source. The inverter is designed carefully to adjust the delay. The delay of the evaluation phase is long enough to attain minimum required pre-amplification gain for a given speed and latch offset elimination. Transition of clkb1 to "1" limits the power consumption of the preamplifier. The

delay time from beginning of stage 1 to stage 2 is controllable and can be tuned to its optimum value. A low power small area delay line based controller is designed to make the comparator robust against PVT variations. The cross-coupled circuit is used to reduce the input common-mode voltage of the PMOS latch which increases the speed.

PROPOSED SYSTEM

Fig [2] demonstrates the proposed dynamic double tail comparator. For low voltage applications, double tail structure has better performance when compared with other architectures. In [1] power changes significantly, due to current variations in the first stage (pre-amplification) is pushing towards this structure. Adding transistors in parallel to the circuit, results in lowering the offset and delay. The load in first stage is a parallely connected dynamic latch, which is used to increase the voltage difference. Due to cascade connection delay will be more when compared to parallel. The latch of the first stage start regenerating depends on the input difference voltage thus provides a large voltage difference. This is sensed at second stage latch regeneration output voltage.

Fig.2 *Intended dynamic double tail comparator*

It consumes less power when compared to prevailing comparator and the delay is diminished. The idea of this structure is based on a separate input and cross coupled latch. This latch enables fast operation. The notion of the comparator is to abate its power consumption and to boost the latch regeneration speed. Based on this intent, in cross coupled manner two control transistors are added to the first stage. The operation of the intended comparator, during reset phase (CLK=0, NMOS_5 and PMOS_3 are off, avoiding static power), PMOS_4 and NMOS_3 pulls both, fn and fp nodes to VDD. Intermediate stage transistors, NMOS_6and NMOS_7,

reset both latch outputs to ground. During decision-making phase (CLK=VDD, NMOS_5, PMOS_3 are on), transistors PMOS_4 and NMOS_3 turned off. Furthermore, at the commence of this phase, the control transistors are still off (since fn and fp are about VDD). Positive feedback during regeneration is intencified which results in lowering the delay time.

<div align="center">

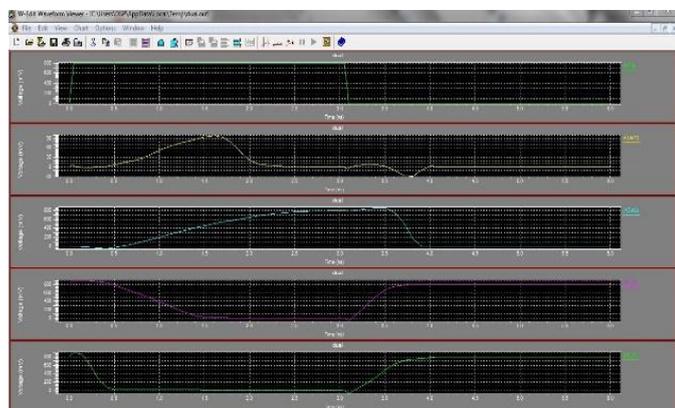**SIMULATION RESULTS**

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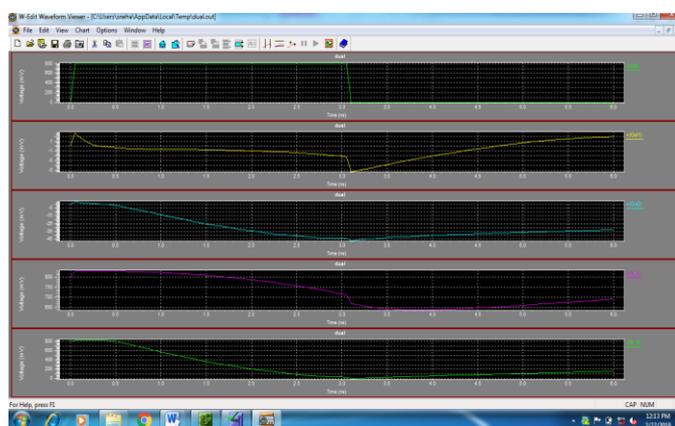*Fig.3 Output of the intented comparator in 180nm*

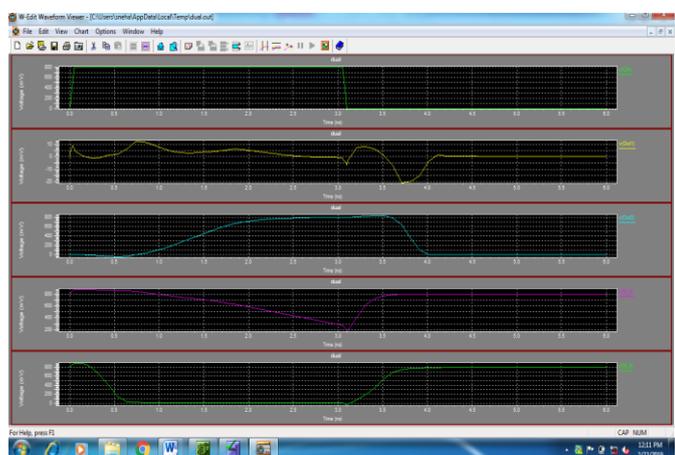*Fig.4 Output of the intented comparator in 90nm*

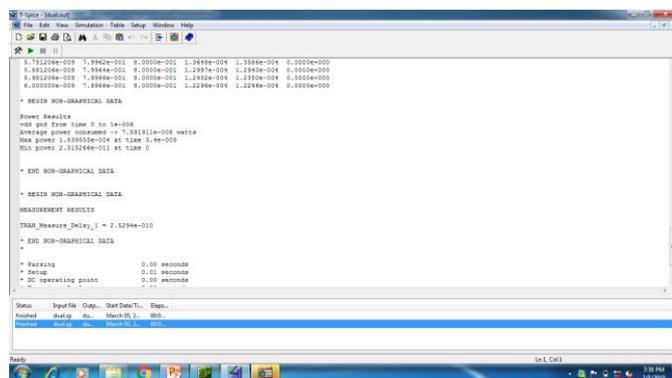*Fig.5 Output of the intended comparator in 45nm*

Fig.6 Calculated power in 180nm

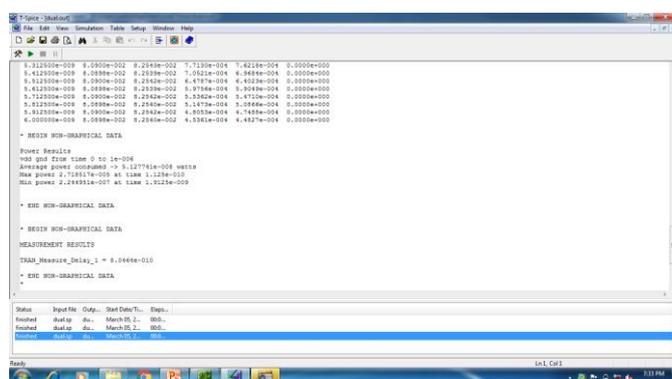*Fig.7 Calculated power in 90nm*
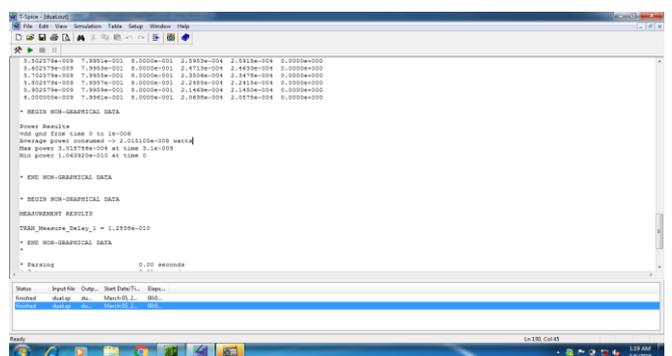
Fig.8 Calculated power in 45nm

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TABLE I

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	TECHNOLOGY (nm)	POWER (uW)	DELAY (ps)	TRANSISTOR COUNT
[1]	180	230	263	16
[4]	180	329	69	16
[8]	180	61	16	15
Existing	180	1.43	-	16
proposed	180	0.0759	252	12
	90	0.0512	804	12
	45	0.0201	265	12

TABLE II

	TECHNOLOGY (nm)	TEMPERATURE (degree)	POWER (uW)	DELAY (ps)
PROPOSED	180	25	0.0759	252
		30	0.07613	262
		35	0.07635	269
		40	0.07657	275
PROPOSED	90	25	0.05127	804
		30	0.05117	806
		35	0.05105	809
		40	0.05090	810
PROPOSED	45	25	0.02015	128
		30	0.02023	138
		35	0.02029	144
		40	0.02038	152

CONCLUSION

In this paper power is calculated for double tail dynamic comparator. Based on analysis a new comparator with low power capability was proposed, simulation in different CMOS technology shows that power of comparator is reduced to greater extent in comparison with conventional comparator and double tail comparator.

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