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Compensation in MOS Current Mirror Circuits

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Abstract

This paper investigates the state of the art compensation techniques and explores various possibilities for the enhancement of bandwidth of MOS-current-mirror circuits such as, simple current mirror, cascode-current-mirror, Wilson-current-mirror, improved-Wilson-current-mirror and Widlar-current-source. In this technique a carefully determined resistance is used in between the gates of primary transistor pair for enhancing the bandwidth. The magnitude error and phase error has been also investigated and found that both of them reduces due to compensation. Realization of both active and passive compensation technique has been also presented in this paper. The proposed circuits have been simulated using PSPICE for 0.25μm CMOS technology and the obtained results are compared with their uncompensated topologies to show their effectiveness.

Keywords: Current mirror, Bandwidth enhancement, Resistive compensation, Magnitude error, Phase.

Introduction

Current mirrors are one of the indispensable building blocks used in analog IC design. They are widely used for biasing and are used as active load for amplifier stages [6] and in analog and mixed mode circuits such as Second generation current-conveyors (CCIIs), Operational Mirrored Amplifiers (OMAs), Current Feedback Operational Amplifiers (CFOAs), analog filters etc. The current-comparator [5], current Schmitt-trigger and current A/D and D/A converters are additional examples of circuits that have benefitted from the use of current mirrors [4].Recent interest in the approach to analog circuit design, with its reliance on the use of current mirrors to achieve better high-frequency performance has led to the need for an increased understanding of the current mirror's high frequency response. It is often required that the current mirror should be capable to operate at high frequency. The commonly used technique for the bandwidth enhancement of a current mirror is a compensation technique. This technique is of two types, namely: "*passive compensation*" and "*active compensation*". Voo applied this technique for enhancement of bandwidth in simple current mirror [1]. The performance of a current mirror is limited by matching properties of the transistor, and the effects of transistor mismatch reduce by compensation [3].

Compensation technique is used in this paper for enhancing the bandwidth of current mirrors without disturbing their DC characteristics. This paper is organized as follows: The passive compensation technique have been applied in section 2 for various types of MOS current mirrors such as simple current mirror, cascode current mirror, Wilson current mirror, improved Wilson current mirror and Widlar current source. The active compensation technique has been applied to some of the current mirrors and is presented in section 3. Section 4 deals with the simulations using PSPICE and the comparative results are shown.

Passive Compensated Current Mirrors

Simple Current Mirror

The simple current mirror is a first order low pass filter whose bandwidth is a function of trans-conductance (g_m) and the gate to source capacitance (C_{gs}) and is given as:

$$\omega_o = \frac{g_m}{2C_{gs}} \qquad (1)$$

A compensation resistor is inserted between the primary gates of simple MOS current mirror as shown in Fig.1 and significant enhancement in bandwidth is observed without disturbing its DC characteristics [1].

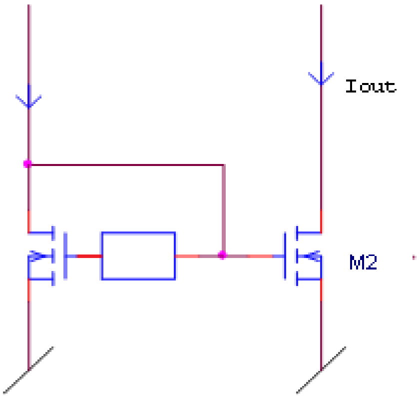


Figure 1: Simple Current Mirror Circuit with passive compensation

A compensation resistor is incorporated between the gates of transistor M_1 and M_2 as shown in the Fig.1, transposes the first order low-pass current mirror into a second order low-pass with one zero and two poles. The 3-db bandwidth for the same is given by

$$\omega_0 = \sqrt{\frac{g_{m1}}{RC_{gs1}C_{gs2}}} \tag{2}$$

It is worth mentioning that, by making $R = 1/g_{m1}$ and $C_{gs2} = C_{gs1}$, the zero which has been added after the insertion of the resistance cancels one of the poles yielding in a first-order system with the frequency response determined by $\omega_0 = g_{m1}/C_{gs1}$; that is the 3-db bandwidth of the compensated current mirror becomes double the bandwidth of uncompensated current mirror. The magnitude error and the phase error of the resistive-compensated-current-mirror are given below by (3) and (4) respectively. During the investigation, it was found that these errors were reduced to a significant level for compensated simple current mirror.

$$\left|\varepsilon_\omega(j\omega)\right| = 1 - \frac{\omega^2\tau_1^2}{8} - \frac{3\omega^4\tau_1^4}{32} - \frac{17\omega^6\tau_1^6}{256} \tag{3}$$

$$arg\left|\varepsilon_\omega(j\omega)\right| = -\frac{\omega\tau_1}{2} - \frac{\omega^3\tau_1^3}{2} \tag{4}$$

where, $\tau_1 = \frac{2C_{gs1}}{g_{m_1}}$

Cascode Current Mirror

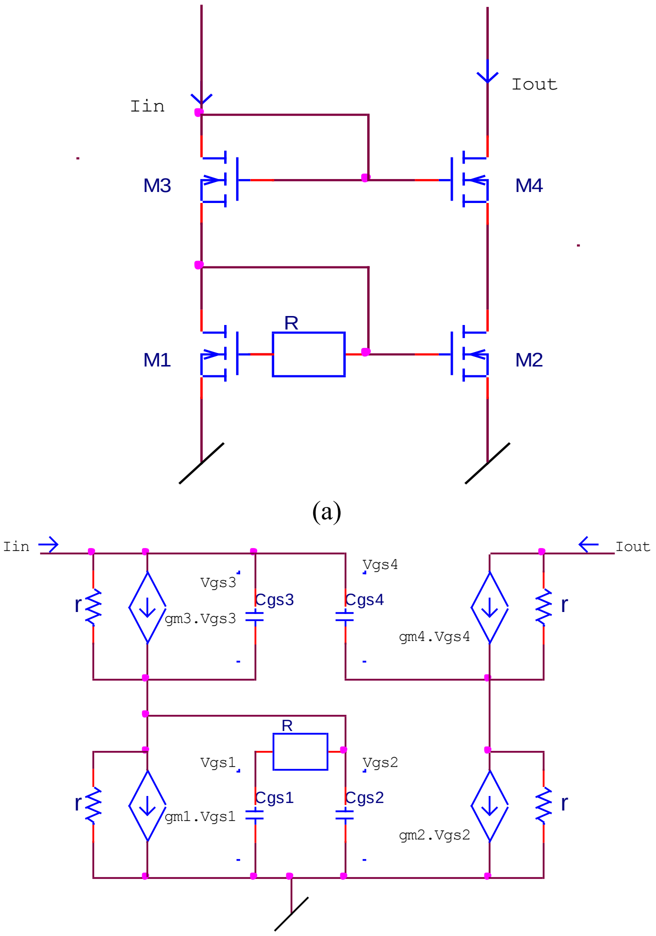
This section discusses the cascode current mirror with bandwidth enhanced by connecting passive resistance in the primary transistor of the current mirror. The uncompensated cascode current mirror is the second order low pass filter whose bandwidth is given as:

$$\omega_0 = \frac{g_m}{\sqrt{2}C_{gs}} \tag{5}$$

The passive compensated cascode current mirror is obtained by inserting a resistance between the gates of M_1 and M_2 as shown in Fig. 2a.

The high-frequency equivalent circuit of compensated cascode current mirror is shown in Fig. 2b. C_{gd} and output conductance has been neglected during the analysis. The small signal analysis of the circuit shown in Fig. 2b yields the following current transfer function-

$$\frac{I_o}{I_i} = \frac{g_{m4}g_{m2}\left(1+sRC_{gs1}\right)}{\left(\left(s^2RC_{gs1}C_{gs2} + s\left(C_{gs1}+C_{gs2}\right)+g_{m1}\right)\left(\left(sC_{gs4}+g_{m4}\right) + (sC_{gs4}(sRC_{gs1}+1)g_{m2}\right)\right)} \tag{6}$$



(a)

(b)

Figure 2: Cascode Current Mirror Circuit (a) Passive Compensated Cascode Current Mirror (b) High-frequency equivalent of Cascode Current Mirror

Putting $C_{gs1} = C_{gs2} = C_{gs3} = C_{gs4}$, $g_{m1} = g_{m2} = g_{m3} = g_{m4}$ & $R = 1/g_{m1}$ in (6) results in a second order equation as shown below-

$$H(s)=\frac{\dfrac{g_{m1}^{\;2}}{C_{gs1}^{\;2}}}{s^2+s\left(\dfrac{3g_{m1}}{C_{gs1}}\right)+\dfrac{g_{m1}^{\;2}}{C_{gs1}^{\;2}}} \tag{7}$$

$$\omega_0=\frac{g_{m1}}{C_{gs1}} \tag{8}$$

Bandwidth of compensated cascode current mirror is given by (8). A close observation of (5) and (8) reveals that at R = $1/g_{m1}$, the bandwidth of compensated MOS cascode current mirror is increased by a factor of $\sqrt{2}$ as compared to the bandwidth of uncompensated MOS cascode current mirror.

The magnitude and the phase error for the compensated MOS cascode current mirror are found to be-

$$\left|\varepsilon_{\omega}(j\omega)\right|=1-\frac{7\omega^2\tau_1^{\;2}}{2}-\frac{\omega^4\tau_1^{\;4}}{2} \tag{9}$$

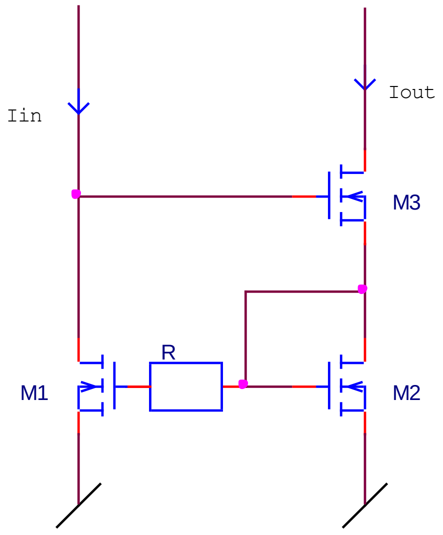
$$arg\left|\varepsilon_{\omega}(j\omega)\right|=-3\omega\tau_1-3\omega^3\tau_1^{\;3} \tag{10}$$

where, $\tau_1=\dfrac{C_{gs1}}{g_{m1}}$

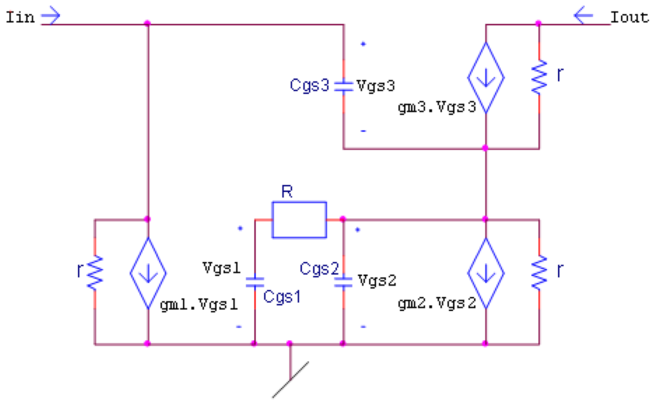
From equation (9) and (10) it can be revealed that, both the errors are considerably reduced for compensated current mirror circuit in comparison to the uncompensated current mirror circuit.

Wilson Current Mirror

The passive compensated Wilson MOS current mirror is shown in Fig. 3a.



(a)



(b)

Figure 3: Wilson Current Mirror Circuit (a) Passive Compensated Wilson Current Mirror (b) High-frequency equivalent of Wilson Current Mirror

Note that the compensating resistor is connected in series with the gate of M_1 and not in series with the gate of M_2 which reduces the bandwidth. The high-frequency equivalent of Wilson current mirror is shown in Fig. 3b and the routine analysis of it give the transfer function as follows-

$$\frac{I_0}{I_i}=\frac{\begin{array}{l}s^2\left(RC_{gs2}C_{gs1}g_{m3}\right)\\+s\left(C_{gs2}g_{m3}+C_{gs1}g_{m3}+RC_{gs1}g_{m2}g_{m3}\right)\\+g_{m3}g_{m2}\end{array}}{\begin{array}{l}s^3\left(RC_{gs3}C_{gs2}C_{gs1}\right)\\+s^2\left(RC_{gs1}C_{gs3}g_{m2}+C_{gs3}C_{gs2}+C_{gs1}C_{gs3}\right)\\+s\left(C_{gs3}g_{m1}+C_{gs3}g_{m2}\right)+g_{m3}g_{m1}\end{array}} \tag{11}$$

Putting $C_{gs}=C_{gs1}=C_{gs2}=C_{gs3}$, $g_m=g_{m1}=g_{m2}=g_{m3}$ and $R=1/g_m$ in (12) results in the transfer function as follows

$$\frac{I_o}{I_i}=\frac{s^2\left(C_{gs}^{\;2}\right)+s\left(3C_{gs}g_m\right)+g_m^{\;2}}{s^3\left(RC_{gs}^{\;3}\right)+s^2\left(3C_{gs}^{\;2}\right)+s\left(2C_{gs}g_m\right)+g_m^{\;2}} \tag{12}$$

$$\left|\varepsilon_{\omega}(j\omega)\right|=1+15\omega^2\tau_1^{\;2} \tag{13}$$

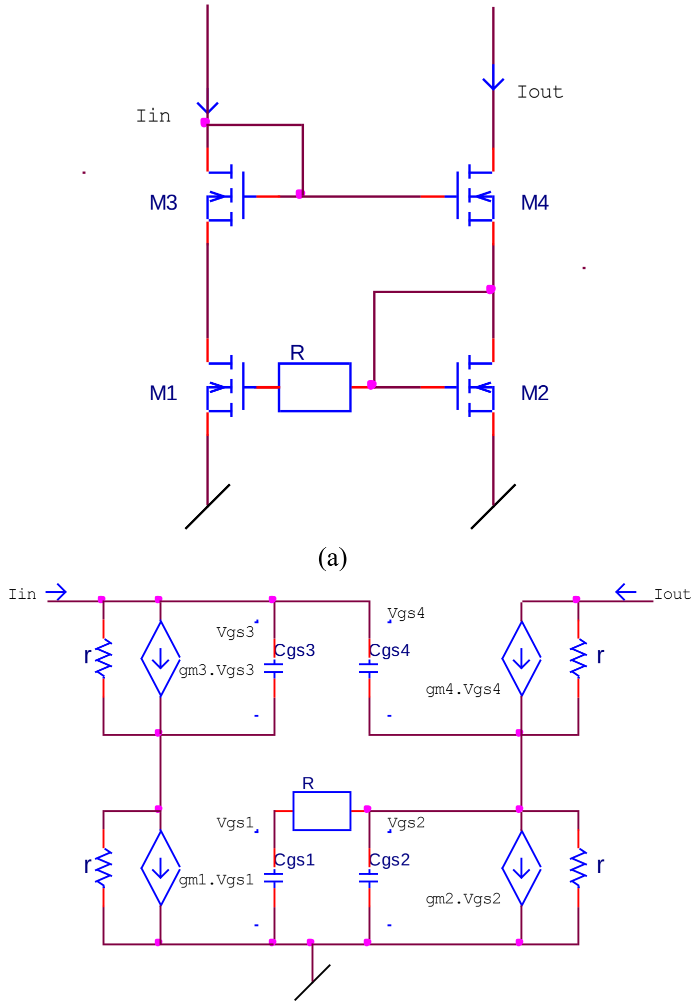
$$arg\left|\varepsilon_{\omega}(j\omega)\right|=3\omega\tau_1-8\tau_1-3\tau_1^{\;3} \tag{14}$$

where, $\tau_1=RC_{gs1}$

Equation (13) and (14) respectively gives the magnitude and phase error for the compensated Wilson current mirror which depicts that, both the errors have considerably reduced.

Improved Wilson Current Mirror

The passive compensated improved Wilson current mirror is shown in Fig. 4a and an analysis of its high-frequency equivalent circuit shown in Fig. 4b reveals that, the circuit realized following current transfer function given by (15).



(a)

(b)

Figure 4: Improved Wilson Current Mirror Circuit (a) Passive Compensated Improved Wilson Current Mirror (b) High-frequency equivalent of Improved Wilson Current Mirror

$$\frac{I_o}{I_i}=\frac{s^2\left(RC_{gs2}C_{gs1}g_{m4}\right)+s\left(C_{gs2}g_{m4}+C_{gs1}g_{m4}+RC_{gs1}g_{m2}g_{m4}\right)+g_{m4}g_{m2}}{s^3\left(RC_{gs4}C_{gs2}C_{gs1}\right)+s^2\left(RC_{gs1}C_{gs4}g_{m2}+C_{gs4}C_{gs2}+C_{gs1}C_{gs4}\right)+s\left(C_{gs4}g_{m1}+C_{gs4}g_{m2}\right)+g_{m4}g_{m1}} \qquad (15)$$

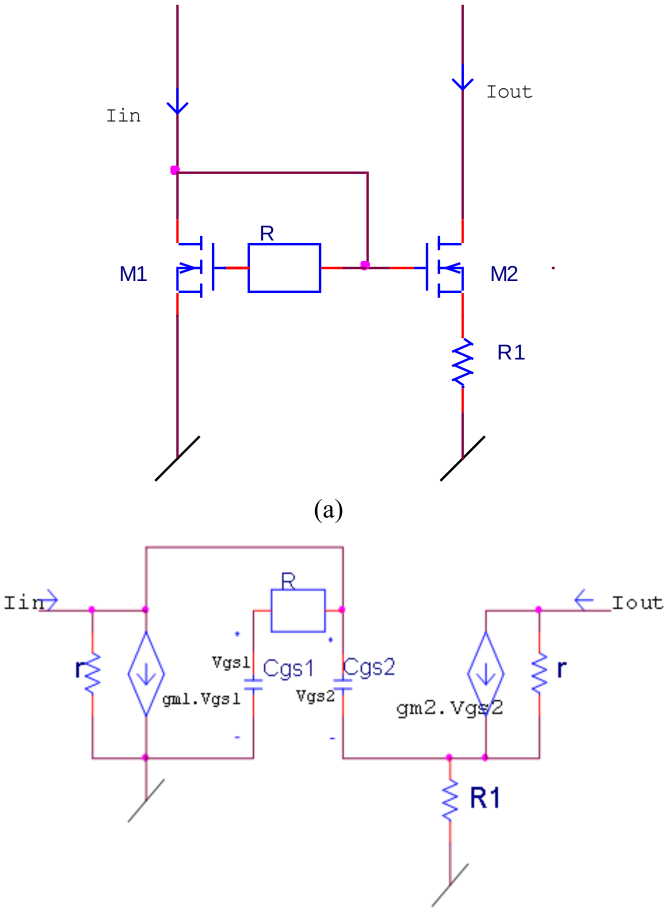
Keeping $C_{gs} = C_{gs1} = C_{gs2} = C_{gs4}$ and $g_m = g_{m1} = g_{m2} = g_{m4}$ in (15), the above transfer function can be rearranged as-

$$\frac{I_o}{I_i}=\frac{s^2\left(RC_{gs}{}^2g_m\right)+s\left(2C_{gs}g_m+RC_{gs}g_m{}^2\right)+g_m{}^2}{s^3\left(RC_{gs}{}^2\right)+s^2\left(RC_{gs}{}^2g_{m2}+2C_{gs}{}^2\right)+s\left(2C_{gs}g_m\right)+g_m{}^2} \qquad (16)$$

The result can be verified through PSPICE simulation.

Widlar Current Source

The compensated Widlar current source is obtained by incorporating a resistor R between the gates of M_1 and M_2 as shown in Fig. 5a. The high-frequency equivalent circuit for Widlar current source is shown in Fig. 5b where gate to drain capacitance of both the transistors $M_1$and M_2 is neglected.



(a)

(b)

Figure 5: Widlar Current Source Circuit (a) Passive Compensated Widlar Current Source (b) High-frequency equivalent of Widlar Current Source

A rigorous analysis of the circuits shown in the Fig. 5b gives the following current transfer function-

$$\frac{I_o}{I_i}=\frac{g_{m2}\left(1+sRC_{gs1}\right)}{\left[\left(sR_1C_{gs2}+g_{m2}R_1+1\right)\left(sC_{gs1}+g_{m1}\right)+sC_{gs2}\left(sRC_{gs1}+1\right)\right]} \qquad (17)$$

Equation (17) reveals that the compensated Widlar current source circuit is a low-pass filter and the 3-db bandwidth is given by

$$\omega_0=\left[\frac{g_{m1}\left(g_{m2}R_1+1\right)}{\left(R+R_1\right)C_{gs1}C_{gs2}}\right]^{1/2} \qquad (18)$$

Active Compensated Current Mirrors

For full monolithic integration, the passive compensation resistor is made up of poly-silicon and absolute value of such type of resistors will have a large tolerance. Besides, the variation in the value of resistor (due to its temperature dependency) does not track the trans-conductance of the MOS transistors. However, for optimum compensation it is required that R = l/g_{ml}, which cannot be obtained easily, because, R is required to track the trans-conductance g_{ml} which varies considerably with process and temperature drifts.

To overcome this draw back the passive resistance can be replaced by an active resistance as shown in Fig. 6, small transistor M_3 (operating in triode region), with tunable gate voltage V_c [2]. This will increase little extra power consumption and minimal increase in chip area. In this paper the active compensation technique has been applied to the circuits of passive compensated cascode current mirror and Wilson current mirror proposed in previous section.

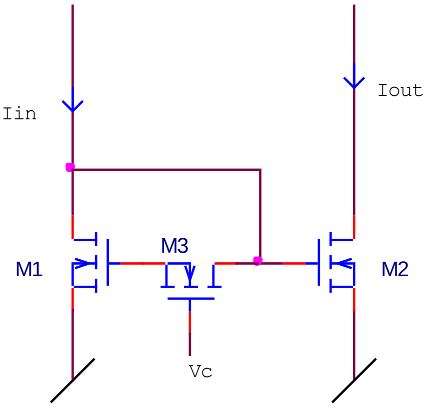


Figure 6: Simple Current Mirror Circuit with Active Compensation

The circuit of active compensated cascode current mirror is shown in Fig. 7.

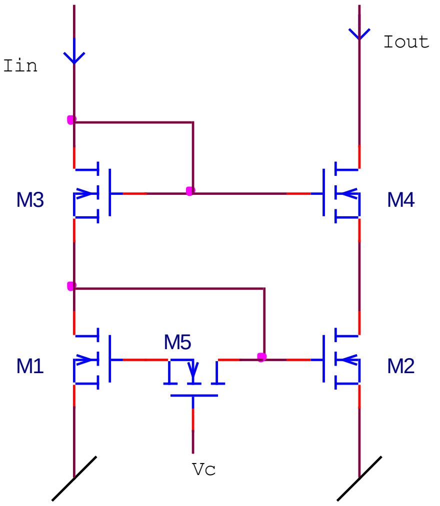


Figure 7: Cascode Current Mirror Circuit with Active Compensation

All transistors M_1 to M_4 are operating in saturation region, whereas transistor M_5 is working in triode region as a voltage controlled resistor and its equivalent resistance r_{ds} is given as

$$r_{ds5}=\frac{1}{\mu_n C_{ox}\left(\frac{w}{l}\right)_5\left(V_{gs5}-V_t\right)} \tag{19}$$

The rigorous analysis of the circuit shown in Fig. 7 gives the transfer function as follows:

$$\frac{I_o}{I_i}=\frac{g_{m4}g_{m2}\left(1+sr_{ds}C_{gs1}\right)}{\left(\begin{array}{l}\left\{\left(s^2 r_{ds}C_{gs1}C_{gs2}+s(C_{gs1}+C_{gs2}\right)+g_{m1}\right\}\\ \left(sC_{gs4}+g_{m4}\right)\left\{sC_{gs4}\left(sr_{ds}C_{gs1}\right)\right\}+g_{m2}\end{array}\right)} \tag{20}$$

Similarly, the active realization of compensated Wilson current mirror is shown in Fig. 8.

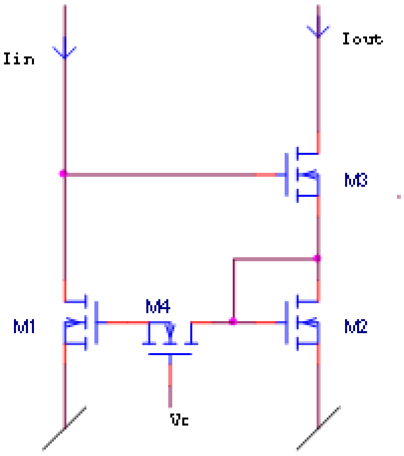


Figure 8: Wilson Current Mirror Circuit with Active Compensation

Rigorous analysis of the circuit shown in Figure-8 reveals the following current transfer function-

$$\frac{I_o}{I_i}=\frac{\begin{array}{l}s^2\left(r_{ds}C_{gs2}C_{gs1}g_{m3}\right)+\\ s\left(C_{gs2}g_{m3}+C_{gs1}g_{m3}+r_{ds}C_{gs1}g_{m2}g_{m3}\right)+g_{m3}g_{m2}\end{array}}{\begin{array}{l}s^3\left(r_{ds}C_{gs3}C_{gs2}C_{gs1}\right)\\ +s^2\left(r_{ds}C_{gs1}C_{gs3}g_{m2}+C_{gs3}C_{gs2}+C_{gs1}C_{gs3}\right)\\ +s\left(C_{gs3}g_{m1}+C_{gs3}g_{m2}\right)+g_{m3}g_{m1}\end{array}} \tag{21}$$

The above current transfer functions reveals that, as the value of r_{ds} is varied by changing the external control voltage V_c, the bandwidth of the circuit becomes tunable.

Simulation Results

All the proposed circuits have been simulated using Pspice for 0.25μm technology. Fig. 9 to 12 shows the magnitude response of the proposed passive compensated cascode current mirror, Wilson current mirror, improved Wilson current mirror and Widlar current source for different values compensating resistance. It is observed that bandwidth of all compensated current mirrors has improved significantly. Active compensated current mirror circuits are proposed in Fig. 7 and 8 with thier magnitude response shown in Fig. 13 and 14 respectively. These figures reveals a significant improvement in operating frequency. Table 1 show the comparative results of different MOS current mirrors with and without compensation. Note that, there is no change in power dissipation and input resistance with or without compensating resistance.

Table 1 Comparitive results for different current mirror topologies

Current mirror	Performance factor without resistance			Performance factor with passive resistance				Performance factor with active resistance			
	Bandwidth (MHz)	Power dissipation (mW)	Input resistance (KΩ)	Bandwidth (MHz)		Power dissipation (mW)	Input resistance (KΩ)	Bandwidth (MHz)		Power dissipation (mW)	Input resistance (KΩ)
				With peaking	Without peaking			With peaking	Without peaking		
Cascode current mirror	147	22.1	0.877	338	307	22.1	0.877	290	267	23.7	0.848
Wilson current mirror	41	24.1	0.569	96	88	24.1	0.569	615	547	21.3	1.071
Improved Wilson current mirror	45	25.9	0.55	102	90	25.9	0.55	-	-	-	-
Widlar current source	241	25.9	0.44	570	504	25.9	0.44	-	-	-	-

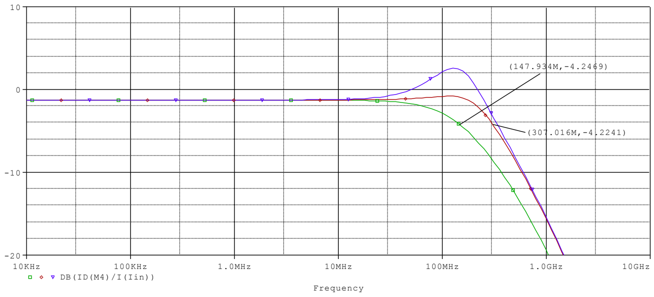


Figure 9: Passive Compensated MOS Cascode Current Mirror Circuit

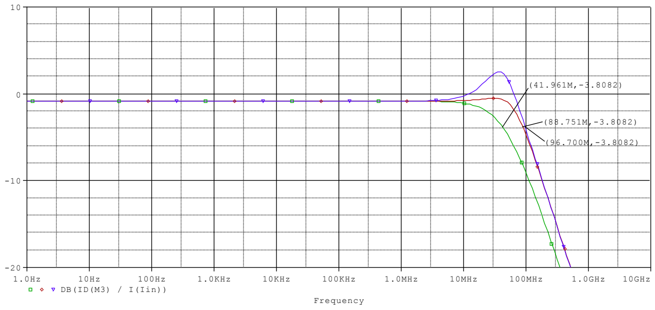


Figure 10 : Passive Compensated MOS Wilson Current Mirror

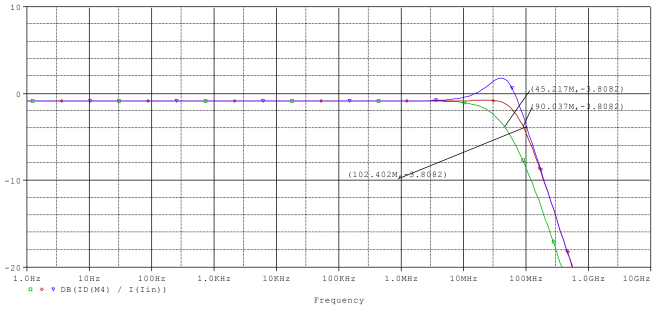


Figure 11 : Passive Compensated Improved Wilson Current Mirror

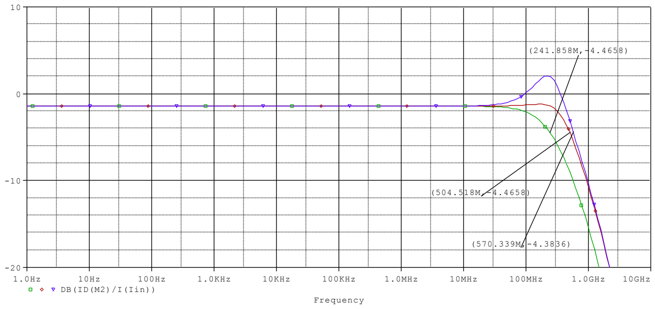


Figure 12: Passive Compensated MOS Widlar Current Source

Conclusion

A simple method for enhancing bandwidth of current mirrors reported in the literature has been verified by incorporating a resistance between the gates of primary transistors. The passive compensation technique is applied to cascode current mirror, Wilson current mirror, improved Wilson current mirror and Widlar current sources. All the proposed circuits have been rigorously analyzed and their current transfer function, bandwidth, magnitude error and phase error have been determined and found that there is a considerable enhancement in the bandwidth, without any change in design parameters such as large signal gain, power consumption and input resistance. All the realized circuits were tested using PSPICE, and the simulated results confirm the theoretical result. The proposed circuits are suitable for VLSI implementation and high-frequency signal processing, useful in communication.

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