

ARQ Technique with Aggressive Packet Combining Scheme for Variable Error Rate Channels to Reduce the Bandwidth and Power Consumption

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Abstract

Automatic repeat request (ARQ) schemes are two way packet transmission systems in which a feedback is used to acknowledge (ACK) or not acknowledge (NACK) each packet. If data is received erroneously, retransmission is sought and too many retransmissions in error-prone wireless environments not only create potential latency but also limit the overall bandwidth capacity. But when the channel is idle, using ARQ would be a clever way to save the bandwidth and thus increasing the throughput (here throughput is calculated as the average (N) number of times a packet is transmitted to get the correct copy. Aggressive packet combining (APC) is a scheme for error control which exploits the information available in the erroneous copies to recover the correct copy. This reduces the number of retransmissions thus reducing bandwidth and power consumption of a system. In this paper, ARQ technique with Aggressive Packet Combining (APC) is considered to improve the performance of wireless network. The proposed scheme has advantage of more bandwidth efficiency, low power consumption, higher throughput and better correction capability than the existing ARQ and APC scheme.

Keywords: Automatic repeat request (ARQ), Aggressive packet combination (APC), bit wise majority logic, throughput, and power consumption.

Introduction

BEC (Backward Error Control) or FEC (Forward Error Control) strategies are used in order to transfer data reliably from source to destination. FEC is used for error correction and BEC is used for error detection. FEC is costly as compared to BEC as FEC consumes higher bandwidth. BEC is implemented by automatic repeat request (ARQ) protocols in which error detection codes are used and ACK (acknowledgment) message and/or NACK (negative acknowledgment) message are used in feedback path to achieve reliable data transmission. Receivers send ACK

message for reception of correct data and NACK message for erroneous data. Due to the limited CRC information and capability, receivers usually discard any data packet with errors and trigger retransmissions, regardless of how many bits are flipped during transmission. As a consequence, the ARQ scheme imposes a high constraint on a time-varying wireless link because errors incurred in transmissions and retransmissions are time independent. Those correct bits of the received packet incur unnecessary retransmissions as well. Unfortunately, the standard CRC technique does not associate with any method to recover errors from erroneous data packets, as an improper process may render a potential computation and resource consumption. Too many retransmissions in ARQ in error-prone wireless environments not only create potential latency but also limit the overall bandwidth capacity. Recent researches have suggested several modifications to improve the performance of ARQ [1-7]. Chakraborty et al. [8-10] suggested a very simple and elegant technique known as packet combining (PC) technique for error correction at the receiving end. In this technique, XOR operation is performed to locate error locations/positions using two received erroneous copies of the packet and correction is done based on the error positions so found. Various modifications of PC are found in literatures and one of these is Majority packet combining (MPC) scheme [11]. An Aggressive packet combining (APC) scheme was proposed by Leung [12] for error control and reducing latency in wireless data communication. This scheme is a modification of majority packet combining scheme for correction of erroneous data which further exploits the information available in the erroneous copies to recover the correct packet. In APC, three copies of a packet are sent from transmitter to receiver. The receiver performs bit wise majority logic on received copies to get a correct copy. In general, an erroneously received packet is likely to possess some useful information by which receivers can derive the original packet from a number of erroneously received copies. Practical channels do not remain in same state all the time. It varies all the time so using only APC scheme will consume

extra bandwidth when the channel is in low (L) error rate condition thus reducing throughput although it has high correction capability. On the other hand, when channel is in high (H) error condition using only ARQ will result in too many retransmissions which lead to latency and extra bandwidth consumption. When channel is in L state sending a single copy will be advantageous over sending multiple copies at a time. Satisfactory performance with ARQ technique may be achieved upto BER of 10^{-3} [10]. ARQ scheme gives higher throughput when channel is in L state and APC gives better error correction capability when channel is in H state. Thus in this paper combination of ARQ technique and APC scheme is taken to implement them in different error rate condition of channels so to improve the performance of the system.

Related Work

Review of Existing ARQ:

Consider an ARQ scheme as shown in figure 1, where packet1 is transmitted and receiver on reception of packet1 will send ACK message if the received packet is correct. Transmitter on receiving ACK message will now transmit next packet. In case erroneous packet is received by receiver, NACK message is sent to transmitter to inform that error occur while receiving data and requesting for retransmission of the packet.

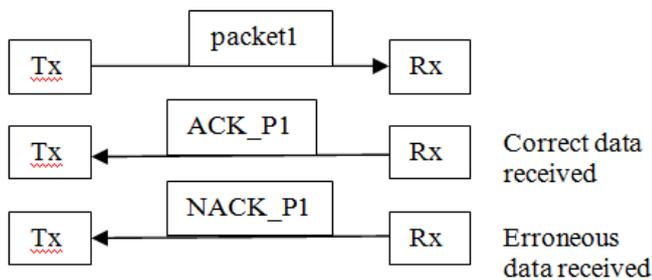


Figure 1: traditional ARQ scheme

Review of Packet Combining Technique:

Packet combining scheme also known as extended automatic repeat request (EARQ) is a modification of existing ARQ. In this scheme errors are located by XOR operation between erroneous copies. Following procedure are performed in packet combining scheme:

Step1) Transmitter sends packet1 to receiver and wait for ACK message before transmitting next packet2.

Step 2) Receiver on reception of correct packet1 sends ACK to transmitter, if the received packet1 is erroneous then the receiver sends NACK to transmitter and request for retransmission of packet1 and keeping erroneous copy in its buffer.

Step 3) If requested retransmission packet1' is correct then receiver discard the previously retain erroneous packet1.

Step 4) When retransmitted packet1' is received erroneously again then bit wise XOR operation is performed between retransmitted packet1' with erroneous retained packet1 stored in receiver's buffer.

Steps 5) Error locations are indicated by presence of 1's at calculated packet after XOR operation.

Steps 6) To obtain correct copy the bit inversion of bit(s) in error location(s) is done.

Let the original packet is "0110".The packet is received as "1110" which is an error. The receiver request for retransmission and retain the erroneous packet. Transmitter retransmits the packet but again the erroneous packet is received by the receiver as "0111". Now, bit wise XOR operation between erroneous copies (i.e. first transmitted packet & retransmitted packet) is performed to locate the error position.

Table 1: An example for Packet Combining scheme

Original	0110
First error packet	1110
Retransmitted error packet	0111
XOR operation between erroneous packet to get the erroneous bit positions	1001

The error locations are identified as first and fourth bit from the left. The receiver can apply bit inversion method to correct error that is by changing "1" to "0" or vice versa. Implementation of packet combining scheme can be found in [13- 14].

Review of Aggressive Packet Combining Scheme

Aggressive packet combining scheme is a modification of MjPc (Majority Packet Combining) [15, 16]. To illustrate APC, let us assume an original packet '11111'. The transmitter sends three copies of the packet to receiver. The entire packets that reached to receiver are erroneous '11011', '11110' & '11011'. Now, majority logic is applied bit by bit on three copies of packet and thus get a generated copy as 11011.

Table 2: An example of Aggressive Packet Combining scheme

Received Copy 1	11011
Received Copy 2	11110
Received Copy 3	11011
Majority logic is applied bit by bit	11011

Receiver applies error detection scheme to find whether generated copy is correct or not. As it is not correct in this case, the receiver chooses least reliable bit from combined packet. In this case these are the third and fifth bit from the left side. Receiver searches correct bit pattern on the least reliable bits followed by error detection. By the process it may get a correct copy. If it fails it requests for retransmission when the sender will repeat three copies of retransmission.

Proposed Scheme

The practical channels are always dynamic [17] and they are all variable error rate channels. In such case alteration of packet being sent by the channel is obvious and it will increase bandwidth and power consumption of the system if retransmission is sought as a result decreasing the throughput or performance of the system. In order to achieve bandwidth

efficient, low power consumption and increased throughput, a new modified technique is introduced for transmission of packet from source to destination. In the proposed technique, Backward Error Control (i.e. existing ARQ) as well as Forward Error Control (i.e. existing APC) strategies are combined to improve the performance of the system in variable error rate conditions. We will assume a two-state channel as in [18] for this scheme.

The channel may stay either in the state of low error rate or in the state of high error rate, which may be respectively, denoted as L and H states. When the channel is in L state, transmitter will follow the conventional ARQ scheme. When the channel is in H state, the transmitter will send $i=2$ copies of transmission of the previous packet keeping previously received copy in its buffer and apply APC in these three copies if the received two copies are also erroneous. Initially assuming that the channel is in L state, Source node will transmit only one copy of the packet as in conventional ARQ scheme. Let us assume that C1 is the first original packet sent by transmitter and following procedure will occur.

Case1: correct packet is received then receiver sends ACK message to transmitter & next packet is transmitted by transmitter.

Case2: copy (C1) received with an error, receiver retains the C1 in error and sends NACK message with requesting for retransmission of packet to transmitter. If transmitter receives two or more than two continuous NACKs, transmitter switches to APC by sending $i=2$ copies and if these two copies are erroneous too then APC is applied using these copies and copy stored in buffer. It amounts to say that receipt of two or more continuous NACKs is the signal of H state of the channel.

Now, in response to NACKs, the transmitter will retransmit two copies of the same packet (C₂ & C₃) instead of one copy (as per existing ARQ transmitter retransmits only one copy).

If the packet reaches the receiver with an error then the entire erroneous copies (i.e. C1, C2 & C3) are taken as in existing APC to perform error correction. Following steps are performed to combine them [12].

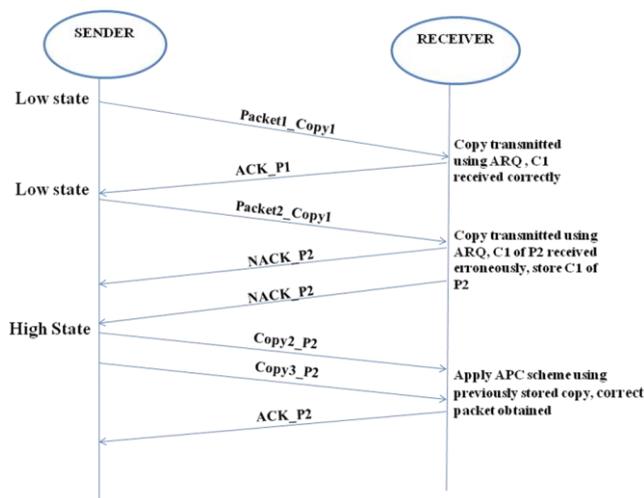


Figure 2: Proposed ARQ-APC scheme for variable error rate channels

Step1: The receiver performs bit by bit majority voting on erroneous packet to produce combined packet.

Let us assume original packet O = '11111' and all error copies at receiver are C1=11011, C2= 11110, C3=11011. After bit by bit majority logic the generated packet is 11011.

Step2: Error detection procedure is done to find whether combined packet generated is correct or not.

Step3: As it is not correct in the given example, the least reliable bit in the combined packet is found. In this case these are the third and fifth bit from the left side.

Step4: The combined packet consists of erroneous two bits '01' in the third and fifth bit from right. The receiver search for the correct bit pattern thus, they may be '00' or '10' or '11'.

Step5: Erroneous two bits are corrected by replacing with the above three bit pattern (i.e. '00' or '10' or '11') and error detection is again done to find the correct copy. Then correct packet '11111' is received by receiver.

Let the probability that the channel is in low and high state are P_L and P_H respectively. The throughput of the proposed ARQ-APC scheme is given as [19]:

$$\eta_{ARQ-APC} = \eta_{ARQ} \cdot P_L + \eta_{APC} \cdot P_H \quad (1)$$

Where

η_{ARQ} = throughput efficiency when the system is in low state
 = throughput efficiency of conventional ARQ

$$\eta_{ARQ} = 1 - P_{ARQ} / 1 + P_{ARQ} \quad (2)$$

Where P_{ARQ} is the packet error probability in ARQ scheme and is given by:

$$P_{ARQ} = [1 - (1 - \alpha)^n] \quad (3)$$

Where α is bit error rate (BER), n is the packet size.

P_L = Probability that the system is in L state

$$= p_1 / (p_1 + p_2) \quad [18] \quad (4)$$

Where p_1 is the transition probability of the system from L state to H state, p_2 is the transition probability from H state to L state

P_H = Probability that the system is in H state

$$= p_1 / (p_2 + p_1) \quad [18] \quad (5)$$

η_{APC} = throughput efficiency when the system is in high state
 = throughput efficiency of conventional APC

$$\eta_{APC} = (1 - P_{APC}^3) / (3 + P_{APC}^3) \quad (6)$$

Where P_{APC} is the packet error probability in APC scheme and is given by:

$$P_{APC} = [1 - (1 - \alpha)^n]^3 \quad (7)$$

Simulation Results and Analysis

We have evaluated the performance of the proposed scheme in terms of packet error rate, bandwidth efficiency, power consumption and throughput. The simulation has been done using MatLab R2012 on windows 7 computer to evaluate the performance in terms of throughput and packet error rate of ARQ, APC and the proposed ARQ-APC scheme. And the qualitative analysis of power consumption and bandwidth

utilization of the proposed scheme and ARQ and APC scheme is done.

Curve (Fig.3) has been plotted by taking values of bit error rate (α) [17] from 10^{-5} to 10^{-2} for probability of packets in error for packet size $n=64$ for ARQ, APC and proposed ARQ-APC scheme. Lesser the packet error rate better will be the correction capability of the scheme.

(a) Probability of packet in error (PER):

Packet error probability in the proposed ARQ-APC scheme is given by:

$$P_{ARQ-APC} = P_{ARQ} \times P_L + P_{APC} \times P_H \quad (8)$$

Where the terms has its usual meaning as given in section III.

(b) Throughput:

Throughput (η) is expressed in terms of average number (i) of packets to be transmitted for successful receipt.

The throughput for the proposed ARQ-APC scheme is given as:

$$\eta_{ARQ-APC} = \eta_{ARQ} \cdot P_L + \eta_{APC} \cdot P_H \quad (9)$$

Where the terms has its usual meaning as given in section III.

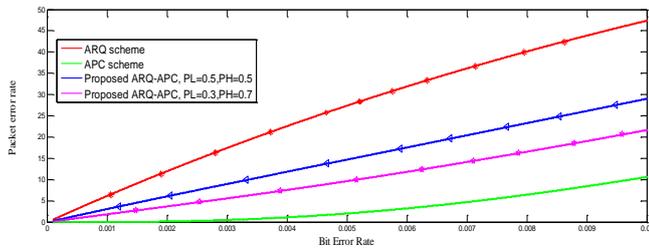


Figure 3: Packet error rate for packet size $n=64$

The simulation results show the effectiveness of proposed scheme over conventional ARQ scheme in high error rate channels. And fig. 4 shows the throughput comparison of ARQ, APC and proposed ARQ-APC scheme.

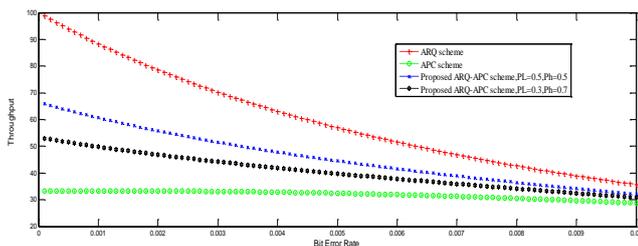


Figure 4: Throughput with packet size $n=64$

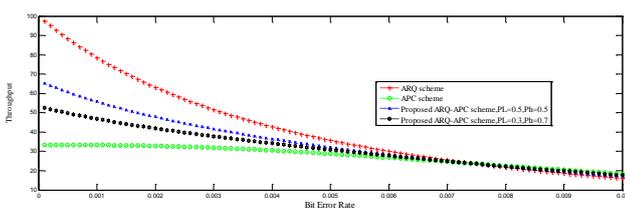


Figure 5: Throughput with packet size $n=128$

As according to fig.5, throughput of the proposed scheme becomes higher than the ARQ and APC scheme when channel condition becomes worst (very high error). When channel condition is in Low state, ARQ gives very good throughput as seen in figure but with the worsening of channel condition proposed scheme dominate all the remaining techniques. And for the remaining parameters following analysis are done:

Case I: Bandwidth efficiency

A measurement of ability of an electronics communication device to transmit information from sender to receiver is known as bandwidth. Let 'Bt' be the bandwidth for transmission of one packet. Let 'Bt' be the bandwidth for transmission of one packet. It is the difference between the upper and lower cutoff frequencies in a continuous set of frequencies given by [20]:

$$B_t = F_U - F_L \quad (10)$$

Where, F_U - Upper cutoff Frequency

F_L - Lower cutoff Frequency

Now, the qualitative analysis are done to find how bandwidth saving and minimized power consumption take place in the proposed scheme. Let us assume that total 10 packets are transmitted and each packet utilizes 1 Bt of bandwidth.

1) As per existing ARQ the total bandwidth utilization will be 10 Bt, if no errors occur while transmitting the packet. In APC, three copies of a packet are sent from transmitter to receiver at one time. While transmitting 10 packets, total number of bandwidth use will be $3 \times 10 \text{Bt}$ i.e. 30Bt.

- Total bandwidth utilization for ARQ = 10Bt (for error free 10 packets)
- Total bandwidth utilization for APC = 30Bt (for 10 packets)

2) In the proposed scheme, while transmitting 10 packets, if error occur in three packets then applying above bandwidth technique the number of bandwidth utilization will be 7Bt for the correctly received packet & for erroneous packet the bandwidth utilization will be $(3 \times 3 \text{Bt})$. Thus total bandwidth uses are 16Bt, which is less as compared to the bandwidth utilization of APC scheme only.

If we calculate the bandwidth saving then the total bandwidth saving as compared to APC is:

- Total bandwidth utilization for the Proposed Scheme = 16Bt (for 3 erroneous packet out of 10 packets)
- Bandwidth saving = $30 \text{Bt} - 16 \text{Bt} = 14 \text{Bt}$

Case II: Energy efficiency

The power consumption is needed for delivering of each packet from source to destination. Power consumption in existing ARQ is less as compared to APC where three copies are sent at a time. We assume P_1 be the power utilized for transmission of packet from source to destination and P_2 be the power used to send ACK/NACK message from receiver to transmitter. NACK & ACK are the feedback message; it is a response on received packets by receiver. Size of the feedback message is very small thus, power use to transmit feedback message is very less as compared to power utilized to transmit packet i.e. $P_1 \gg P_2$.

If 10 packets are transmitted as per existing ARQ, total number of power consumption when error free packet is received is P_t .

$$P_{TARQ} = 10P_1 + 10P_2 \quad (P_1 \gg P_2)$$

For APC, power utilized to transmit 10 packets is P_{TAPC}

$$P_{TAPC} = 30P_1$$

Power consumption in a condition where error occur in three packets while transmitting 10 packets is

$$P_t = 10P_1 + 13P_2 + 6P_1' \quad (P_1 \gg P_2)$$

Here, $6P_1'$ is the power utilized to retransmit the copies of previous error packet. As compared to APC, total power saving by the proposed scheme is

- Power saving = power utilized in APC - power utilized in proposed scheme.
- Power saving is = $30P_1 - (10P_1 + 13P_2 + 6P_1')$
- Assume $P_1 = P_1'$ & $P_1 = 4P_2$ (since packet size of NACK or ACK is very small as compared to data packet as $P_1 \gg P_2$)
- Power saving of the proposed technique, $P_{TARQ-APC} = 30P_1 - 20P_1 = 10P_1$

Conclusion

The proposed technique of combined ARQ with Aggressive Packet Combining scheme can be used for error detection as well as error correction, which is better than existing ARQ and APC in terms of bandwidth utilization, power consumption, packet error probability and most importantly throughput as seen in section IV. We have studied the proposed scheme in the two states considered as Low and High state. This scheme which simply estimates the channel state based on the ACK/ NACK messages received and adaptively switches its operation mode. Simulation results show that proposed ARQ-APC scheme gives higher throughput than the conventional APC and lower PER than ARQ scheme. Also the proposed scheme has less bandwidth and power consumption as compared to ARQ and APC alone. The proposed scheme can be generalized to consider more channel states. However the proposed scheme of ARQ-APC scheme, inherit the limitation of APC scheme, which is the inability to tackle the situation when error occur in the same bit location of all the received erroneous copies. Thus, we can conclude that the proposed scheme gives better performance in variable error rate channel as compared to existing ARQ and APC technique.

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