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Design of Gate All Around Silicon Nanowire FET with Triple Material Gate

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Abstract

In this paper we investigate the performance of a gate all around nanowire FET with triple material at gate. The electrical characteristics of the proposed structure is compared with previously developed structures. DIBL (Drain Induced Barrier Lowering) and DC gain is also compared and found to be good compared with existing *single* gate and double gate structures. All the simulations are done using TCAD (Technology Computer Aided Design) Sentaurus Simulator.

Keywords: Nanowire, TCAD, Sentaurus, DIBL, Gate all around.

INTRODUCTION

Following Moore's law to meet the requirements for speed, complexity and circuit density the transistors have been scaled down throughout years. But as scaling progresses short channel effects also get introduced [1]. So new models have to be developed as an alternative for planar MOSFET technology. The gate all around structure shows an improvement in electric field intensity at source-channel interface [2]. Thereby the structure is able to withstand many short channel effects. The three dimensional structure of a gate all around nanowire FET with triple material at gate is shown in figure 1.

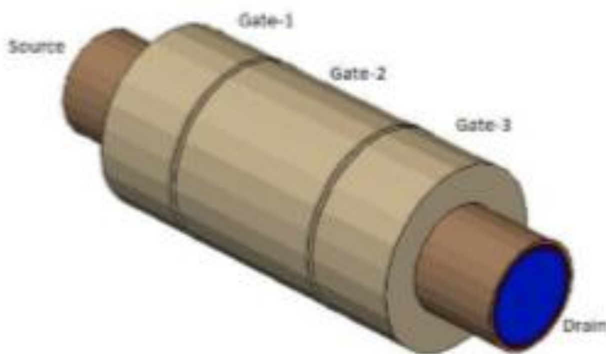

Fig 1: 3D Structure of gate all around nanowire FET with triple material gate

METHODOLOGY

Structure design and all simulations are done using Sentaurus Device Simulator. Sentaurus Device is used to simulate the electrical characteristics of the device. Finally, Sentaurus Visual is used to visualize the output from the simulation in 2D and 3D, and Inspect is used to plot the electrical characteristics. Typical tool flow of the device simulator is shown in the figure 2.

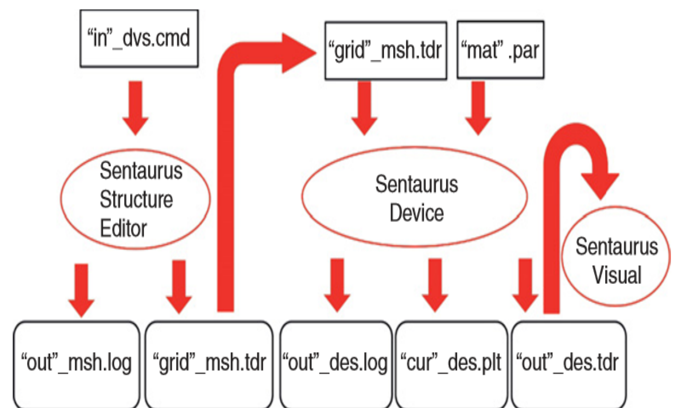

Figure 2: Typical tool flow with device simulation using Sentaurus Device

By numerical calculation of the physical equations governing the carrier profile and the conduction mechanisms TCAD mimics the electrical behavior of the FETs. Any real FET is approximated as a virtual device whose physical property such as doping is discretized into a number of mesh points (also called nodes or grids). Therefore, the actual continuous device is represented as a finite number of sparse mesh points. The physical equations such as the Poisson equation and the electron and hole current continuity equations are self-consistently solved at these discrete mesh points in an iterative manner. In each iteration, an error is calculated and the tool tries to converge upon a solution which produces an error which is lower than an acceptable value (which may be predefined). Therefore, the TCAD essentially emulates the electrical behavior of any FET by numerical solution of some differential equations.

The electrical characteristics of the device are simulated using the Sentaurus device (Sdevice). In addition to the TDR file, which contains information about the device structure, Sdevice requires a command file that contains all the relevant information about the physical models to be used for device simulations, the initial boundary condition of the contacts, the mathematical solver to be used for numerical simulations, the voltage or current values to which the contact electrodes need to be ramped, the microscopic properties that need to be analyzed such as electric field, potential profile, and so on. Apart from the command file, Sdevice also requires a parameter file as input. The parameter file contains the default values of all the parameters used in the physical models governing the FET behavior. These parameters may be tuned to match the experimental results which is known as model calibration. Sdevice generates a final TDR file, which contains the spatial solution of the different equations, and a PLT file, which contains the relationship between the terminal voltages, currents, and charges. Sentaurus visual (Svisual) utilizes the final TDR file as input and can be used to visualize the different microscopic properties such as the electric field, carrier concentration, potential profile, and so on, which were specified in the command file used for Sdevice. These properties are obtained from the spatial solution of the different differential equations in Sdevice. Moreover, Svisual can also be used to perform mathematical operations on the obtained microscopic properties such as integration, multiplication, differentiation, and soon. The information about the terminal charges, voltages, or currents at different contacts is embedded in the PLT file. Svisual can also be used for analyzing data from the PLT file [3].

STRUCTURE AND DEVICE DIMENSIONS

A schematic view of three dimensional gate all around nanowire FET implemented in a TCAD Sentaurus Simulator is shown in figure 3.

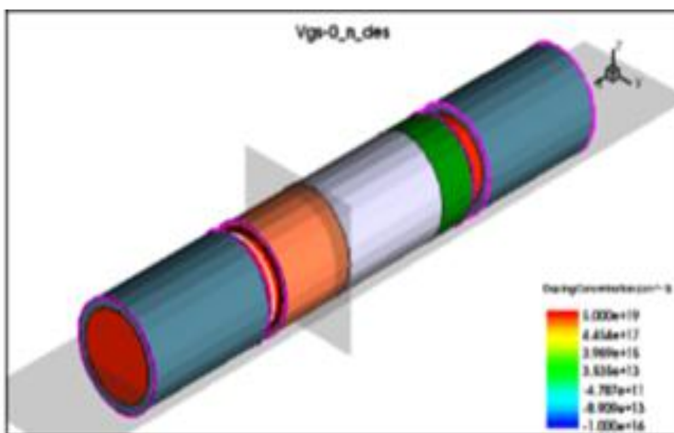

Figure 3: Simulated structure of gate all around nanowire FET with triple material gate

In the proposed structure a cylindrical channel ended with source and drain regions is designed. The channel region is covered with a gate oxide which is covered with gate region.

The gate region is made of three materials. The work functions for the gate material are selected as 4.4eV for gate1, 4.8 eV for gate 2 and 4.6 eV for gate 3. The work functions of the metal gate has direct impact on the potential and lateral electric field over the channel.

Low band gap materials such as germanium and silicon-germanium is used as source & drain materials respectively [4]. Silicon is utilized as the channel material. The source and drain regions are doped with n-type material of doping concentration. The dimensions of the device is given in the following table.

Table 1: Device Dimensions

Region	Material	Doping/work function	Length/Thickness
Source	Germanium	5e19	40 nm
Drain	Si-Ge	5e19	40 nm
Intrinsic	Si	1e16	60 nm
Gate 1	Silver	4.4	10 nm
Gate 2	Tungsten	4.8	30 nm
Gate	Copper	4.6	20 nm
Oxide	SiO2	-	60 nm

The proposed device is designed on Sentaurus Device Editor (SDE) and the simulation results for the structure is obtained on Sentaurus Visual.

The mobility model used here is high field saturation. For recombination SRH-Auger model is utilized.

RESULTS AND DISCUSSIONS

The 2D cross sectional view of the simulated gate all around nanowire FET with triple material gate is shown in the figure 4.

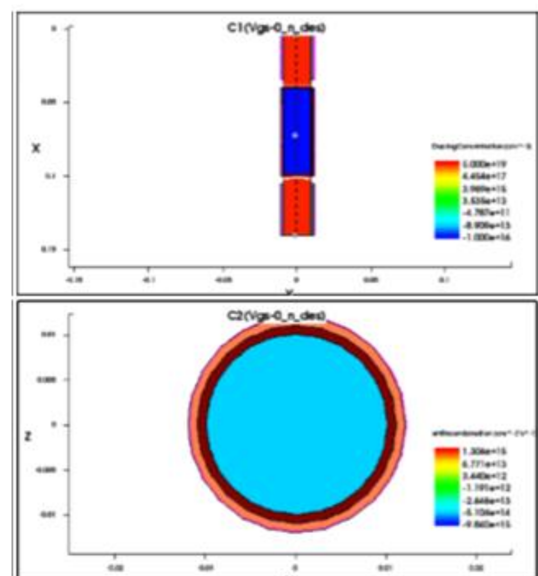

Figure 4: 2D Cross sectional view of TMG GAA NWFET

The energy band diagram of the triple material gate GAA NWFET is shown in figure below.

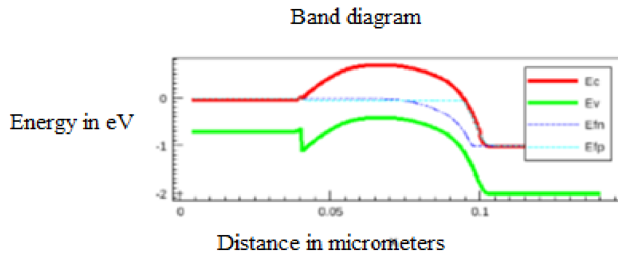

Figure 5: Energy band diagram of TMG GAA NW FET

The DIBL (Drain Induced Barrier Lowering) of single material gate, double material gate and triple material gate structures are compared in the following table. Here DIBL is measured as the threshold voltage variation when drain voltage is varied from 0.1 to 1V. DIBL is lower for triple material gate structure. It is because the M1 region is screened from drain voltage variation by M2 and M3 regions.

Table 2. Comparison of DIBL

Structure	DIBL(mV/V)
Triple material gate structure	20.6
Double material gate structure	22.7
Single material gate structure	46.1

Figure 6 shows the electrostatic potential of the simulated device.

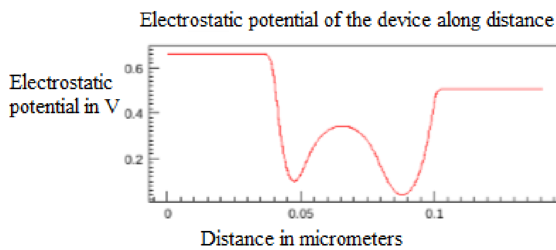

Figure 6: Electrostatic potential of TMG GAA NWFET.

Also on closer inspection of electric field of triple gate structure, the electric field is lower near the drain end. This suppresses the hot carrier effect.

The following figure gives the variation of drain current with respect to gate voltage.

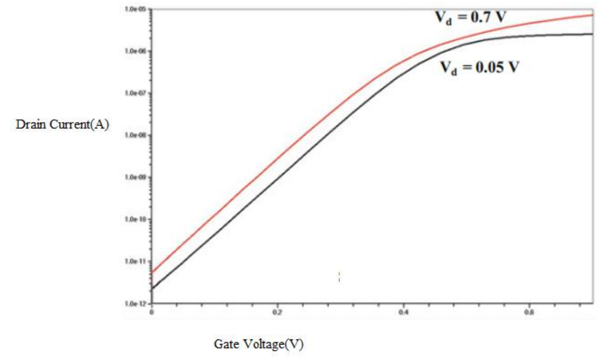

Figure 7: Transfer characteristics

Also the dc gain of single gate, double gate and triple gate structures have been compared in the following table.

Table 3: Comparison of dc gain

Structure	DC gain(dB)
Triple material gate structure	25.51
Double material gate structure	24.62
Single material gate structure	15.54

CONCLUSIONS

A triple material gate in gate all around nanowire FET structure is proposed in this paper. Based on the simulation results it is found that due to the presence of three different materials with different work functions the device shows reduced DIBL and hot carrier effect thereby increasing its reliability. Also the dc gain of such a device is found to be higher than conventional structures. Further improvement in the device can be done by changing the work functions of the gate material and also by changing the length ratios of gate regions.

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