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Optimal Performance Tunnel FET for Low Power Applications

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Abstract

'Compact', 'Complex' and 'Cost effective' are the three important 'C's in today's electronics era. Scaling down of devices is occurring at an exponentially fast rate resulting in increased integration density of chip which brings about unprecedented complexities in the fabrication process. The conventional device structures are not able to withstand the miniaturization of dimensions due to a number of limitations like increase in power consumption, leakage current, subthreshold swing, short channel effects etc. The Tunnel FET is a very efficient solution to the problems and can be used for low power applications. Band gap engineering is considered so as to increase drain current at the same time reducing leakage current. The Si-Ge TFET is found to be insensitive to temperature and there is an improvement in on current. The simulation tool used is Sentaurus TCAD with the help of which output characteristic, energy band diagram and various parameters like electric field, electrostatic potential, current density and lattice temperature are obtained.

Keywords: Electric field, electrostatic potential, current density, lattice temperature

I. INTRODUCTION

It becomes highly essential to reduce the power consumption of the electronic circuits. [1]. Researchers are finding new device architecture and new materials to replace or modify the present technology thus improving its complexity and frequency. The industry is getting ready for the post silicon era with emerging materials such as III-V compounds and carbon and a number of innovative de vice architectures. The TFET is considered to be a low power device and offers steep subthreshold slope, and allows threshold voltage and V_{DD} scaling beyond CMOS limits. As the density of devices keeps increasing, the operating voltage has to be lowered down proportionally to make the power consumption per unit area constant. The thermionic emission of carriers over a channel barrier, has imposed fundamental limits on voltage scaling and reduction of power dissipation. The operating voltage can be controlled by the subthreshold swing (SS). TFET device simulated here uses a doping less Si-Ge material as source and drain and Si as channel.

The various disadvantages of TFET like very low on/off current ratio and low on current due to less sensitivity to electric field as potential between channel and source increases[3]. Here lower bandgap material Si-Ge is used as source and drain so as to improve on current. Also doping less materials are taken so as to reduce the random dopant fluctuations (RDF) to reduce the off current.

II. TFET STRUCTURE AND WORKING

The TFET is a transistor which obeys the principle of electron band to band tunneling. It can act as a switch in on and off conditions at lower voltages compared to that of MOSFET, so TFET can be used in low power consumption of electronic devices for large scale integrated circuits. The current through the tunnel FET is smaller than the current through the MOSFET and has been an issue for practical tunnel FETs. The tunnel FET with the new architecture uses a new channel and electrode structure to allow a higher electric field to be applied at a specific gate voltage. The developed tunnel FET is expected to help to reduce the power consumption of large-scale integrated circuits (LSIs). A major challenge in TFET is to achieve a reasonable on current.

When a gate voltage is applied to the gate electrode of a tunnel FET, the width of the barrier between the source and the channel decreases owing to the effect of the electric field. As a result, the electrons pass through the barrier because of the tunneling effect and current flows through the transistor. Based on this principle, the tunnel FET can switch the current on and off at a lower voltage than that of conventional MOSFETs. The very fast switching of the tunnel FET enables design of low-power electronic circuits that can operate at lower voltages.

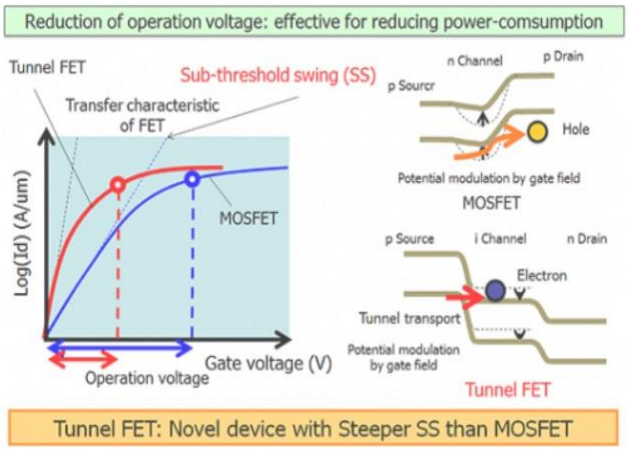

Fig 1. VI characteristic of TFET and MOSFET with respect to the tunneling phenomenon [12]

Fig.1 shows the comparison in the VI characteristics of the TFET and MOSFET devices. The transfer characteristics show a sub-60 SS. The value of drain current is much smaller than the expected to compete with the CMOS technology. The application of positive gate source voltage pulls down the channel band profile that increases the charge carrier concentration in the channel region. Initially, no BTBT take place across the source channel junction and the drain source current remains very small. As the gate source voltage pulls down the channel conduction band below the source valence band BTBT starts across the source channel junction a sharp increase in current is observed. Any further increase in gate source voltage continues pulling down the channel conduction band, until it aligns with the drain conduction band. As a result, the SS of TFETs increases with gate source voltage.

In this work Source and Drain are uniformly doped n type and p type materials Si-Ge and the channel is Si. The Si-Ge material is of supreme quality and the energy band gap lineup at the heterointerface is determined by the strain. The Si-Ge films are more stable thermally and can be grown without the danger of dislocations. The expected performance enhancement comes from the lighter effective mass, reduced interval scattering and the possibility of having a better heterointerface than that between SiO2 and Si (amorphous crystalline interface). This results in improved carrier mobility and transconductance.

III. SIMULATION AND RESULTS

A. Simulation Technology

The two-dimensional device simulation is performed using the simulation tool TCAD (Technology Computer Aided Design) Sentaurus from Synopsis Corporation. It is used for simulating both heterostructure and homostructure devices. Advanced physical models and robust numerical methods are used for simulating the electrical behavior of semiconductor devices. The device simulation helps in understanding the physical processes occurring in the device structure and the underlying physics behind them. This will help in enhancing the performance of new generation devices. Sentaurus device simulates the structure and output can be visualized using SVisual tool. Conditions can be changed and the interiors can be visualized using this tool. The Hydrodynamic model is more accurate than Drift Diffusion model, since DD model is incapable of reproducing the velocity overshoot effects, often observed in III-V semiconductor devices with sub-micron gate lengths. The effect of hot electrons is not taken into account while solving for electron and hole current densities. Moreover, it often overestimates the effect of impact ionization. Therefore, for sub-micron devices and with short gate lengths, Drift Diffusion model shows some discrepancies and the Hydrodynamic model may be more appropriate.

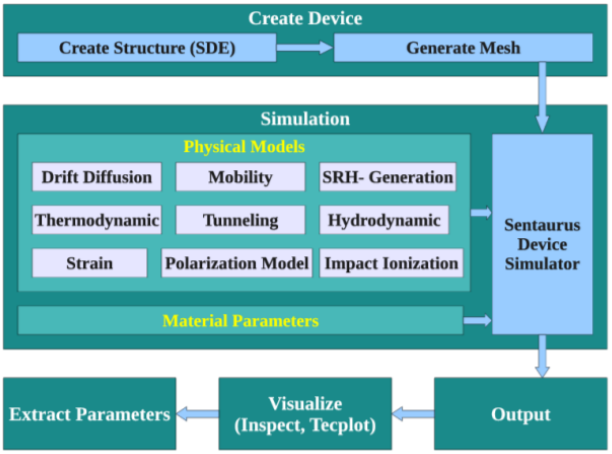

Fig 2: TCAD Sentaurus Physical Simulation methodology [7]

B. Simulation Results

A proper, accurate model for device of interest is crucial to help in producing the necessary evaluation and projection of the final device performance. The model of TFET in Fig.3 is simulated using the TCAD Sentaurus simulation tool. The output characteristic, VI characteristic and band diagram of TFET is being obtained as shown in Fig.4 and its performance is compared with Si TFET. It is observed that the band gap is narrowed further due to the undoped Si-Ge material used in the source-drain regions.

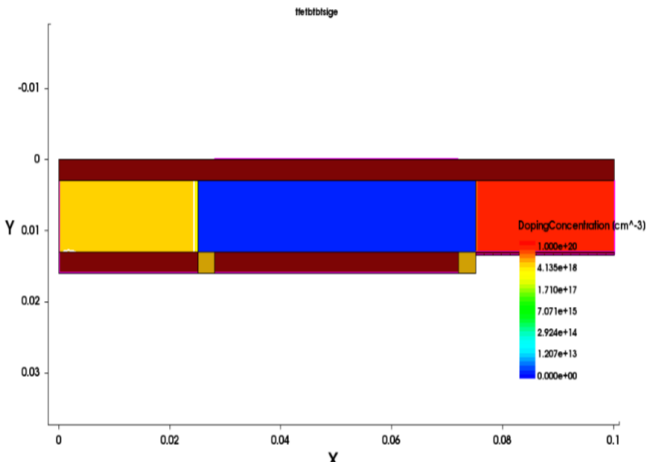

Fig 3: Structure of TFET with Doping concentration gradient

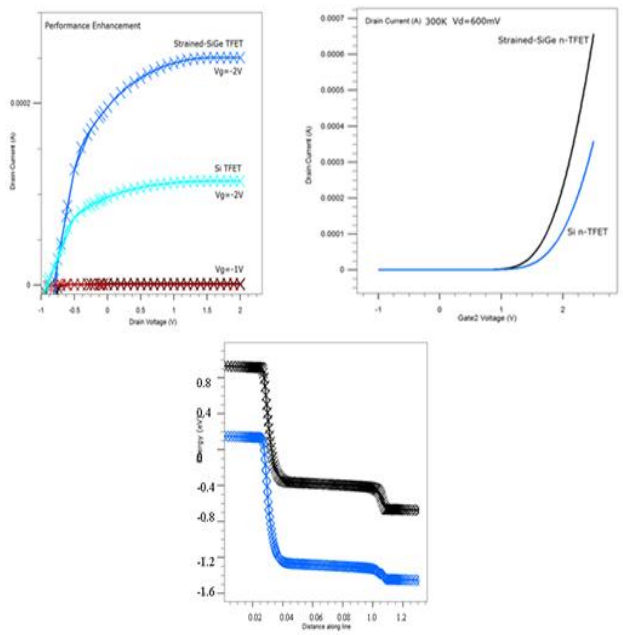

Fig 4. Drain Characteristic, Transfer Characteristic and Energy Band Diagram of Si-Ge TFET

There is an excellent increase in drain current with change in gate source voltage. The leakage current is also reduced which results in better Ion/Ioff ratio.

Four parameters taken into consideration are the electric field, electrostatic potential, lattice temperature and electron current density. The simulated results are obtained along the length of the device. It is inferred that there is an increase in electron current density, electric field and electrostatic potential in the channel near the source. The Si-Ge material has an energy band gap smaller than Si and controllable by varying the Ge content. Band gap engineering is made possible which has a tremendous impact on the on current.

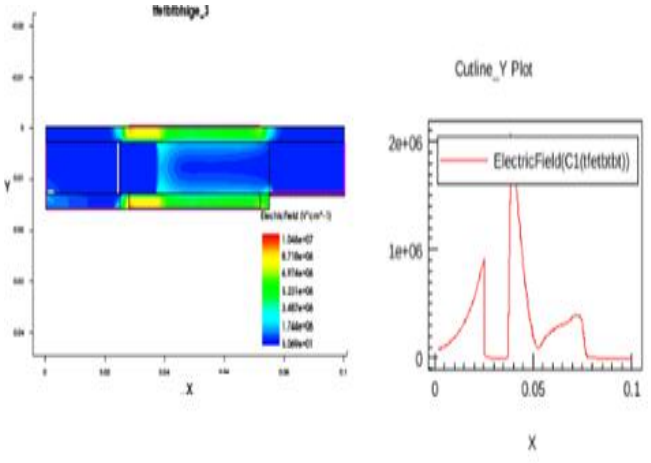

Fig 5: Variation of Electric Field along the length of TFET device

The gate control over the channel increases so that electric field intensity is maintained high as in Fig.5.The tunneling probability is calculated as a function of this parameter. The average subthreshold slope decreases as bandgap decreases.

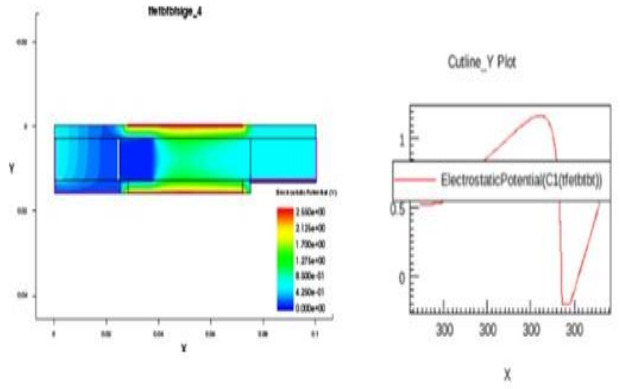

Fig 6: Variation of Electrostatic potential along the length of TFET device

The electrostatic potential of the device in Fig.6 is found to gradually increase towards the drain region and take a steep dip towards the drain junction.

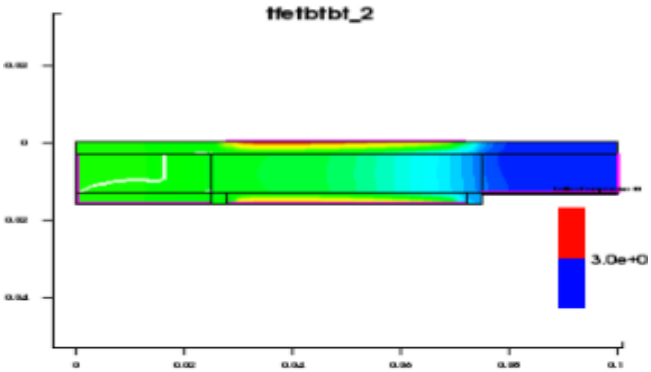

Fig 7: Variation of Lattice temperature along the length of device

The lattice temperature is observed to be concentrated towards the contacts. TFET is capable of working over wide range of temperature without much variation in performance.

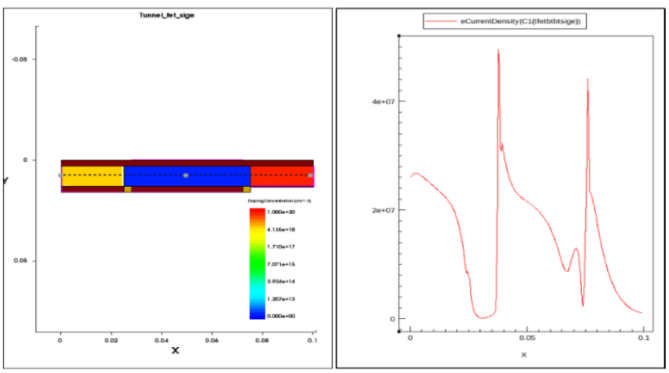

Fig 8: Electron current density variation along the length of device

The Electron current density increases to peak values which results in increase in drain current as in Fig.8. Thus, at low voltages the tunnel FET is an assured candidate which provides a good increase in current.

IV. CONCLUSION

Conventional MOSFETs are getting replaced by more novel devices like the Tunnel FET as it can be used for low powered applications, has low subthreshold swing and low off state leakage current. The TFET still has a few drawbacks like low on state current and RDF effects. The Doping less Si-Ge TFET considered here can overcome these disadvantages and also improve on current and eliminates the high temperature doping and annealing processes during its fabrication. The Ion/off ratio can be improved. The TFET is also found to be insensitive to temperature variations from the lattice temperature profile.

The proposed structure has the advantages of heterojunction material. The on-state current can be improved by using smaller band gap material in the source and drain side. The operation voltage of the device can be reduced to below 0.5V and drain current has performance improvement of above 200%. Further improvements can be obtained by using heterojunction of III – V compounds as materials.

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