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A Simple and Novel scheme of LC-VCO for Ultra Low power Low phase Noise Applications

Karim Zouaq, Abdelmalik Bouyahyaoui, Mustapha Alami and Abdelhamid Aitoumeri
STRS Lab. Institut National des Postes et Telecommunications, INPT
10112 Rabat, Morocco.

Abstract: This paper presents a simple and novel scheme of the ultra-low power low-phase noise LC-VCO (Voltage Controlled Oscillator) designed in 130 nm CMOS technology. The architecture of this VCO combines a simple cross-coupled differential structure (N-pair) biased in weak inversion (WI) or Subthreshold regime, and a PMOS tail current source biased in strong inversion (SI) or in superthreshold regime. This VCO topology demonstrates a good performance and the ability to ensure the required robustness even while working in the worst conditions. The proposed VCO demonstrates a tuning range of 7.26–6.69 GHz (8.17%) with only 63.22 μW power consumption from 0.4 V dc supply. The phase noise in the worst case is -51.76 dBc/Hz at 1 kHz and -124.3 dBc/Hz at 1 MHz, respectively.

Keywords: Phase noise, low power, Voltage Controlled Oscillator (VCO), weak Inversion (WI), worst conditions.

INTRODUCTION

There is an emerging set of applications for which energy consumption and phase noise are the key metric, the explosive growth in wireless communication has led to an increased demand for wireless products that are low-cost, ultra-low power, and compact in size. In recent years, The LC-VCO design for low power and low phase noise applications, has become a major research area and actually a lot of researches focus on improving VCO structures. Therefore, many recent works have proposed different techniques to reduce power consumption and phase noise. Using current reuse configuration [1, 2] and reducing supply voltage [3] are the two popular techniques in the literature. Weak Inversion behavior described by E. Vittoz [4] demonstrates that it is possible to take advantage of this regime in designating analog CMOS circuits.

The fact that VCO is trade-offs among power consumption, phase noise, and chip area [5], it should be interesting to operate VCO or some parts of VCO in the Weak Inversion region. In fact, Designing CMOS LC VCO in Weak Inversion region offers many features that can be exploited to minimize the offset and the noise of differential pairs, with the additional advantage of minimum saturation voltage [6]. Generaly, it has ben proofed that the subthreshold CMOS transistors exhibit higher transconductance and comparable phase noise performance with the superthreshold [7]. However, subthreshold operation is less robust to transistor mismatches, power-supply noise, and temperature, issues that must be addressed via appropriate architectural and biasing techniques to ensure the required robustness even while working in the worst conditions. Biasing must never be used in subthreshold operation, where there is exponential sensitivity to temperature and voltage. Robust biasing techniques for subthreshold operation that are insensitive to temperature variations and power-supply noise are required [7]. In this work, a simple 0.4 Volt LC VCO structure is proposed, The circuit uses a classical subthreshold NMOS cross-coupled (N-Pair) to enhance the negative resistance, a PMOS transistor biased in superthreshold region (Saturation regime) and sized to flow a strong current sufficiently insensitive to variations of the voltage and the temperature, then to ensure the required

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robustness even while working in the worst conditions. In addition a LC tank with a high quality factor is implemented in the same chip.

The remaining part of this paper is organized as follow: Section I presents the Weak Inversion regime and its advantage in LC-VCO design, Section III describes both the designing considerations of the proposed VCO and the simulated results. Finally, the conclusions are drawn in Section V.

WEAK INVERSION REGIME AND BENEFITS

The subthreshold region of operation is present in a transistor when it is operated below its threshold voltage and where the bandwidth available per ampere of current consumed in the transistor is maximal with the ability to use small power-supply voltages, the bandwidth per watt of power consumed in the transistor is maximized in its subthreshold regime. Consequently, subthreshold operation is the most power efficient regime of operation in a transistor [7]. The drain current in weak inversion can be approximated by (1):

$$I_{ds} = e^{\left(\frac{V_{gs}-V_{th}}{nU_t}\right)}\left(1 - e^{\frac{V_{ds}}{U_t}}\right) \tag{1}$$

Formula (1) is the classic gate-referenced equation for subthreshold operation, revealing the exponential relationship between the current and V_{gs}, and also the exponential dependence of the current on U_t andV_{th}. n is termed the subthreshold slope coefficient, defined by (2):

$$\frac{1}{n} = \frac{C_{ox}}{C_{ox} + C_{dep}} \tag{2}$$

where C_{ox} and C_{dep} are the gate oxide capacitor and the surface depletion capacitor respectively. U_t is the thermal voltage, V_{gs} and V_{ds} are the gate to source and drain to source voltages respectively. I_{ds} is termed the specific current, which is given by (3)

$$I_{ds} = C_{ox}\mu\left(\frac{W}{L}\right)(n-1)U_t^2 \tag{3}$$

$$\frac{g_m}{I_{ds}} = \frac{1}{nU_t} \tag{4}$$

The transconductance to current ratio defined by equation (4) is an important metric for determining the speed available for a given level of power consumption and it is maximal and constant in weak inversion. As the most of VCO designers uses the cross-coupled architecture (PMOS pair and/or NMOS pair) to generate the negative resistance, it is very important to know that the differential pairs are preferably operated in or close to weak inversion, the most benefit is that their equivalent input noise and their offset are both minimized in this mode of operation. Thus the equivalent noise resistance of the MOSFET [6] is given by (5):

$$R_N = \frac{\rho}{WLf} + \frac{\gamma}{g_m} \tag{5}$$

where f is termed the frequency and WL is the channel area, the parameter ρ depends on the process and on the gate oxide capacitance, γ is the thermal noise excess factor. The first term represents the flicker noise component generated at the surface of the device and the second term is the channel noise component that is inversely proportional to gm. For a given drain current, this component of equivalent input voltage noise density is thus minimum in weak inversion, consequently this feature contribute to minimizes the spectral density of the total output current noise in the circuit. Thus, low current requirements limit the use of resistors, reduce speed and bandwidth and increase the noise voltage spectral densities. However, the possibility of operating transistors in weak inversion helps to counter these limitations, the very low value of saturation voltage permits peak-to peak amplitudes close to the supply voltage and the maximum value of transconductance-to-current ratio provides a large DC gain per stage, as well as minimum noise for a given current. As consequence. The well controlled exponential characteristics permit interesting analog sub-circuits [8].

DESIGN CONSIDERATIONS

Design under normal conditions

Figure 1 shows the circuit schematic for the proposed LC VCO. A subthreshold NMOS cross-coupled (differential N pair) topology was used to reduce the voltage headroom and the power dissipation. A simple PMOS transistor biased in superthreshold region is used as tail current source and sized to make the whole circuit sufficiently insensitive to PVT variations, the PMOS body is connected to V+ output in order to minimize the power dissipation and makes possible the oscillation start-up of the VCO. The

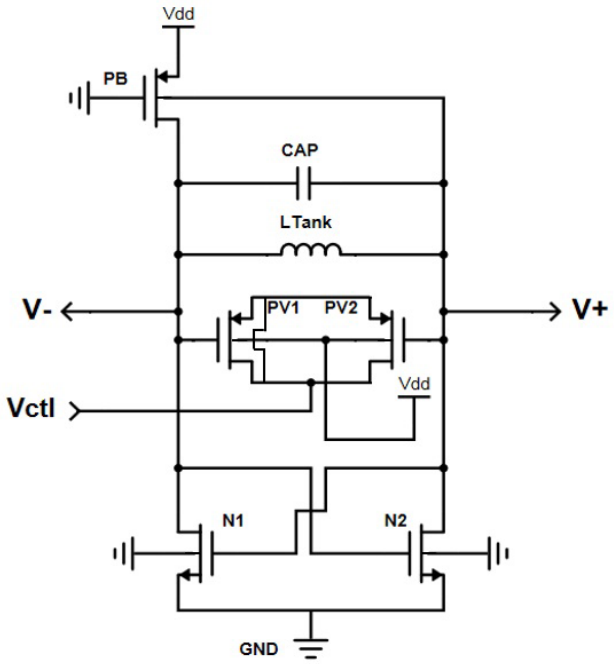

FIGURE 1. Proposed Oscillator.

proposed VCO design strategy (V+ and V- are the end outputs of this VCO, Fig 2. shows theirs waveforms) consists on the minimization of both phase noise and power consumption by using the minimum of components. The design methodology starts with optimization of the LC-tank by maximizing the corresponding quality factor Q and minimizing resistive losses. In fact, a spiral inductor with large track width and minimum number of turns is chosen to ensure the lower resistance and higher quality factor, regarding the active elements, the multi-finger transistors are employed to decrease the gate resistance R_g, which influences the noise performance of MOSFETs.As tuning range, the PMOS varactor (I-MOS structure) is used for the proposed VCO resonator in order to achieve the lower phase noise. In fact, minimizing both power consumption and phase noise is performed under a certain tuning range constraints. The fig. 3 shows the evolution of power dissipation and phase noise when varying the tuning voltage V_{ctrl} from zero to 1 Volt.

The table I summarizes all significant results of the proposed VCO. Therefore, the oscillation frequency can be tuned from 7.26 to 6.69 GHz when varying the tuning voltage V_{ctrl} from zero to 1 Volt, so that the frequency tuning range is about 8.17%. The achieved phase noise is −127.3 dBc/Hz at 1MHz offset as shown in Fig. 4.The total power consumption is only 63.22 W with 0.4 Volt supply voltage.

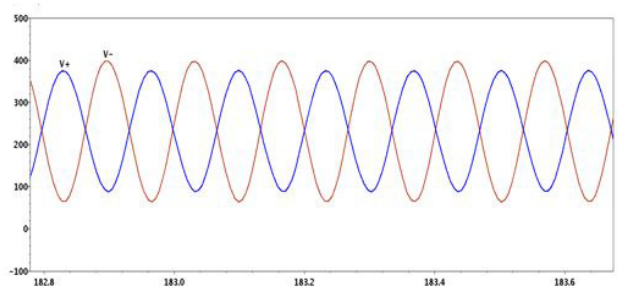

FIGURE 2. VCO single end output waveform at V_{ctl} = 0 V.

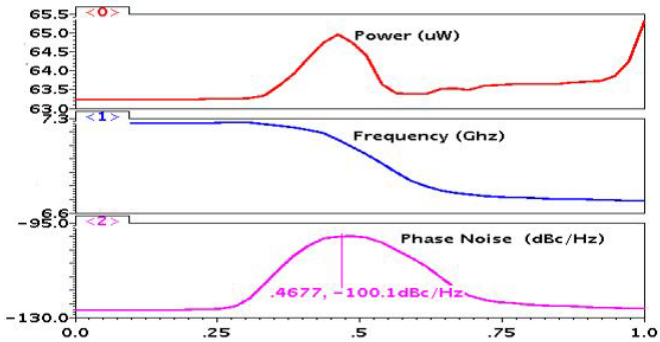

FIGURE 3. VCO outputs variations with tuning range: $< 0 >$ Power,$< 1 >$ Frequency, $< 2 >$ Phase noise.

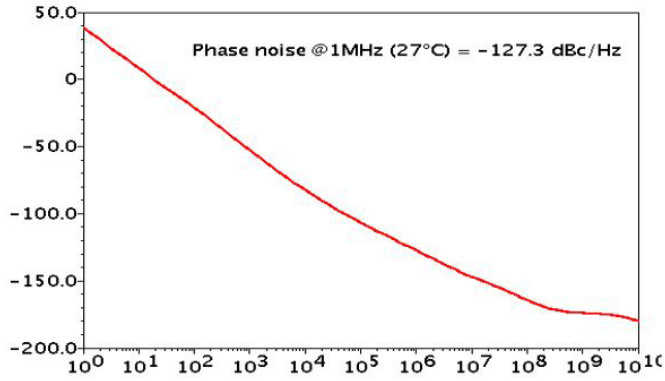

FIGURE 4. Phase noise waveform of the designed VCO.

Figure 5 shows the layout shot of the proposed chip, and can be seen the die size that is 299 µm by 238.4 µm without pads.

Design under PVT variations

PVT-independent biasing is crucial for robust operation in subthreshold circuits where currents have an exponential sensitivity to temperature. The proposed design demonstrates an acceptable immunity to PVT variations while

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Table 1. Simulation results.

Characteristics	This Work
Voltage (V)	0.4
Frequency (GHz)	7.259
Peak to peak (mV)	330
Tuning Range (%)	8.17
Power (Î¼W)	63.22
Phase Noise@1Mhz(dBc/Hz)	−127.3
FOM (dBc/Hz)	−216.90
FOMt (dBc/Hz)	−218.65
Setup time(ns)	70.65

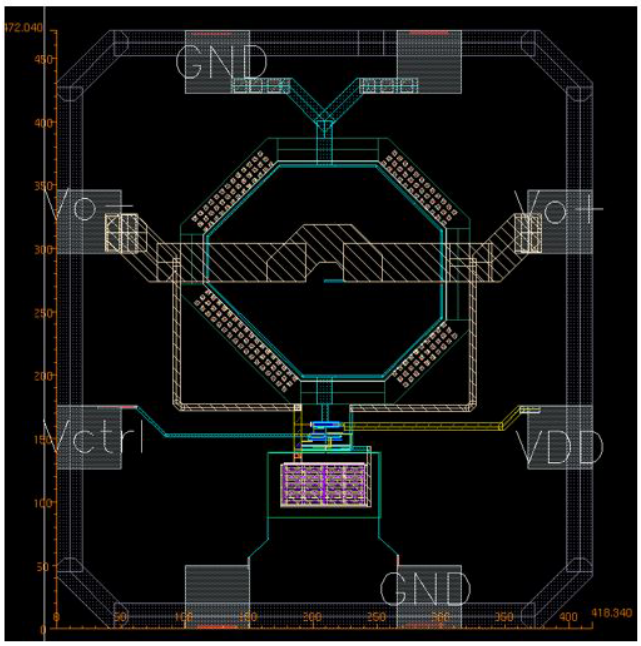

FIGURE 5. Annotated layout of the proposed VCO.

using only a simple PMOS transistor operating in saturation region and without any supplement circuit that possibly causes degradation of circuit performance (Power and Phase noise) , and uses more chip area. Therefore, to demonstrate this robustness. Three corners have been defined using ADE XL tools:

- Best case: combines a Fast-Fast process, high V_{dd} and a low temperature (ff, 0.4V, −40 °C).
- Worst case: combines a slow-slow process, low V_{dd} and a high temperature (ss, 0.36V, 125 °C).
- Typical case: lies between these two extremes (tt, 0.4V, 27 °C).

Table II summarizes the obtained simulation results and the percentages of variation of the three given corners. As result, the oscillation is preserved in the whole studied

Table 2. VCO responses to PVT variations.

	tt (0.4v,27°C)	ss (0.36v,125°C)	ff (0.44v, −44°C)
Frequency (GHz)	7.259	7.278 (0.26 %)	7.197 (0.85%)
Peak to peak (mV)	330	323 (2.12 %)	287 (13 %)
Power (W)	63.22	74.9 (18.47 %)	58.31 (7.76%)
Phase Noise @1MHz (dBc/Hz)	−127.3	−124.3 (2.35%)	−127.4 (0.07%)

cases. In the worst case, the frequency, the power consumption and the phase noise have been changed by 0.26 %, 18.47 % and 2.35 % respectively compared to the typical condition. In the best case, the obtained variations in term of phase noise performance, frequency oscillation and power dissipation are equal to only 0.07%, 0.26 % and 13 % respectively compared to the typical condition. Therefore, these results shows that the proposed circuit is insensitive to PVT (Process, Voltage, and Temperature) variations.

Results evaluation

The VCO design can be evaluated using FOM (Figure of Merit) and FOM$_t$ parameters as follow:

$$FOM = L\{\Delta f\} + 10log(PDC(mV)) - 20log\left(\frac{F_{osc}}{F_{offset}}\right) \quad (6)$$

$$FOM_t = FOM - 20log\left(\frac{TR(\%)}{10}\right) \quad (7)$$

where TR (%) is termed the tuning range defined as follow:

$$TR(\%) = \left(\frac{F_{min} - F_{max}}{F_{min} + F_{max}}\right) * 200 \quad (8)$$

and $L\{\Delta f\}$ is termed the phase noise at the offset frequency F_{offset} from the oscillation frequency F_{osc}. PDC is the core DC power consumption in mW. The FOM and FOM_t of the proposed VCO is −216.90 dBc/Hz and −218.65 dBc/Hz respectively.

The Table III compares the proposed VCO performance with some recently published works. It is clear from the table that our proposed VCO is demonstrating a good performance in terms of power and phase noise. Even our design focus on ultra-low power applications, that use low voltage as supply, we tried to show several works, despite

Table 3. VCO performance comparison with other published works.

Design	Ref.	Voltage(V)	Power (μW)	TR(%)	Phase Noise@1Mhz(dBc/hz)	Frequency(Ghz)	FOM(dBc/hz)	$FOM_t(dBc/hz)$
This work	**130nm**	**0.4**	**63.22**	**8.17**	**-127.3**	**-216.90**	**7.259**	**-218.65**
[3]	180 nm	0.45	430	8	−105.9@400KHz	2.63	−185.9	−183.96
[9]	180 nm	0.8	230	11.3	−118.3	2.5	−192.6	−193.7
[10]	180 nm	1.1	5880	96.94	−115.87	2.389	−175.8	−194.73
[11]	180 nm	0.6	63.6	7.26	−114.1	2.495	−194	−191.2
[12]	180 nm	0.46	346	7.5	−107.8	10.94	−193.8	−193.8
[13]	180 nm	0.5	730	20	−117	2.41	−186	−192
[13]	180 nm	0.43	465	20	−115.6	2.41	−186.5	192.5
[14]	180 nm	0.5	660	18	−120	2.65	−189.9	−195
[15]	65nm	1	5600	-	−128	3.5	−191.4	-

the fact that the designers have used more voltage and power to achieve to desired performances, it is seem that our design remains better, and even while working in the worst conditions. However, this design presents an asymmetry of VCO single end output waveforms. In fact, there is a small mismatch between V+ and V−, caused by the single PMOS tail source that flows the current to the cross coupled structure.

CONCLUSION

In this paper, a design for an Ultra-low power and low phase noise 7.26 GHz LC-VCO been proposed, this VCO uses a N-pair cross coupled CMOS as transconductance generator, and it is biased with only a single PMOS transistor operating in saturation regime. The whole circuit consumes only 63.22 μW under 0.4 V. The simulation results shows that the proposed VCO is insensitive to environmental variations and can be used even while working in the worst conditions. This VCO topology has been implemented using 0.13 um CMOS technology, it operates a frequency tuning from 7.26 GHz to 6.69 GHz by varying the value of the supply voltage from 0 to 1Volt, this design can achieve −218.65 dBc/Hz as FOM_t value.

Since the results obtained for the design are very encouraging, and the biasing with a simple PMOS operating in Strong inversion gives a certain immunity to PVT variations, it should be interesting to design a PVT-independent biasing circuit in order to obtain a very high immunity to temperature, supply and process and prevent any limitations in terms of robustness. The proposed design would be useful in many wireless communications, where high sensitivity, low phase noise, low power, and differential operation are needed, such as those for GSM, Bluetooth, and 802.11g applications.

REFERENCES

[1] J. Jung, et al., June 2011, “Compact sub-1mW low phase noise CMOS LC-VCO based on power reduction technique”, Microwave Symposium Digest (MTT), IEEE MTT-S International, pp. 1–4.

[2] Chin-Lung Yang and Yi-Chyun Chiang., 2008, “Low Phase-Noise and Low-Power CMOS VCO Constructed in Current-Reused Configuration”, IEEE microwave and wireless components letters, vol. 18, no. 2.

[3] Hanil Lee, Saeed Mohammad, 2007, “A Subthreshold Low Phase Noise CMOS LC VCO for Ultra Low Power Applications,” IEEE microwave and wireless components letters, vol. 17, no. 11, pp. 796–798.

[4] E. Vittoz, 1977 and 1978, “LSI in watches,” Solid-State Circuits, Ed. Journal de Physique, pp. 14–20.

[5] R. L. Bunch, and S. Raman, 2003, “Large-signal Analysis of MOS Varactors in CMOS -Gm LC VCOs,” IEEE Journal of Solid-State Circuits, vol. 38, pp. 1325–1332.

[6] Alice Wang, Benton H. Calhoun Anantha, P. Chandrakasan, 2006, “Sub-threshold Design for Ultra Low-Power Systems,” Springer Science+Business Media, LLC.

[7] Rahul Sarpeshkar, 2006, “Ultra low power bioelectronics: fundamentals, biomedical applications, and bio-inspired systems,” p. cm. ISBN 978-0-521-85727-7 (hardback).

[8] E. Vittoz, 1994 “Micropower techniques,” researchgate 234783317.

[9] Deng Xiaoyinga, Lin Xin and Zhu Mingcheng, 2017, “A 0.23 mW self-biased current-reuse CMOS LC-VCO based on novel interposed network,” IEICE Electronics Express.

[10] S.L. Jang, C.C. Wang and M.H. Juang, 2017, “Dual-resonance concurrent oscillator,” Micro-electronics Reliability.

[11] I. Ghorbel, F. Haddad, and W. Rahajandraibe, 2015, “Ultra Low Power RF Cross-Coupled VCO Design in the Subthreshold Regime with High Immunity to PVT Variations in 130nm CMOS Technology,” New Circuits and Systems Conference (NEWCAS), IEEE 13th

International Conference.

[12] D. Fathi and A.G. Nejad, 2013, "Ultra low power, low phase noise 10 Ghz LC VCO in the subthreshold regime," SciRes, Circuits and systems, 4, 350–355.

[13] Dongmin Park, SeongHwan Cho., April 2009, "Design Techniques for theory and Techniques," IEEE Transactions on, vol. 57, no. 4, pp. 767–774.

[14] E. A. Vittoz, June 1985, "The Design of High-Performance Analog Circuits on Digital CMOS Chips," IEEE Journal of Solid-State Circuits, vol. 20, no. 3, pp. 657–665.

[15] N.-J. Oh, 2014, "A phase-noise reduction technique for RF CMOS voltage-controlled oscillator with a series LC resonator," Microelectron. J., vol. 45, no. 4, pp. 435–440.