Wideband Spectrum Analyzer with Hardware Accelerated Kernel Function Modulation

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Abstract

The article considers an original way of constructing a digital signal processing system based on modulated harmonic functions. Instead of a table representation, the architecture of a hardware generator of transcendental functions modulated by the Gaussian function is proposed. This allows you to flexibly control the behavior of the convolution kernel in the frequency and time domains. The implementation of the method based on Xilinx FPGA.

Keywords: wavelet, FPGA, spectrum.

INTRODUCTION

Two basic trends in the digital measurement devices may be highlighted. First is a continuous hardening of requirements to precision, bandwidth, measurement rate and other similar parameters of devices. Second is a visible extensive development of microelectronic hardware, which may be used as a hardware platform for measurement systems.

Comparing these trends, it is easy to see there is a well-known mainstream approach based on the intensive usage of digital signal processing (DSP) algorithms for achieving improved parameters of measurement systems. Electronic hardware and DSP algorithms have a mutual influence, leading to dependence between the algorithms used and the effectiveness of the hardware used for its implementation. To optimize the resulting features, such as price/performance and price/precision, designers must use co-optimized architectures in the terms of algorithms and hardware features.

A key feature of DSP hardware is the 'Multiply and Accumulate' (MAC) operation, ideally suited for FIR and IIR filters and Fourier Transform. These algorithms are based on the convolutional operator, described as:

$$S = \int_{t_1}^{t_2} x(t) w(t) dt$$
 (1)

or, in discrete form

$$S = \sum_{i=t_1}^{t_2} x_i w_i \tag{2}$$

where x(t) – analyzing signal,

w(t) – kernel function.

Using harmonic function as kernel, Fourier Transform is performed. For widely used Fast Fourier Transform (FFT) direct representation of the kernel function for different frequencies is replaced by a special set of frequencies, which allows for the significant decreasing of the number of operations. However, fundamental limitations on the frequency set exists for FFT. Also, pure harmonic functions have a significant dependence on the time window.

MODULATED HARMONIC FUNCTION AS A KERNEL

Based on a wavelet analysis approach it is possible to construct set of kernel functions based on a harmonic series, using a modulation function as a window. For example, a Gaussian window is known as a sub-optimal way to a create kernel with a balanced localization in time and frequency domains.

$$w(t) = (\cos\omega t + j \cdot \sin\omega t)e^{-\frac{t^2}{k}}$$
(3)

where k - is a constant for fading control, providing a zerolevel DC component for the kernel function.

A particular case of this kernel is known as a Morlet wavelet function [1, 2]. However, a certain interval in the time domain is usually used for a Morlet wavelet. In this article we describe an approach based on the usage of a matched fading constant and a time window size. The magnitude of the response of a Morlet kernel function for a different interval of a kernel in a time domain is shown on the Fig. 1.



Figure 1. Magnitude response of a Morlet kernel function for a different size of a kernel in a time domain

Analyzing (3), no fast representation for FFT for this kernel is allowed in general. On the other hand, graphics on Fig. 1 show the flexibility of kernel functions constructed with different matched pairs of fading constants and sizes of the time window.

HARDWARE ACCELERATED GENERATION OF KERNEL FUNCTION SAMPLES

Existing hardware platforms, such as FPGA, provides a comprehensive set of building blocks for digital signal processing. With base types of blocks, such as configurable logic cells, block RAM and DSP cells (XtremeDSP or DSP48 in Xilinx FPGA), full implementation of DSP systems may be realized in single digital chip. This also allows for the use of post-processing using embedded processor cores [3, 4, 5].

Equation (3) contains trigonometric and exponential functions, which has no direct implementation on the gate-level logic design. For high sampling frequencies, it may be impossible to store all kernel samples in the on-chip memory. However, an effective algorithm for bit-by-bit calculation is known [6, 7, 8]. This is Coordinate Rotating Interface Computer (CORDIC), which can be used to calculate a pair of sin/cos or hyperbolic sinh/cosh functions. Having a hyperbolic pair of $\cosh(x)$ and $\sinh(x)$ it is possible to calculate exponential functions according to:

$$exp(t) = \cosh(t) - \sinh(t)$$
 (4)

Since the CORDIC algorithm has a limitation for the interval of an argument, the exponent calculation must be improved. This may be done by adding a table representation of the exponential functions for a fixed set of arguments, as described:

$$\{exp(t_1), exp(t_2) \dots \} where t = 0.5 * N,$$
(5)
N - integer coefficient

In this case, the exponent may be calculated as shown below:

$$exp(t_1 + t_2) = exp(t_1) \cdot exp(t_2) \tag{6}$$

where $exp(t_1)$ is calculated by the CORDIC module and $exp(t_2)$ is a table value.

Having two parts of the exponent, it is possible to calculate the modulation coefficient, combining CORDIC IP-core for a fractional part of the argument and the table representation for the integer part of the argument. The structure of IP-core for the accelerator of the kernel function samples is shown on Fig. 2.

International Journal of Applied Engineering Research ISSN 0973-4562 Volume 13, Number 8 (2018) pp. 5605-5608 © Research India Publications. http://www.ripublication.com



Figure 2. Structure of IP-core for accelerator of kernel function samples.

EXPERIMENTAL RESULTS

The approach described above was used in several projects implemented with Xilinx FPGA. These Projects include a spectrum analyzer for software defined radio and precision wideband phase analyzer for high-voltage equipment. An example of passband filter generated by this IP-core is shown on the Fig. 3. It is clear to see a precisely modulated kernel function provide significantly better magnitude in pass-stop intervals and has a smaller level of magnitude oscillations.

With a small-to-medium sized FPGA it is possible to create many independent signal processing datapaths for wideband signal analyzing systems. Since modulation provides passband extension, a smaller count of datapaths compared to FFT processing system is enough to cover a certain bandwidth.





A hardware generator has been designed with VHDL language in Xilinx Vivado IDE and targeting Xilinx series 7 FPGA (Artix-7, Kintex-7, Virtex-7). For 32-bit phase, 24 XtremeDSP hardware blocks are used to provide full datapath for one data processing channel, including kernel function generator and output accumulators for existing or future components. With 240 DSP blocks in low-cost XC7A100T and 840 blocks in medium-sized XC7K325T, used in the reference projects, this approach is an effective way to use embedded FPGA blocks. Implemented devices are measurement units for high-voltage equipment monitoring systems and capable of measuring tangent losses in dielectrics with an error of less than 10⁻⁴ radians in a wide frequency band. This is possible due to highorder hardware generated kernel functions, which provide the required level of noise hardening for DSP subsystems. Total performance for medium-sized FPGA can be more than 120 GMAC/s, that is unobtainable for DSP processors and allows for the building of high-precision and wide-bandwidth measurement devices.

CONCLUSIONS

The presented approach summarizes the experience of building hardware-accelerated generators of kernel functions, using trigonometric and exponential components, which usually requires complex floating-point subsystems. Replacing memory tables with hardware generators, built with the support of FPGA embedded XtremeDSP blocks, it is possible to provide a huge stream of kernel function samples with on-chip modules only. Generated functions can be modulated, with a regulated sample rate and exponential fading, allowing the performance of various kinds of analysis in time-frequency domains.

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