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A Novel Dynamic Scan Low Power Design for Testability Architecture for System-On-Chip Platform

John Bedford Solomon[1], D Jackuline Moni[2] and Y. Amar Babu[3]

[1]Research Scholar, Karunya University, Coimbatore, Tamil Nadu, India.
[2]Professor, Karunya University, Coimbatore, Tamil Nadu, India.
[3]Associate Professor , LBRCE, Mylavaram, Andhra Pradesh, India.

Abstract

Design for Testability and Low power design issues are demanding requirements for System-On-Chip plat form to provide high performance and highly reliable chips. In this paper a novel dynamic scan low power design for testability architecture has been proposed for reducing test power on System-On-Chip platform. The area analysis of proposed architecture for soft core Microblaze based System-On-chip observes 5% reduction of area and test power also reduced by 10% approximately. The area and power analysis of proposed architecture for Microblaze based SoC platform, Picoblaze based SoC platform and Ultrasparc T2 architectures has been observed for optimized area and power design metrics.

Key words: Soft cores -MicroBlaze, PicoBlaze, System-On-Chip, Low power, Design for Testability.

INTRODUCTION

As density of transistors per chip would be double every year according to moore's law, made today's System-On-chip platform more complicated with multiple design metric issues like area, power, speed, test data, test power reduction[1-5]. To analyze the proposed dynamic scan low power design for testability architecture performance, Xilinx soft cores MicroBlaze, PicoBlaze have utilized to build system-on-chip platforms. The MicroBlaze is 32 bit Harvard bus Reduced Instruction Set Computer architecture. It has 32 general purpose registers, 3 operand instruction format. It includes instruction and data caches, 32-bit barrel shifter, hardware divider, fast simplex link FIFO channels, hardware acceleration modules and hardware debug module. The MicroBlaze based SoC platform uses Xilinx microkernel and UART custom peripherals. It also support third party RTOS[6-14]. The MicroBlaze required 525 slices in Spartan-3 FPGA and executes 65 D-MIPS at 80 MHz. The PicoBlaze is a 8 bit RISC core, requires 192 logic cells and 212 macrocells in Spartan-3 FPGA[14], executes 37 MIPS at 74MHz. The Sun Microsystems UltraSPARC T2 microprocessor is also used to study the performance of proposed dynamic scan low power DFT architecture.

The dynamic scan low power DFT architecture has been implemented on above mentioned architectures to analyze area and power analysis. The same SoC platforms were used for analyzing different low power techniques like clock gating, power gating and clock-power gating and scan design test architectures for area and power analysis. The clock gating technique provide power reduction at cost of increases area and also introduces glitches which may cause to malfunctions. The power gating techniques also very useful for power reduction in System-On-chip platform but designer has to analyze in detailed the architectural changes based on application requirements. But this technique also increases area slightly as overhead. By applying both clock gating and power gating, further area and power can be optimized in System-on-chip platform[15-20]. The scan chain based techniques increases area and power but improves controllability and observability. All these low power techniques and test synthesis techniques has been utilized to analyze the performance of dynamic scan low power design for testability technique.

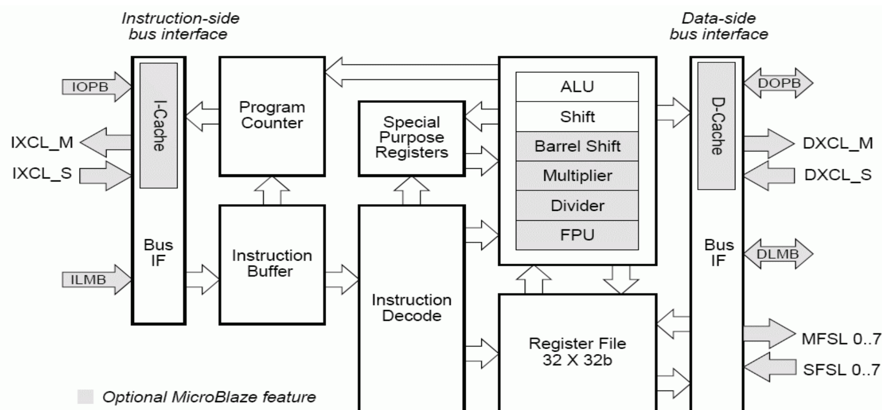

Figure 1: MicroBlaze architecture

RELATED WORK:

The power consumption at system level depends on switching frequency, capacitive load, supply voltage, leakage current, short circuit power. By controlling supply voltage power can reduced, for that multi supply voltages can be used but as technology node shrinks leakage current increases and there by leakage power consumption increases. At system level more power hungry network is clock network, by using various clock synthesis techniques power consumption due to clock network can be reduced. All these low power techniques increases area and there is always area power tradeoff.

To improve the controllability and observability at system level various test techniques have been introduced. The scan chain techniques use extra multiplexers to improve testability[21], but need to choose different scan chains to minimize the test complexity. The test synthesis technique increases area but improves the fault coverage and testability.

The low power techniques, Design for testability techniques both can be applied simultaneously at system level to improve reliability and performance of System-On-chip platform. But design metric area increases by simultaneously applying low power and test techniques. One best solution to minimize the effect is dynamic scan techniques. In this paper dynamic scan cell structure has been introduced and implemented at system level to predict the performance of SoC platform. The test architectures Mirocblaze based SoC platform, PicoBlaze based SoC platform, UltraSparc T2 architectures has been used for area and power analysis of proposed dynamic scan low power design for testability architecture.

DYNAMIC SCAN LOW POWER DESIGN FOR TESTABILITY ARCHITECTURE:

A. Dynamic Scan Cell architecture

In modern System-on-chip platform modules are reused to reduced design complexity. Many of these IP components have their own design for testability. The development of System-On-Chip depends on vendors. Different vendors use different IP cores. So Complexity of design for test increases at system level because of multi vendor IP cores.

By using proposed dynamic scan cell architecture dynamically logic core can be excluded and included during testing time, there by power can be reduced dynamically. The existing low power and DFT techniques can be adapted with dynamic scan DFT technique.

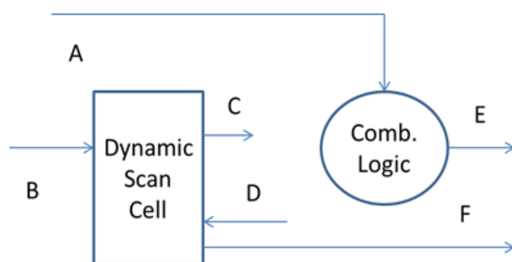

Figure 2: Dynamic Scan Cell

The length of TDR chain reduced by using dynamic scan technique. All low power techniques add area which impact on test time. The low power design techniques tradeoff between area, power and speed.

B. Design Methodology

The design methodology for dynamic scan low power design for testability techniques is as shown in figure. By selecting scan chain to apply dynamic scan chain initiates the design methodology first step. Select partitioned scan chain to insert dynamic scan architecture. This gives modified dynamic scan chain net list then apply ATPG for modified dynamic scan net list. By using dynamic scan chain logic core can be excluded from chain thereby test data size can be reduced and new test pattern are produced. Apply these new test patterns to modified dynamic scan chains and check fault coverage and observe controllability and observability of the test SoC architectures.

If desired reduction in test data is achieved then next scan chain can be select for testing. Otherwise different partition is selected from scan chains to insert dynamic scan design for test technique.

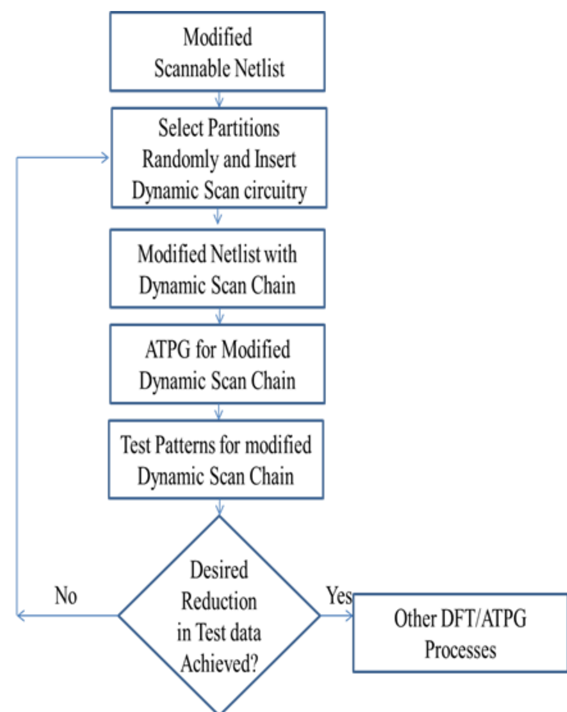

Figure 3: Design Methodology

C. Implementation at System-On-Chip Platform

The proposed dynamic scan low power design for testability implemented for test System-On-Chip platforms as shown in figure3. The test architecture consists of processor core, memory core, IP core, data storage. The required test data is verified using design methodology and used to processor core first then memory core and applied for every core on test system-on-chip architectures. To evaluate the performance of

proposed dynamic scan low power design for testability architectures , three SoC platform have been selected. They are Microblaze based, Picoblaze based SoC platform, ultrasparc T2 architectures.

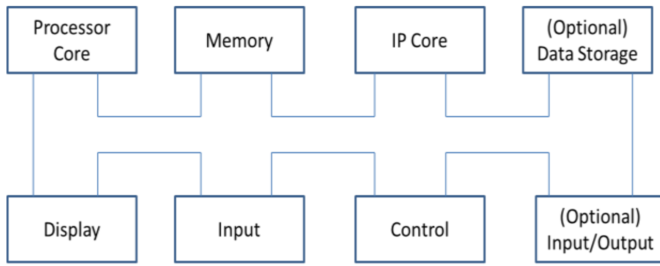

Figure 4: Test Architecture

RESULTS AND DISCUSSION:

The proposed Dynamic Scan Low power Design For Testability architecture evaluated at top level UltraSPARC Chip multiprocessor, Microblaze based SoC platform and PicoBlaze based SoC by sending minimum test data and using minimum test time. Each core evaluated separately for observability and controllability for improved testability. Table 1 shows area tradeoff analysis of DS-LDFT in percentage compared with standard(SD) architecture with low power and DFT techniques, Clock gating(CG), Power gating(PG), scan chain(SC- Multiplexed Flip Flop), scan chain with power and clock gating(PG,CG,SC). Our proposed architecture shows low power consumption with improved testability.

Table 1: Area Analysis of Dynamic Scan Low power DFT

Test Architecture	Clock Gating	Power Gating	Clock Gating + Power Gating	Scan Design	Dynamic Scan DS-LDFT
Micro Blaze based SoC	10	15	25	35	30
Pico Blaze based SoC	15	23	40	38	30
T2-Cores	25	40	60	50	40

Table 2: Power Analysis of Dynamic Scan Low power DFT

Test Architecture	Clock Gating	Power Gating	Clock Gating + Power Gating	Scan Design	Dynamic Scan DS-LDFT
MicroBlaze based SoC	20	18	25	28	10
PicoBlaze based SoC	21	20	23	25	11
T2-Cores	18	18	20	26	15

CONCLUSIONS

To improve the reliability of SoC platform, we need to integrate SoC architecture with low power and design for testability which is very challenging to optimize both power, area and performance. But with our dynamic scan low power design for test architecture we have shown on Microblaze based SoC Platform, PicoBlaze based SoC platform that power consumption can be get reduced by 10% while still maintaining a higher reliability of chip. Further area reduction is reduced by 5%. This work can be further enhanced with network on chip as test architecture.

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