

# An Efficient Reconfigurable Fir Filter based on Twin Precision Multiplier and Low Power Adder

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## Abstract

This paper proposes a low power reconfigurable finite impulse response (FIR) filter using a twin-precision multiplier and a low power carry select adder. The multiplier is capable of performing two independent  $N/2$ -bit multiplications in parallel which reduces the power based on partial products reordering. Reordering of partial products is applied on High Performance Multiplication (HPM). The adder used is the low power and area efficient carry select adder (CSLA). The structure of this adder that there is scope for reducing the area and power consumption in the CSLA. The proposed design has reduced area and power as compared with the regular Reconfigurable FIR Filter. The results analysis shows that the proposed structure is better than the regular FIR structure.

**Keywords:** Low power filter, reconfigurable design, twin precision, HPM, CSLA

## INTRODUCTION

One of the most widely used operations performed in the mobile computing and various multimedia applications is finite impulse response (FIR) filtering. Many efforts for reducing the power consumption of FIR filter is done by the optimization of filter coefficients. FIR filter operations performs the convolution sum and so by minimizing the number of additions and multiplications and accelerating the operations is one of the main goals of this research. The amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we change the filter order by turning off some of multipliers, significant power savings can be achieved. However, performance degradation should be carefully considered when we change the filter order.

Multiplication is one of the most area consuming arithmetic operations in high-performance circuits. As a consequence many research works deal with low power design of high speed multipliers. Multiplication involves two basic operations, the generation of the partial products and their sum. In the fixed point arithmetic of FIR filter, full operand bit-widths of the multiplier outputs is not generally used. In other words, when the bit-widths of data inputs and coefficients are 16, the multiplier generates 32-bit outputs.

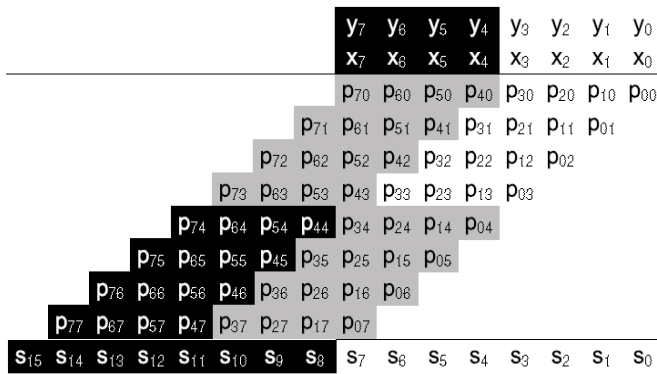
However, considering the circuit area of the following adders, the LSBs of multipliers outputs are usually truncated or rounded off, which incurs quantization errors. When we turn off the multiplier in the FIR filter, if we can carefully select the input and coefficient amplitudes such that the multiplication of those two numbers is as small as the quantization error, filter performance degradation can be made negligible. Several studies has been done on operand bandwidth and it has been shown that for SPECint95 benchmarks more than 50% of the instructions are instructions where both operands are less than or equal to 16 bits. This property was explored to save power, through operand guarding  $n$  which the most significant bits of the operands are not switched and thus power is saved when narrow width operations are computed consecutively. Moreover in this paper we present a reconfigurable FIR filter architecture, where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. In other words, when the data sample multiplied to the coefficient is so small as to mitigate the effect of partial sum in FIR filter, the multiplication operation can be simply canceled. So in effective to the operand guarding using the twin precision technique and the multiplier being turned off when the input coefficients are lower than the threshold, power saving can be done to a large extent compared to the earlier proposed FIR architecture.

Addition operation has been performed in the proposed architecture by the area and power efficient low power carry select adder (CSLA) in place of the normal adder. In the conventional digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. But in CSLA adder the problem of carry propagation delay is done by independently generating multiple carries and then select a carry to generate the sum. It uses a Binary to Excess-1 Converter (BEC) instead of Ripple Carry Adder with  $C_{in} = 1$  in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the  $n$  bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section III.

## LOW POWER MULTIPLIER USING TWIN PRECISION TECHNIQUE USED IN THE PROPOSED FIR FILTER

In twin precision multiplier it is possible to perform two  $N/2$  bit multiplications in parallel in an  $N$  bit multiplier. One  $N/2 \times N/2$  bit multiplication is performed using  $N/2 \times N/2$  bit partial product bits in the least significant part of the multiplier and another  $N/2 \times N/2$  bit multiplication using partial product bits in the most significant part.

Twin precision multiplier mainly operates in three modes namely Full or Double Precision mode (FDP), Dual Single Precision mode (DSP) and Single Precision mode (SP). The FDP mode is used for normal  $N \times N$  multiplications. In this mode nearly 100% of the twin precision circuit is used. In DSP mode, two  $N/2$  multiplications can be performed concurrently. In this mode more than 50% of the circuit is not used. And in SP mode, only one  $N/2$  Multiplication is performed and 75% of the circuit is not used.



**Figure 1.** Partial product representation of an unsigned 8 bit multiplication where a 4-bit multiplication, shown in white, is computed in parallel with a second 4-bit multiplication, shown in black

The illustration of 8-bit unsigned multiplication, by performing two (black and white) 4-bit multiplications in concurrent is given in Fig 1. The white and grey are the important partial products. When performing a 4-bit multiplication in a standard multiplier normally one quarter of the logic cells are performing any useful operations, which is depicted in the grey regions. The twin-precision technique rearranges logic to greatly reduce power dissipation and delay for 4-bit multiplications. Also, this technique allows the logic gates, which are not used in the 4-bit multiplication taking place in the grey region, to perform a second, independent 4-bit multiplication (the black regions). The basic operation of generating a partial product is that of a 1-bit multiplication using a 2-input AND gate, where one of the input signals is one bit of the multiplier and the second input signal is one bit of the multiplicand.

## A. HPM IMPLEMENTATION

To obtain high speed and/or low-power implementations, a logarithmic reduction HPM tree [11] is preferred for summation of the partial products. A logarithmic reduction tree has the advantage that the logic depth is shorter. Further, a logarithmic tree has fewer glitches making it less power dissipating. Regarding the connectivity of cells, a triangular reduction tree is preferred rather than a rectangular. This is because the total wire length for an 8-bit multiplier is approximately 38% shorter for the triangle compared to the rectangle.

The partial products which are needed in DSP and SP modes are named as important (IMP), which is represented by '>' (Figure 2). The unused IMP partial products are in DSP and SP are termed as unimportant (UIMP), which is represented as 'x'. The reordering of partial products has been performed in three stages and this technique is applied in HPM implementation. In the first stage the two operands of the multiplier are multiplied and partial products are formed as parallelogram structure. (Fig 2(a)) In the second stage the parallelogram structure of partial products is rearranged into triangular by moving the higher height partial products to the lower height. (Fig 2(b)). This helps to reduce the total wire length in the cell placement compare to parallelogram structure. Finally, the reordering of partial products is done by moving all the IMP partial products to the higher height the IMP partial products to the higher height of the partial product tree.(Fig2(c))

The partial products are formed by using two input AND gates for the IMP partial products. An extra control signal is used to control the UIMP partial products in twin precision multiplier, so 3-input AND gate is used in generating the UIMP partial products. Then the generated partial products are reordered. This reordered partial products causes to switch less number of half adder and full adders. In the proposed FIR architecture the multiplier is turned off by converting the 3 input AND gate into a 4 input AND gate where the 4<sup>th</sup> input signal is used to turn of the multiplier by setting it as zero when the input coefficients are less than the threshold.

The column compression is done using HPM. In the HPM algorithm, the height of the tree is reduced by one for each row. For example rows 8, 7, 6, 5, 4, 3, 2 for an 8-bit multiplier. By using this column compression technique the height of the tree is reduced to two. The Fig.3 shows the block diagram for unsigned 8-bit twin precision multiplier by using reordering of partial products and HPM reduction tree. The architecture shows that the transitions that are taking place in DSP and SP mode is reduced compared to basic HPM which leads to the reduction of switching power. In Fig 3, a 4-bit multiplication computed by most significant bits are represented using the full adders are shown in black. Another 4-bit multiplication which is computed by the least significant bits are shown in white. The adder blocks given in grey remains idle in the DSP mode. The white blocks are enabled only in SP mode.

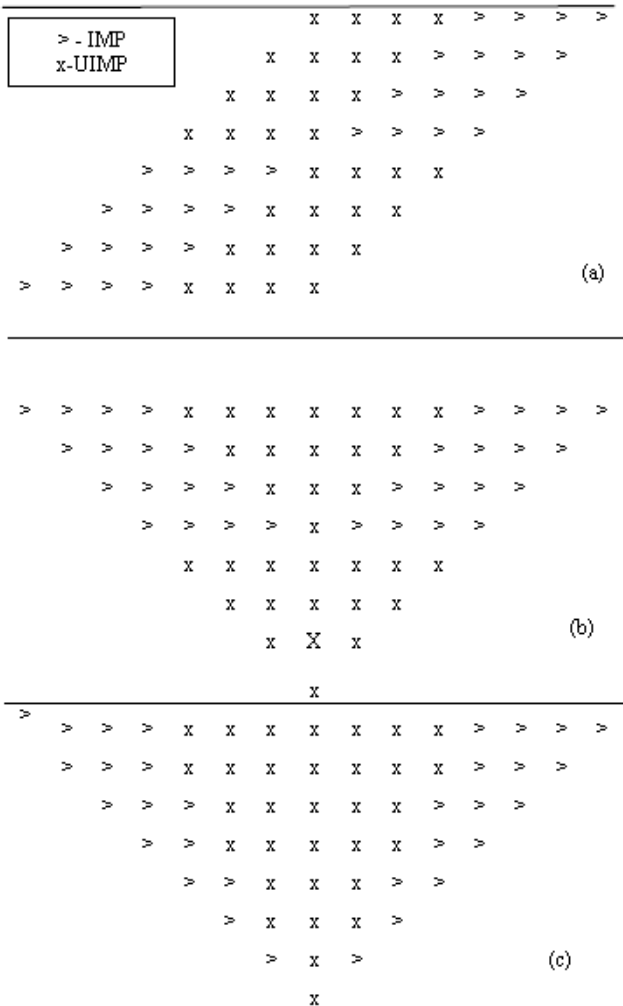


Figure 2. Reordering of partial products for lower switching activity

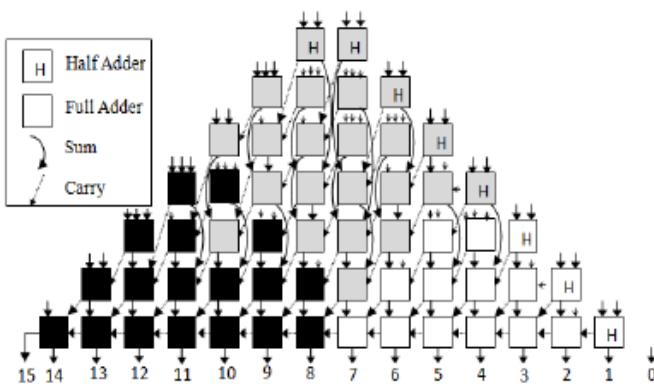


Figure 3. Architecture of an unsigned 8-bit twin precision multiplier by using reordering of partial products and HPM reduction tree.

**LOW POWER CARRY SELECT ADDER USED IN THE FIR ARCHITECTURE**

Addition operation has been performed in the proposed architecture by the area and power efficient low power carry select adder(CSLA) in place of the normal adder. In the conventional digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. But in CSLA adder the problem of carry propagation delay is done by by independently generating multiple carries and then select a carry to generate the sum .It uses a Binary to Excess-1 Converter (BEC) instead of Ripple Carry Adder with  $C_{in} = 1$  in the regular CSLA to achieve lower area and power consumption [2]-[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the  $n$  bit Full Adder (FA) structure.

The basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal  $C_{in}$ . The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

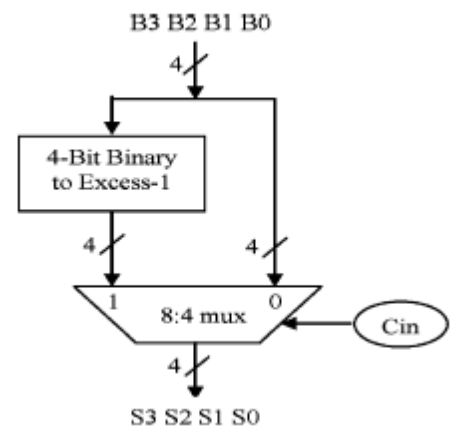


Figure 4. BEC with 8:4 mux used in the adder

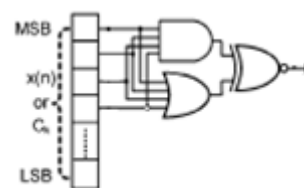
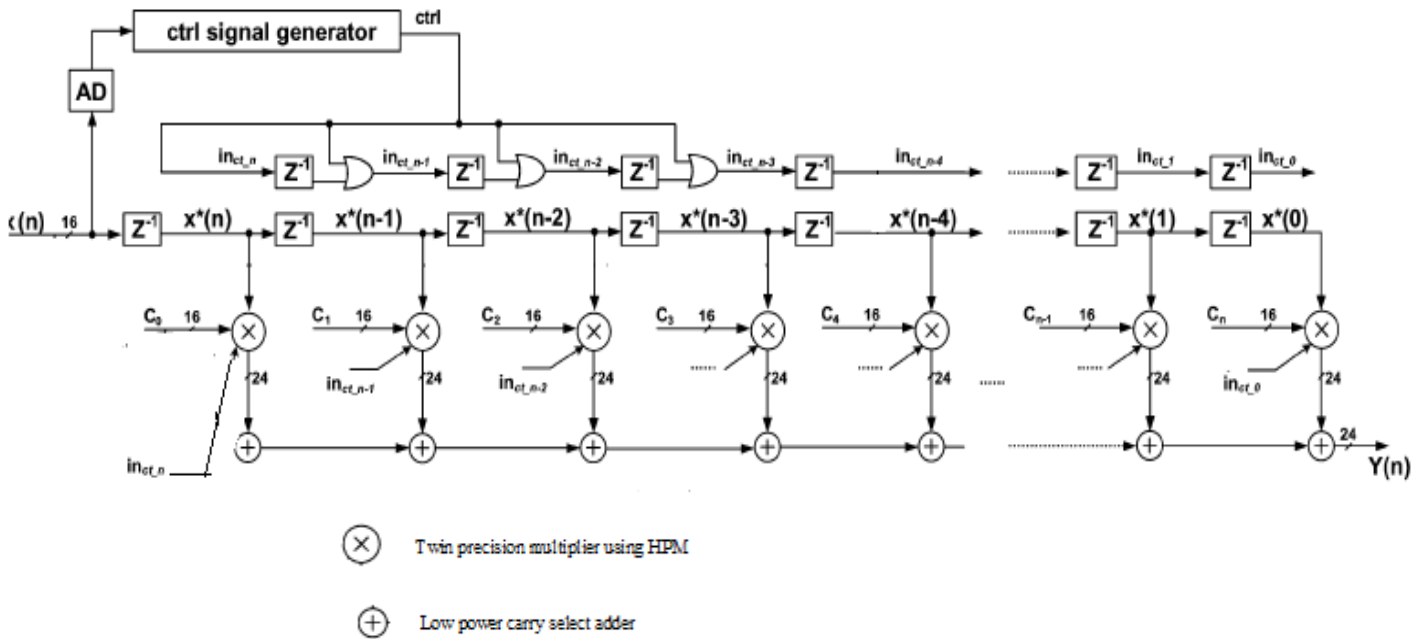


Figure 5. Amplitude detection logic(AD)

**ARCHITECTURE OF PROPOSED MODIFIED FIR FILTER INCORPORATING THE TWIN PRECISION MULTIPLIER AND LOW POWER ADDER**



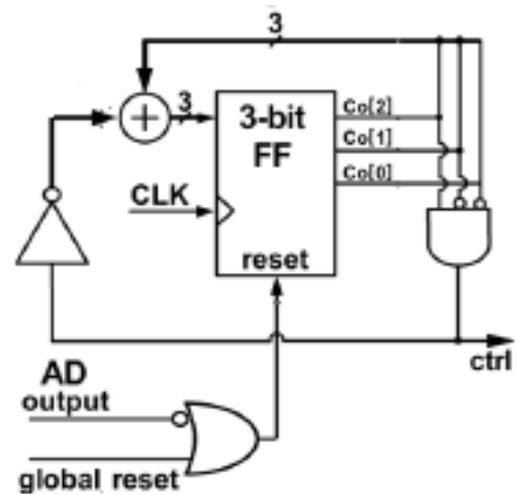
**Figure 6.** Modified FIR filter architecture using Twin precision technique and low power carry select adder

**A. AMPLITUDE DETECTION LOGIC AND CONTROL GENERATOR**

In order to monitor the amplitudes of input samples  $x(n)$  and cancel the right multiplication operations in the fir filter, amplitude detector (AD) in Fig. 5 is used. When the absolute value of input is smaller than the threshold, the output of AD is set to “1”. AD can be implemented using a simple comparator.

Fig. 7. shows the *ctrl* signal generator design. As an input smaller than the threshold comes in and AD output is set to “1”, the counter is counting up. When the counter reaches *m*, the *ctrl* signal in the figure changes to “1”, which indicates that consecutive *m* small inputs are monitored and the multipliers are turned off. In the proposed reconfigurable filter, if we turn off the multiplier by considering each of the input amplitude only, then, if the amplitude of input abruptly changes for every cycle, the multiplier will be turned on and off continuously, which incurs considerable switching activities. . Using *ctrl* signal generator, the number of input samples consecutively smaller than threshold are counted and the multipliers are turned off only when *m* consecutive input samples are smaller than threshold.

**SIMULATION RESULTS**



**Figure7.** Schematic of control signal generator

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device		On-Chip	Power (W)	Used	Available	Utilization (%)			Supply	Summary	Total	Dynamic	Quiescent
Family	Spartan3	Logic	0.000	792	1536	52		Source	Voltage	Current (A)	Current (A)	Current (A)	
Part	xc3s50	Signals	0.001	948	---	---		Vccint	1.200	0.007	0.002	0.006	
Package	pq208	MULTs	0.000	4	4	100		Vccaux	2.500	0.008	0.001	0.007	
Grade	Commercial	IOs	0.040	96	124	77		Vcco25	2.500	0.016	0.015	0.002	
Process	Typical	Leakage	0.028										
Speed Grade	-5	Total	0.069										
Environment		Thermal Properties		Effective TJA	Max Ambient	Junction Temp							
Ambient Temp (C)	30.0			(C/W)	(C)	(C)							
Use custom TJA?	No			37.0	82.4	32.6							
Custom TJA (C/W)	NA												
Airflow (LFM)	0												
Supply Power (W)											Total	Dynamic	Quiescent
											0.069	0.041	0.028

Figure 8. Simulated power analysis

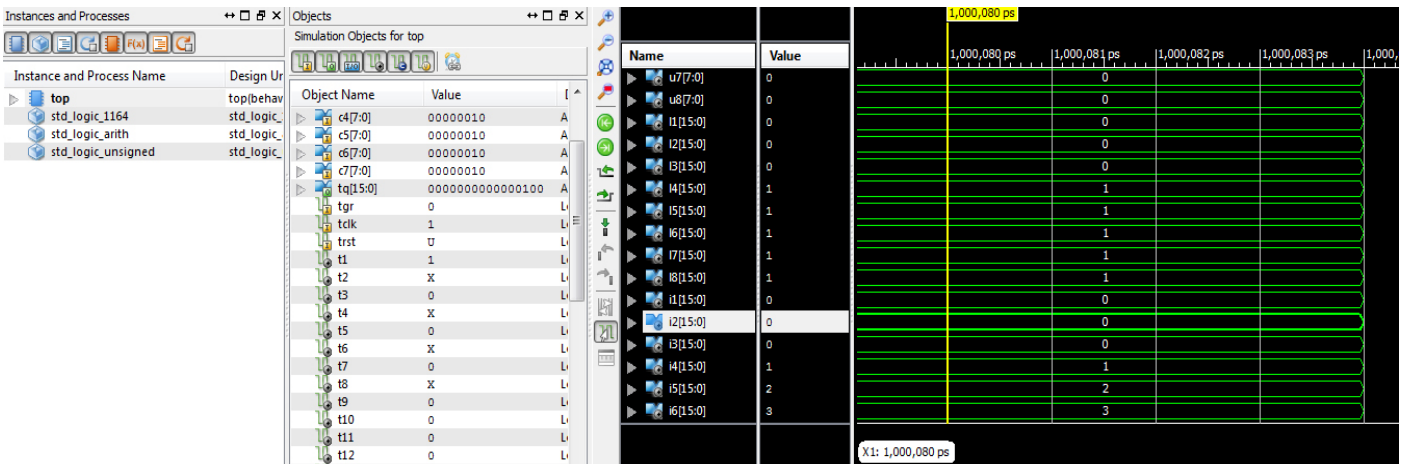


Figure 9. Simulation waveforms

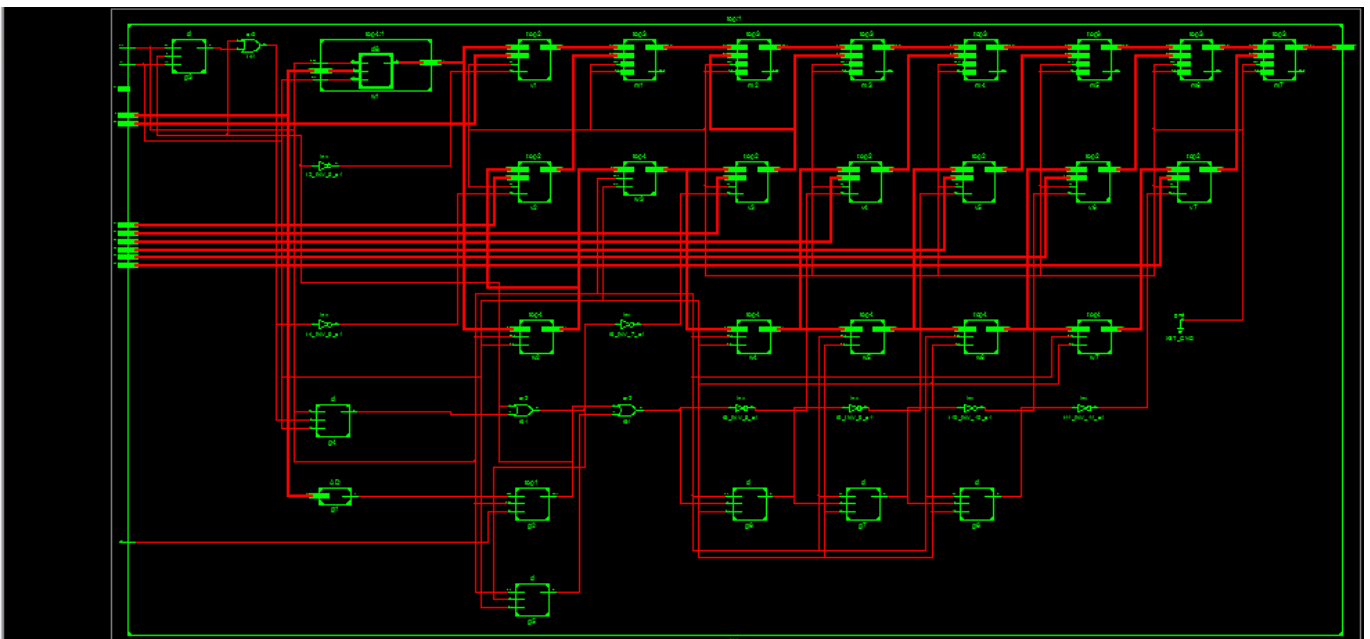


Figure 10. RTL Schematic

## CONCLUSION

In this paper a modified reconfigurable FIR filter is proposed by incorporating the twin precision multiplier and a low power carry select adder. The reordering of partial products technique using HPM implementation has less power consumption compared to the normal conventional multipliers used in the existing FIR filter. Also the power and area savings has been enhanced by replacing the normal adders by low power carry select adder in the proposed modified FIR filter. So the two major operations, multiplication and addition in the FIR filter are done at the cost of low power and area compared to the normal existing FIR architecture. Thus a low power reconfigurable FIR filter architecture for low power application is presented to allow better trade off between the filter performance and computational energy.

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