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Top Gate Planner Carbon Nanotube Field Effect Transistor using Nanohub

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Abstract

A study of I_d versus V_{gs} characteristic of the top gate planner CNTFETs for different diameter and length of carbon nanotube is done and simulation of the same is performed over Nanohub. The characteristic curve is plotted for three cases: (i) (10, 0) CNT with channel length 10nm and gate length 8nm, (ii) (10,0) CNT with channel length 15nm and gate length 12nm and (iii) (13,0) CNT with channel length 10nm and gate length 8nm. It is found that CNTFET is capable of delivering three to four times higher drive currents than the Si MOSFETs at an overdrive of 1 V, and has about four times higher transconductance. Thus, for future applications and performance point of view, CNTFETs can be a better choice than a conventional MOSFET.

Keyword: Carbon Nanotube, FET, CMOS, Dielectric Constant, Nanoelectronics

INTRODUCTION

In the Carbon nanotube Field Effect Transistor (CNTFET) technology the single wall carbon nanotube (SWCNT) is generally used as a channel between source and drain in CNTFET. Both p-channel and n-channel devices can be made from nanotubes. The physical structure of CNTFETs is very similar to that of MOSFETs and their I-V characteristics and transfer characteristics are also very promising and they suggest that CNTFETs have the potential to be a successful replacement of MOSFETs in nanoelectronics [1].

The first carbon nanotube field-effect transistors were reported in 1998. These were simple devices fabricated by depositing single-wall CNTs (which is synthesized by laser ablation) form solution onto oxidized Si wafers which had been pre-patterned with gold or platinum electrodes [2]. The electrodes served as source and drain, connected via the nanotube channel, and the doped Si substrate served as the gate. All early CNTFET were p-type, i.e., hole conductors. Whether this was due to contact doping or doping by the adsorption of oxygen from the atmosphere was initially unclear. N-type conduction was achieved by doping from an alkali (electron donor) gas and by thermal annealing in vacuum [3]. Doping by exposure to an alkali gas involves charge transfer within the bulk of the nanotube, analogous to doping in conventional semiconductor materials. The ability to make both p-type and n-type CNTFETs enabled the first carbon nanotube CMOS circuits. These were demonstrated by Derycke et al., who built simple CMOS logic gates, including an inverter in which the two CNTFETs were fabricated using a single carbon nanotube. Subsequently, more complex carbon nanotube based circuits have been built [4,5,6,7,8].

TOP GATE PLANNER CNTFET

To get better performance Wind et al. proposed the first top gate CNTFET in 2003[9]. The carbon nanotube is completely embedded within the gate insulator, offering the full advantage of the gate dielectric. This top gate structure allows the fabrication of both n-type as well as p-type devices. It contains an additional advantage that with only slight modification, it can be made suitable for high-frequency operation, which is not possible with back-gated devices due to the large overlap capacitance between the gate, source, and drain. These features make the top gate devices the most technologically relevant CNT transistors fabricated so far, and they allow for a more direct comparison with mainstream silicon-based MOSFETs [9]. Figure-1 shows the schematic diagram of a top-gate CNTFET with Ti source, drain, and gate electrodes. A 15-nm SiO2 film was used as the gate oxide. Here gate is placed over the CNT.

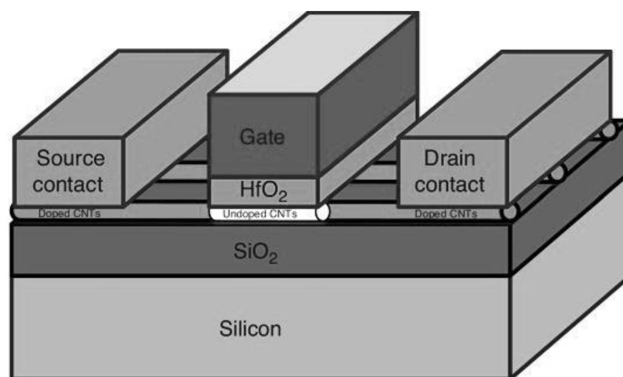

Figure 1: Top Gate CNTFET

Modeling Top Gate CNTFET

A Top Gate CNTFET model is given by Yao Xu and Ashok Srivastava. They suggested static and dynamic model of Top Gate CNTFETs. On the basis of current transport mechanism in carbon nanotube, the static and dynamic model of Top Gate CNTFETs is developed. The Static model of CNT-FET is shown in Figure 2, which is similar to the structure of a typical MOSFET, where a SWCNT forms the channel between two electrodes, which work as the source and drain of the transistor. The structure is built on top of an insulating layer and a substrate which works as the back gate. The top gate is metal over the thin gate oxide [10]. Current transport

equations in a CNT-FET are developed in which both drift current and diffusion currents mechanisms are included.

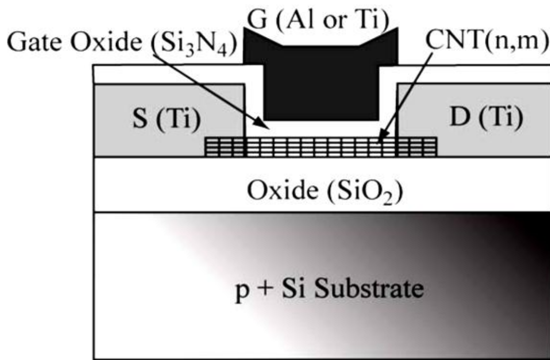

Figure 2: Cross sectional view of top gate CNTFET model

$$I_{ds} = I_{drift} + I_{diff}$$
$$= \beta\left[f_{drift}\{\Psi_{cnt,s}(L), V_{gs}\} - f_{drift}\{\Psi_{cnt,s}(O), V_{gs}\}\right] + \beta\left[f_{diff}\{\Psi_{cnt,s}(L), V_{gs}\} - f_{diff}\{\Psi_{cnt,s}(O), V_{gs}\}\right] \quad (1)$$

Where,

$$f_{drift}(\psi_{cnt,s}(x), V_{gs}) = (V_{gs} + V_{sb} - V_{fb})\psi_{cnt,s}(x) - \frac{1}{2}\psi^2_{cnt,s}(x)$$

$f_{diff}(\psi_{cnt,s}(x), V_{gs}) = \frac{kT}{q}\psi_{cnt,s}(x)$, and $\beta = \gamma\frac{\mu C_{ox1}}{L^2}$

In equation (1) L is gate length, μ is carrier mobility, K is Boltzmann constant, T is temperature in Kelvin (°K), V_{fb} is flat-band voltage, V_{sb} is source-substrate voltage, $\psi_{cnt,s}$ is surface potential of CNT and C_{ox1} is gate-oxide capacitance per unit area. Thus, for a carbon nanotube of length *L* and radius r in a CNT-FET, the oxide capacitance is given by:

$$C_{ox1} = \frac{2\pi\varepsilon_{ox1}L}{\ln\left(\frac{T_{ox1} + r + \sqrt{T^2_{ox1} + 2T_{ox1}r}}{r}\right)} \quad (2)$$

In equation (2), T_{ox1} is the thickness of the gate oxide and *r* is the radius of the CNT. If we include the effect of channel length modulation through the parameter λ as in the case of MOSFET the equation (1) of drain current in saturation region is modified as:

$$I_{ds} = \beta\left[f\{\psi_{cnt,s}(L), V_{gs}\} - f\{\psi_{cnt,s}(O), V_{gs}\}\right](1 + \lambda V_{ds})$$

The dynamic response of a CNT-FET can be modeled using Meyer capacitance model as shown in figure 3. The value of capacitances, C_{gs}, C_{gd} and C_{gb} based on current transport modeling of CNT-FETs are as follows:

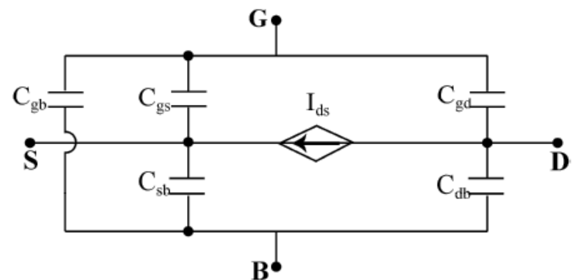

Figure 3: Meyer capacitance model for CNT-FETs.

In linear region,

$$C_{gb} = 0$$

$$C_{gs} = -\frac{\gamma\mu W|C_h|C'^2_{ox1}}{2\beta}.$$
$$\frac{\left[\delta Ie^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} + \frac{kT}{q} + V_{fb} - V_{gs})\right]\left[\delta Ie^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_C}{q} + \frac{kT}{q} + V_{fb} - \frac{2}{3}V_{gd} - \frac{1}{3}V_{gs})\right]}{\left[\delta Ie^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_C}{q} + \frac{kT}{q} + V_{fb} - \frac{1}{2}V_{gd} - \frac{1}{2}V_{gs})\right]^2}$$

$$C_{gd} = -\frac{\gamma\mu W|C_h|C'^2_{ox1}}{2\beta}.$$
$$\frac{\left[\delta Ie^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_c}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - V_{gs})\right]\left[\delta Ie^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_c}{q} + \frac{E_c}{q} + \frac{kT}{q} + V_{fb} - \frac{1}{3}V_{gd} - \frac{2}{3}V_{gs})\right]}{\left[\delta Ie^{-1} - \delta\Delta(\phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} + V_{fb} - \frac{1}{2}V_{gd} - \frac{1}{2}V_{gs})\right]^2}$$

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In saturation region,

$$C_{gb} = 0$$

$$C_{gs} = \frac{1}{3}\frac{\gamma\mu W|C_h|C_{ox1}'^2}{\beta}$$

$$C_{gd} = 0$$

Assuming C_{sb} and C_{db} to be equal to one half of the series combination of insulator capacitance, $C_{ox2}/2$ and depletion-layer capacitance, $C_{subs}/2$, the expression for C_{ox2} and C_{subs} is obtained as:

$$C_{ox2} = \left. 2\pi\varepsilon_{ox2}L \middle/ ln\left(\frac{T_{ox1} + r + \sqrt{T_{ox2}^2 + 2T_{ox2}r}}{r}\right)\right.$$

$$C_{subs} = \frac{N_A q\varepsilon_s + \sqrt{N_A q\varepsilon_s}\sqrt{8C_{ox2}^2 V_{gb} + N_A q\varepsilon_s - 8C_{ox2}^2\phi_{ms} - 8C_{ox2}^2\psi_{cnt}}}{4C_{ox2}(V_{gb} - \phi_{ms} - \psi_{cnt})}$$

Where, ε_s is the permittivity of semiconductor, W_s is the depletion region width and N_A is the doping concentration. The threshold voltage of CNTFETs is proportional to the inverse of the diameter of nanotubes as:

$$V_{th} = \frac{0.42}{d(nm)}\ eV$$

Where, d is the diameter and V_{th} is the threshold voltage. A simulation compatible model is shown in Figure 4. In figure V_{FB} is the flat band voltage, which is a voltage at which there is no electrical charge in the semiconductor and therefore no voltage drop across it, in band diagram the energy bands of the semiconductor are horizontal (flat).

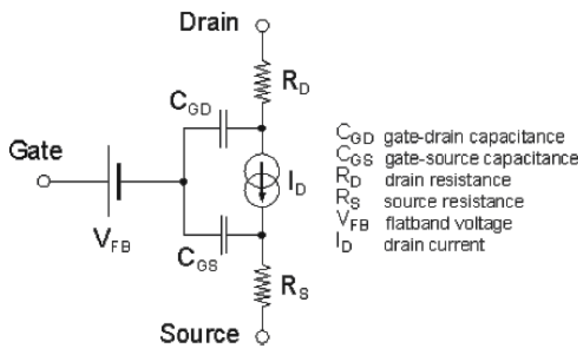

Figure 4: Electrical simulation compatible model for CNTFET.

SIMULATION OF TOP GATE PLANNER CNTFET

In this section the simulation of planner CNTFETs have been done and an attempt is made to show that the CNTFETs are better in performance than the conventional Field Effect Transistors. The simulation of planner type CNTFETs is done with the help of http//:www.nanohub.org, which provides very good on line simulation tools for the simulation of nano devices such as CNTFETs, Si-Nanowire FETs and many types of conventional Field Effect Transistors like p-n junction, Si-MOSFET, DG-MOSFET etc. The Nanohub was created by the NSF-funded Network for Computational Nanotechnology and provides very good resource for nanoscience and technology.

To simulate Top gate Planner CNTFET a Carbon Nanotube of Chiral Vector (13,0) with diameter of about 1nm is taken. Following parameters are submitted in CNTFET tool to simulate the Top gate Planner CNTFET.

Parameter	Value
Bond length of carbon (c-c)	= 0.144 nm
Nanotube length (l)	= 80 nm
Top gate length	= 84 nm
Top gate thickness	= 5nm
Top gate width	=20nm
Gate insulator thickness/height	= 1.0nm
External Source- Drain contact length	= 0nm
Source –drain thickness height	= 7nm
Source drain width	= 15nm
Substrate to nanotube gap/distance	= 0.144nm
Substrate thickness/height	= 9nm
Device width	= 20nm
Dielectric constant of nanotube interior	= 1.0
Dielectric constant of gate insulator	=20 (high –k dielectric ZrO_2)
Dielectric constant of substrate	= 3.9 (for silicon oxide SiO_2)

To reduce the leakage current and to minimize the other type of losses, the materials having high dielectric constant is preferred in advance node technology like 45-nm, 32-nm and 22-nm. Some materials possessing high K are: Hafnium Oxide HfO_2 ($\mathcal{E}_r$=12), Zyrconium Oxide ZrO_2 ($\mathcal{E}_r$=20), Tantalum Oxide Ta_2O_5 ($\mathcal{E}_r$ =25) and Titanium Oxide TiO_2 ($\mathcal{E}_r$ =40). In the simulation of planner CNTFET ZrO_2 is used as dielectric material.

The length of carbon nanotube is taken as 80nm so that it can be compared in terms of I_{on}/I_{off} with respect to 90nm technology node parameters. Since the CNTFETs are fabricated on Silicon Dioxide (SiO_2) substrate, hence the value of substrate dielectric is taken as 3.2.The c-c bond coupling energy is taken as 3eV. The simulation operating temperature of the top gate planner CNTFET is set at 300°K.

The simulation is done to obtain the output characteristic (I_d-V_d) at different gate voltage (V_g). The range of drain voltage is 0V to 0.4V and the plots are obtained for gate voltages 0.2V, 0.3V, 0.4V and 0.6V.

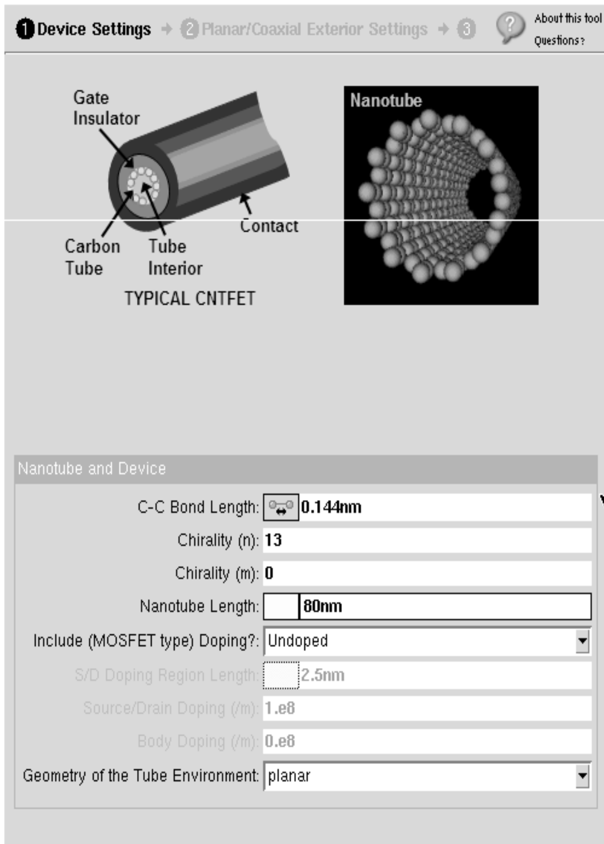

Figure 5(a)

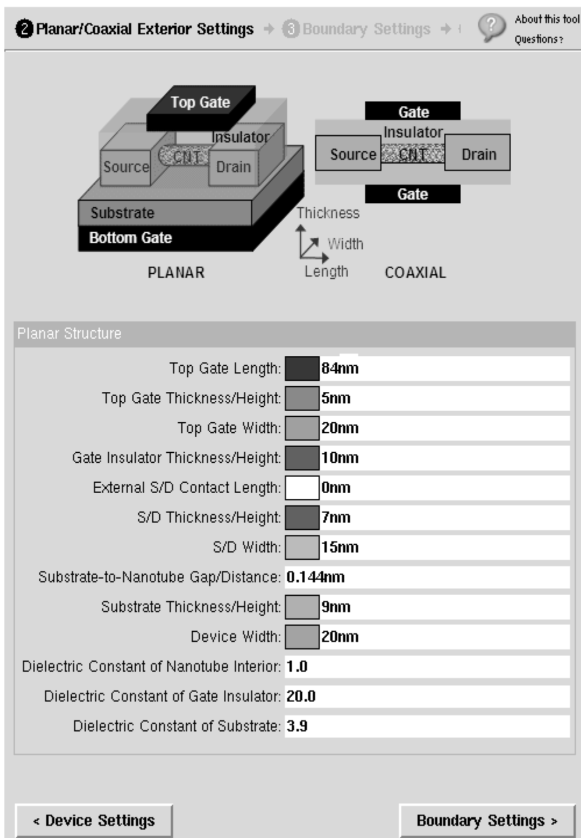

Figure 5(b)

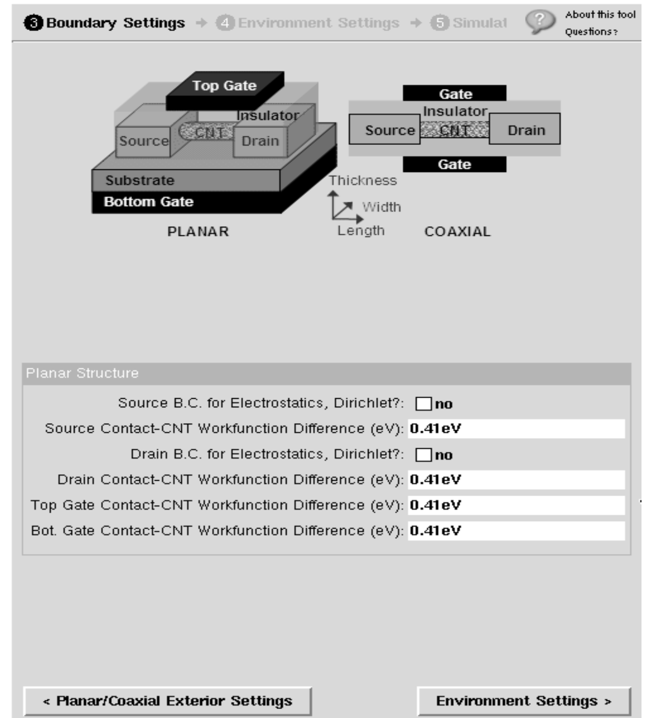

Figure 5(c)

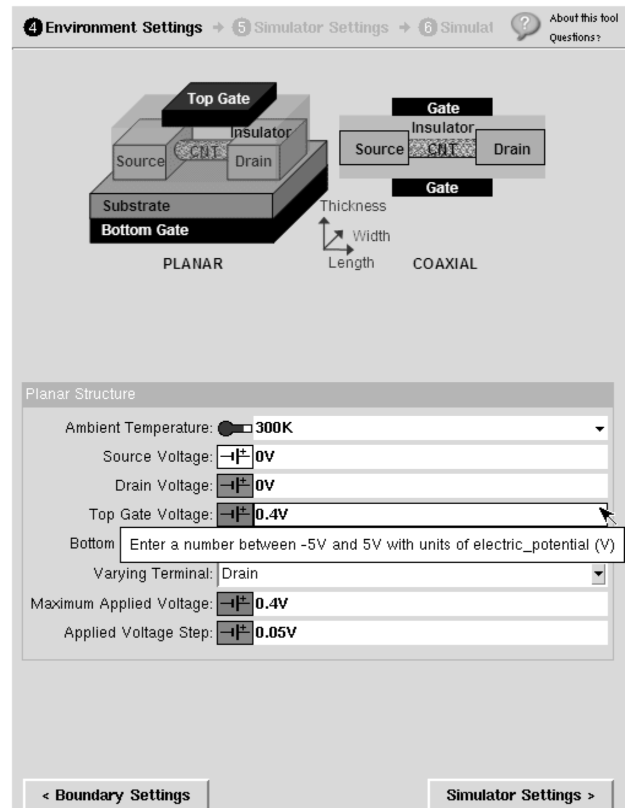

Figure 5(d)

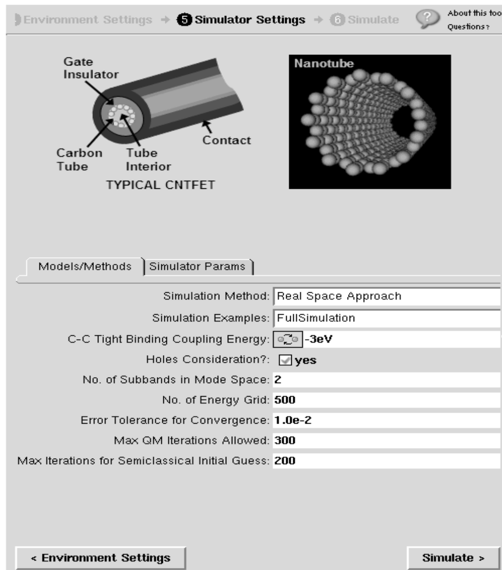

Figure 5(e)

Figure 5(a),(b),(c),(d),(e): Description of top gate planner CNTFET on Nanohub.

SIMULATION RESULT

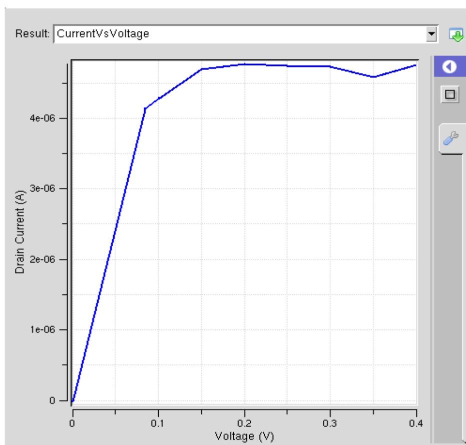

Figure 6(a): (I_d ~ V_d at V_g = 0.6 volts)

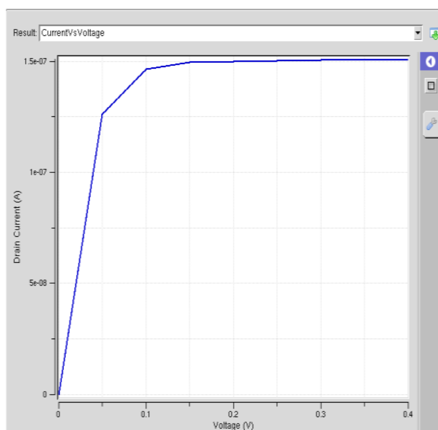

Figure 6(b): (I_d ~ V_d at V_g = 0.4 volts)

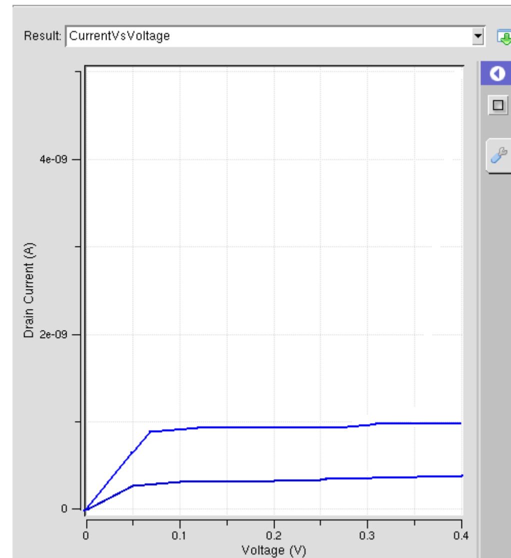

Figure 6(c): (I_d ~ V_d at V_g = 0.2 volts)

CONCLUSION

Figures 6(a) to 6(c) shows the I_d ~ V_d characteristics of top gate planner CNTFET, from these curves it is apparent that CNTFET produces a good replacement of Field Effect Transistor. One can simulate the CNTFET for different diameter and observe the effect on output characteristic. The I_d ~ V_g characteristic for the top gate planner CNTFETs for the different diameter and length of carbon nanotube is shown in the figure 7. These are plotted for three cases: (i) (10, 0) CNT with channel length 10nm and gate length 8nm, (ii) (10,0) CNT with channel length 15nm and gate length 12nm and (iii) (13,0) CNT with channel length 10nm and gate length 8nm. Comparing the first two it is observed that keeping the diameter of CNT fixed, if the length of CNT is varied, this results in higher saturation current for smaller channel length. Again comparing the curves for first and third set which are drawn for different chirality, the saturation drain current is higher for a CNTFET consisting of smaller diameter keeping the length constant.

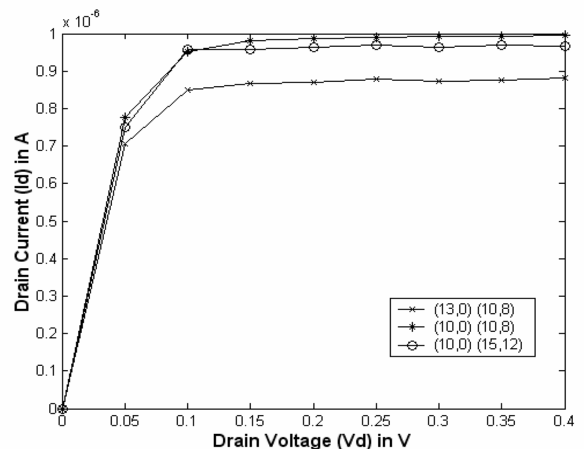

Figure 7: I_d ~ V_g characteristics for different diameter and length of carbon nanotubes

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