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Design of an Optimized FBMC Transmitter by using Clock Gating Technique based QAM for Low Area, Power and High Speed Applications

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Abstract
The filter bank multicarrier modulation (FBMC) technique is one of multicarrier modulation technique (MCM), which is mainly used to improve channel capacity of cognitive radio (CR) network and frequency spectrum access technique. The existing FBMC contains serial to parallel converter, normal QAM modulation, Radix2 inverse FFT, parallel to serial converter and poly phase filter. It needs high area, delay and power consumption. To further reduce the area, delay and power of FBMC structure, a new clock gating technique is applied in the QAM modulation, radix2 multipath delay commutator (R2MDC) based inverse FFT. The clock gating technique is mainly used to reduce the unwanted clock switching activity. The clock gating is nothing but clock signal of flip-flops is controlled by gate (i.e) AND gate. Hence speed is high and power consumption is low. The comparison between existing QAM and proposed QAM with clock gating technique is carried out to analyze the results. Conversely, the proposed inverse R2MDC FFT with clock gating technique is compared with the existing radix2 inverse FFT. The proposed FBMC with clock gating technique offers low area, power and high speed than the existing FBMC structures.

Keywords: OFDM, FBMC, clock gating technique, R2MDC based inverse FFT; FIR filter and PASTA adder.

INTRODUCTION

The Filter bank multicarrier modulation (FBMC) is mainly used in optical communication, wireless communication, Cognitive Radio (CR) network and multiple access networks. The FBMC is mainly used to transmit a multiple data at a time with multiple carrier frequency. The huge data is transmitted at a time by using either OFDM or FBMC. The large data are divided into multiple subcarriers OFDM. Hence signaling overhead is high and spectral efficiency is low in OFDM. To avoid this kind of issue, non-orthogonal filter bank technique is used in FBMC in order to achieve high spectral efficiency and low signal overhead.

LITERATURE SURVEY

Recently, filter bank multi carrier modulation technique is significant in 4G and 5G wireless communications. In 5G air interface, Filter bank multicarrier with offset quadrature amplitude modulation (FBMC-OQAM) scheme is mainly used to improve the spectral efficiency. It gives the best spectrum shape when compared to existing OFDM modulation scheme. Furthermore it enables superior mobility support [1]. However the complexity of this modulation scheme is very high. These days, digital modulation methods are used to transfer digital to analog signals. Modulation is nothing but varying the frequency or phase or amplitude of carrier signal with respect to amplitude or phase or frequency of message signal [3]. Modulation technique is mainly used for high distance data transmission purpose by boosting the carrier signal. Lot of digital modulation technique are available such as continues phase modulation (CPM), Quadrature amplitude modulation (QAM), frequency shift keying (FSK), phase shift keying (PSK) and amplitude shift keying (ASK) [4]. From these modulations, the QAM is one of the finest digital modulation methods. The mixture of ASK and PSK modulation is also called as QAM modulation. In-phase signal (I) and quadrature phase signal (Q) are used in QAM. From these two phase signal, one phase signal is used as cosine waveform and an additional phase signal is used as sine waveform. Amplitude modulation (AM) is carried out for these two phase signal along with a finite number of amplitudes. All these signals are added at final stage. It looks like two channel system, which is working based on ASK modulations. These results are equivalent to mixing of ASK and PSK. The most important benefit of QAM modulation is able to transmit several bit of information per symbol. It gives high speed when compared to all other modulation technique such as QPSK and BPSK modulations [2].

Time or space domain to frequency domain conversion is carried out by using Fast Fourier Transform (FFT). Conversely, the frequency domain to time domain conversion is performed by using the inverse FFT (IFFT) operation [5]. FFT is useful for demodulation function. Similarly, the IFFT is useful for modulation function. Furthermore IFFT is incorporated in the transmitter side as well as FFT is applied in the receiver side. Several types of FFT techniques are presented such as mixed radix, radix2, radix4 and radix8 [6]. The recital of radix4 is high when compared to the radix2. However the difficulty of radix2 is low when compared to the radix4 operation. Also the radix2 FFT offers low area and power than the radix8 and radix4 operation. Presently, pipelined feedback and feed forward FFT are introduced for parallel operation. Single path delay feedback (SDF) and multi-path delay feedback (MDF) are pipelined feedback FFT/IFFT structures. Single-path delay commutator (SDC) and multi-path delay commutator (MDC) are used as pipelined feed forward FFT/IFFT [7]. Consequently the speed is very high in MDF and MDC based FFT/IFFT due to adding more delay element than the radix2, radix4, radix8 and mixed radix. Other than the power and area is high [9]. On the other hand, the area and power is very low in SDF and SDC based FFT/IFFT. However the performance is lower than the MDF and MDC based FFT/IFFT [8]. To keep away from this kind of issue, we are going to use radix2 based MDC structure with clock gating technique to achieve low area, delay and power

with less complexity at a time. The clock gating technique is nothing but system clock and enable signal are given to AND gate. The AND gate is on when both signal are high. Hence the clock signal is generated when both enable and system clock are high. This is called as clock gating technique. Also the final clock generation output is called as gated clock [16] and [17]. In this paper, the clock gating technique is applied in QAM, R2MDC based inverse FFT. The clock gating technique is one of the power optimization techniques in VLSI. The clock gating technique is mainly used to reduce power dissipation due to high frequency and high load of clock signal.

EXISTING FBMC TECHNIQUE

The existing FBMC consists of QAM modulation, Radix2 inverse FFT, parallel to serial converter and poly phase filter as shown in fig.1. QAM modulation is used to boost the carrier signal during the data transmission. The 128 point Radix2 IFFT used to convert frequency to time domain. This 128 bit converted to 8 bit by using parallel to serial converter. Finally, the poly phase filter is used to removes the side lobes of FBMC transmitter. Hence we can get the clear carrier output.

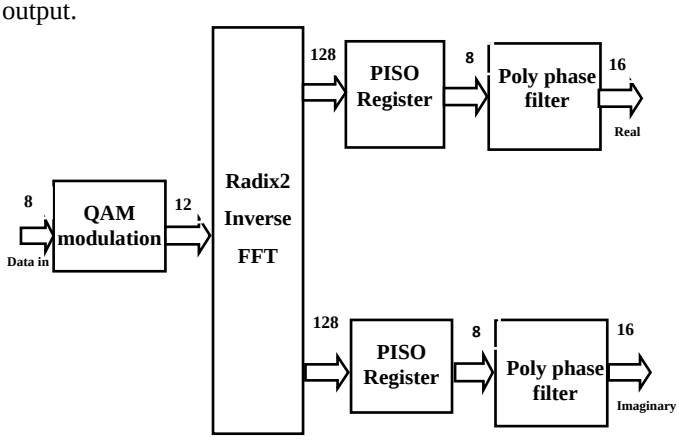

Figure 1. Block diagram of Existing FBMC transmitter

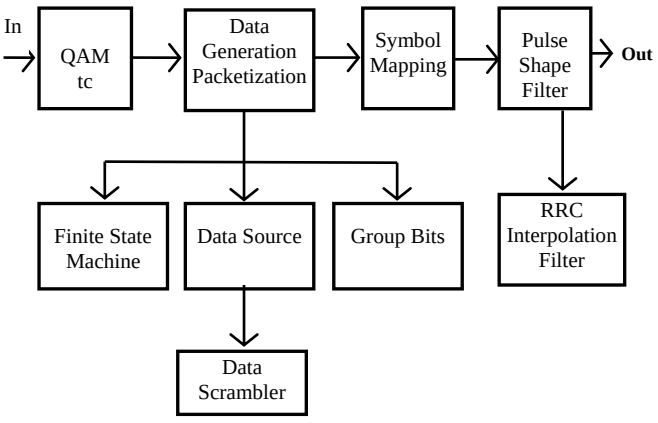

Figure 2. Block diagram of Digital QAM modulation

The digital QAM modulation technique consists of QAM trellis code (QAM-tc), data generation and packetization (DGP), symbol mapping and pulse shaping FIR filter as shown in fig.2. In the DGP, the whole data are divided into n number of packets and grouping the bits for symbol mapping. In DGP, the controller (FSM) and data source are used to make preamble bit and data bit. The packets are constructed by using scrambling operation of data source. The input data bit stream into six bit integer conversion process is carried out by group bits at 1/6 of sampling rate, as needed by the symbol mapper. In symbol mapping, maps the bits output from DGP to QAM symbols. The up sampling and pulse shaping of symbols is performed by using interpolating root raised cosine (RRC) filter for data transmission.

PROPOSED FBMC TECHNIQUE

The proposed FBMC transmitter contains QAM modulation with clock gating, R2MDC based IFFT with clock gating, parallel to serial converter (PISO). The 64 QAM modulations are performed by combing amplitude modulation and phase shift keying. In digital QAM, the amplitude shift keying is used to convert two digital bit streams. This QAM modulation achieves high data rates by using efficient constellation diagram and linearity of communication channel. The constellation diagram is a representation of signal modulated by a digital modulation scheme. It is used to display the signals as two dimensional XY plane scatter diagram. Type of interference and distortion in a signal is recognized by using constellation diagram measurement. QAM is a higher order of modulation. So it able to carry more bits of data per symbol. The data rate of a link can be increased by selecting high order QAM (64QAM) as shown in Fig.3. Also clock gating technique is applied in three places of QAM modulation technique in order to reduce power dissipation and optimize the power consumption than the existing QAM modulation. The circuit diagram of 8point inverse R2MDC FFT with CGT is shown in fig.5. From the figure, it consists of butterfly unit (BF), commutator (C2), delay elements (1, 2, 4, 8 bit size), clock gating technique (CGT), diamond shape indicates trivial rotation (odd s) and circle shape denotes non trivial rotation operation (even s). Instead of pipelined technique, here clock gating technique is applied in the R2MDC IFFT [8] and [9]. The speed is low in radix2 IFFT.

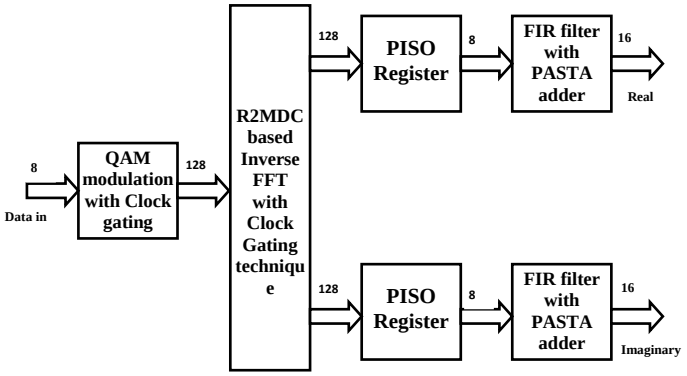

Figure 3. Block diagram of proposed FBMC transmitter

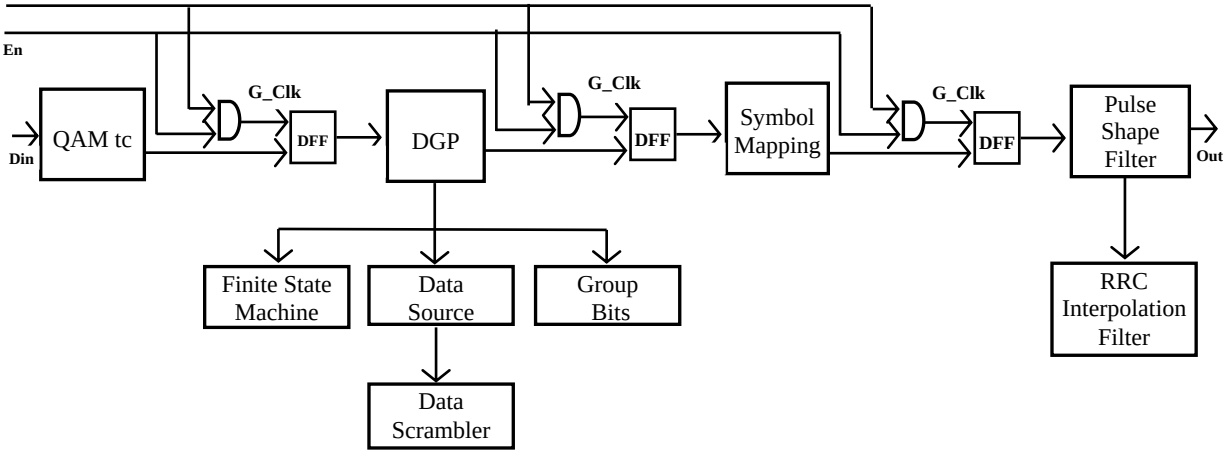

Figure 4. Block diagram of proposed digital QAM modulation with clock gating technique

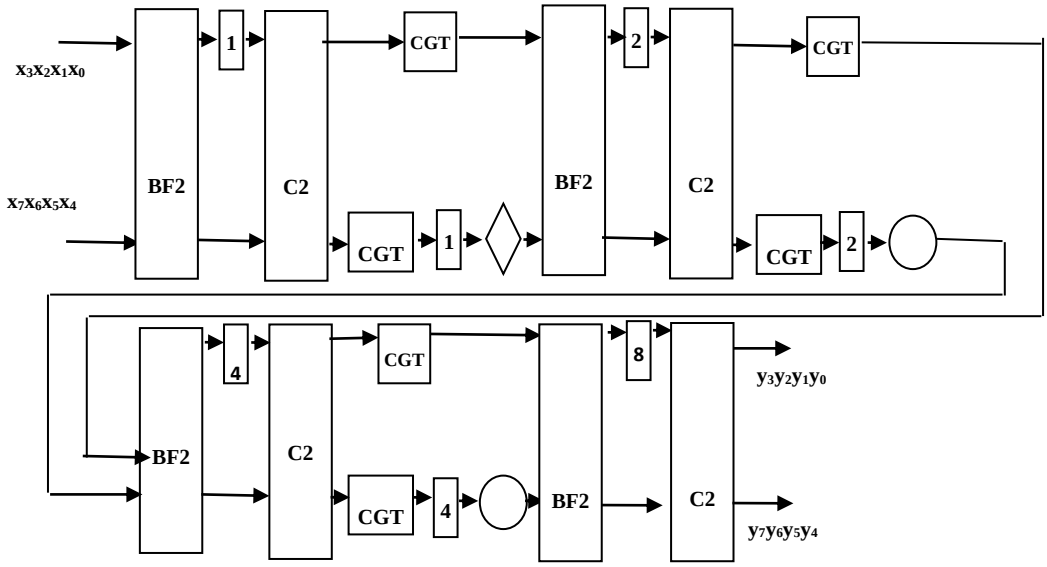

Figure 5. Circuit diagram of 8 point inverse R2MDC FFT with clock gating technique

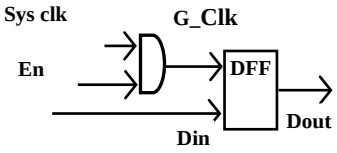

Figure 6. Circuit diagram of clock gating technique (CGT)

To overcome this problem, the multiple delay element with gate control is used to achieve high speed, low area and low power consumption. Addition, subtraction and multiplication operation is performed in butterfly units. Commutator is used to act as switch to transfer data from one stage to another stage. The –j involves real and imaginary swapping and sign conversion. The clock gating structure is shown in fig.6. The system clock and en signal are given to AND gate to produce the gated clock, which is given as clock input of D flip-flops. Hence the clock generation is enabled during active duration. Clock generation is disabled during inactive (hold) condition. Hence it will reduce power dissipation, area and increase the speed of R2MDC FFT.

RESULTS AND DISCUSSION

In this paper, the design of existing and proposed QAM modulation, Existing and proposed IFFT, existing and proposed filter are designed using Verilog HDL language. These three modifications are included in FBMC transmitter structure. Simulation is evaluated by using modelsim6.3g and synthesize process is carried out by Xilinx ISE 13.2, Virtex5, XC5VLX30 and FF324 devices. Initially, the comparison between existing and proposed QAM modulation is performed to analyze area, delay and power as shown in Table.1. From the results, it shows that the proposed QAM modulation with clock gating techniques offers 1% area reduction, 1% power

reduction and 40% delay reduction than the existing QAM modulation.

Type of Transmitter	Slices	LUT	Flip-flops	Power (W)	Delay (ns)
Existing QAM	1055	2244	2466	25.732	6.164
Proposed QAM2 with Clock gating technique	1039	2127	2308	21.726	3.689

Table.1 Comparison between existing and proposed QAM modulation

After that second comparison is performed for both existing and two proposed IFFT as shown in Table.2. The first the comparison between existing radix2 IFFT and pipelined based R2MDC is carried out. From the obtained results it shows that the pipelined based R2MDC IFFT offers 38.55% area reduction and 1% power reduction than the existing radix2 IFFT. But the delay is increased and speed is decreased. To avoid this problem, the clock gating technique is applied in R2MDC IFFT to achieve low area, delay and power than existing radix2 IFFT. The proposed R2MDC with clock gating technique (CGT) offers 36.64% area reduction 21.13% power reduction and 10.74% delay reduction when compared to existing radix2 IFFT.

Type of IFFT	Slices	LUT	Flip-flops	Power (W)	Delay (ns)	Frequency (MHz)
Existing inverse radix2 FFT	262	695	354	10.425	8.721	114.666
Inverse R2MDC FFT with clock gating	166	444	228	8.222	7.784	128.472

Table.2 Comparison between existing and proposed inverse FFT

Type of Filter	Slices	LUT	Flip-flops	Power (W)	Delay (ns)	Frequency (MHz)
Existing FBMC Using Poly phase filter	217	497	224	17.407	2.458	406.835
Proposed FBMC Using clock gating	45	127	99	10.427	0.978	1022.547

Table.3 Comparison between existing and proposed filter

Type of Transmitter	Slices	LUT	Flip-flops	Power (W)	Delay (ns)	Frequency (MHz)
Existing FBMC	4186	13658	7802	44.760	23.685	89.047
Proposed FBMC with clock gating	4005	12686	7416	29.992	2.835	105.234

Table.4 Comparison between existing and proposed FBMC Transmitter

Finally, these modifications are included in FBMC transmitter structure. Comparison between existing and proposed FBMC is performed and the results are given in Table.4. The proposed FBMC without clock gating technique is compared with the existing FBMC transmitter and results says that the proposed FBMC without clock gating gives 5.75% area reduction, 21.86% power reduction and 72.38% delay reduction than the existing FBMC transmitter. Similarly, the proposed FBMC with clock gating technique offers 4.32% area reduction, 32.97% power reduction and 88.03% delay reduction than the existing FBMC transmitter.

CONCLUSION

In this paper, low area, low power and high speed filter bank multi carrier (FBMC) transmitter with clock gating technique is proposed by using modified R2MDC based IFFT, modified QAM modulation with clock gating technique. Simulation is carried out to check the functionality of FBMC transmitter. Synthesis process is performed to evaluate the area, delay and power. FPGA Virtex5 device is used to get the synthesized results of both existing and proposed FBMC transmitter. The proposed inverse R2MDC FFT with clock gating offers 22.83% average area and delay and power product (ADP) than the existing radix2IFFT. Also the proposed QAM modulation with clock gating offers 14% average area, delay and power product (ADP) product than the existing QAM modulation. Similarly, the proposed FBMC transmitter offers 41.66 average area, delay and power (ADP) product than the existing FBMC transmitter. In future, the MIMO FBMC transmitter/receiver is designed for huge data transmission purpose. Also some advanced filter technology is applied for MIMO FBMC transmitter.

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