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Single Phase Asymmetrical Cascaded MLI with Extreme Output Voltage Levels to Switch Ratio

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Abstract

This paper proposes an asymmetrical cascaded single phase H-bridge inverter. The proposed inverter consists of two modules with unequal and isolated dc sources. Each module is composed of dc source, conventional four switches H-bridge and single bidirectional switch. To increase the output voltage levels, the tertiary ratio, 1:3, between its two dc sources is adopted. Both the fundamental frequency and the multicarrier pulse width modulation (PWM) control schemes are employed to generate switches signals. By controlling the inverter modulation index, the proposed inverter can generate an output voltage having up to seventeen levels by using only two modules. The proposed topology has also the feature of modularity which means that it can be extended to any levels by adding new modules. The proposed topology is simulated using an inductive load and some selected simulation results have been provided to validate the proposed inverter.

Keyword: Cascaded Multilevel inverter; symmetrical and asymmetrical configuration; Pulse width modulation; Fundamental frequency control; Selective harmonic elimination (SHE).

INTRODUCTION

Multilevel inverters (MLIs) have gained grate interests in power electronics conversions techniques in the recent years. MLIs are preferred to conventional two level inverters due to (a) they can generate an output voltage which is very close to the sinusoidal waveform and thus they are considered as high power quality systems, (b) they can operate at low switching frequency with high quality output waveforms due to the increased levels and therefore switches stresses and electromagnetic interference can be diminished. The first MLI is the neutral point clamped topology [1]. Generally there are three main MLIs, diode-clamped, flying-capacitor, and cascaded H-bridge (CHB)[2-3] .

Generally the CHB MLI consists of a number of conventional H-bridge inverter modules. Each H-bridge module can generate three levels (0, V_{dc}, $-V_{dc}$). These H-bridge modules are generally connected in series and the final output voltage is synthesized by the combination of theseH-bridge modules. The CHB has the advantage of simple control and structure due to the modular characteristic. Therefore, it is very easy to replace any module if it becomes faulty. Even without discontinuing the load, it is possible to bypass the faulty module by applying an suitable control technique[4 - 6].

The CHB inverter can be divided into two main groups; symmetric and asymmetric or hybrid. The output voltage levels of asymmetric per arm that can be generated are 2n+1where 'n' is the number of H-bridge series connected modules. On the other hand, the most well-known ratios for asymmetric are binary and tertiary, they can generate2(n+1)-1voltage levels per arm. Therefore the asymmetric MLI can reduce the size and cost of the system and improve the reliability due to using fewer semiconductors and capacitors.

A single-phase 7-level PWM inverter is proposed in [7]which synthesizes seven voltage levels per cycle (0, V_{dc}, $2V_{dc}$, $3V_{dc}$, $-V_{dc}$, $-2V_{dc,}$ $3V_{dc}$). This inverter nearly triples the output voltage levels and thus its output voltage harmonic contents are reduced compared to the conventional H-bridge inverter. In [8], authors added a bidirectional switch to the conventional H-bridge single phase inverter. Therefore a five level output voltage waveform. In [9] authors used two series similar modules of the inverter proposed in [8] with equal dc sources. Thus that topology can generate 9 levels (0, V_{dc}, $2V_{dc}$,$3V_{dc}$, $4V_{dc}$, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$) and it is considered as a symmetric MLI. In this proposed topology an asymmetrical CHB inverter based on [8] and [9]is presented. Instead of using equal dc sources, the tertiary ratio is employed to increase the voltage levels with the same number of switches. The number of output voltage levels is increased to 17. The presented MLI in this paper is a modular in addition to both fundamental frequency and PWM control schemes can be employed. Simulation results are provided to verify the validity of the proposed system

The paper is organized as follows: section 2 gives the operational principles of the proposed MLI topology. The Modulation Techniques for the proposed MLI is presented in section 3. Subsequently simulation results are provided in section 4. Modularity of the proposed topology has been studied in section 5. Section 6 presents a comparison between the proposed topology and existing counterparts MLI topologies. Finally conclusion is presented in section 7.

OPERATIONAL PRINCIPLES OF ASYMMETRICAL CASCADED MLI TOPOLOGY

Figure 1(a), (b) and (c) shows the proposed 17 levels single phase asymmetrical cascaded inverter topology and its generated output voltage waveforms for low and medium modulation index (mi). The proposed inverter consists of two series connected modules based on [9]. Each module consists of five IGBT switches as well as four main diodes. Each module requires two equal and non-isolated dc sources. To increase the levels of output voltage, a tertiary ratio 1:3 between the upper module dc source ($2\,V_{dc}$) and the lower module dc source ($6\,V_{dc}$) is adopted. It can be noted that, the input voltage for each module is divided into two equal voltages as shown in figure 1. To obtain this number of levels from the conventional topologies like cascaded H-bridge (CHB) [10], neutral point clamped (NPC) [11], or flying capacitor (FC) inverters [12], a large number of switches and diodes have to be used. The main advantages of the proposed topology are; (1) high level switch ratio (LSR) [13] because of using unequal DC voltage values (1:3 dc source ratio) resulting in reducing the number of components used; (2) the switches utilized in upper module with lower dc source value operate at switching frequency, while the switches utilized in lower module with higher dc source value operate at low frequency. Consequently the switches losses will be reduced.

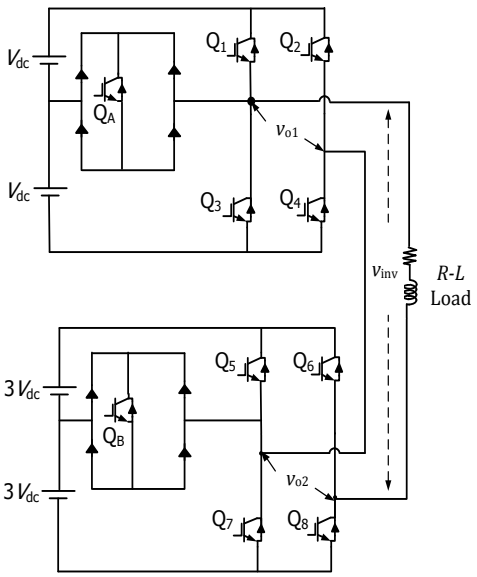
The generated output voltage levels of the proposed MLI are shown in Table 1 where two modules are considered with 10 switches and 4 diodes that are able to generate 17 output voltage levels. The lower module dc voltage source is three times the upper module dc voltage source. From Table 1, to achieve any level, four switches have to be turned on. As an example, for the first level Q_4, Q_a, Q_7, and Q_8should be turned on to get V_{dc} in the output. In this case, inverter voltage v_{inv} = V_{dc}=$v_{o,1}$. It could be noticed from figure 1 (b) and (c) that as the modulation index increases, more levels are generated.

MODULATION TECHNIQUES FOR THE PROPOSED MLI

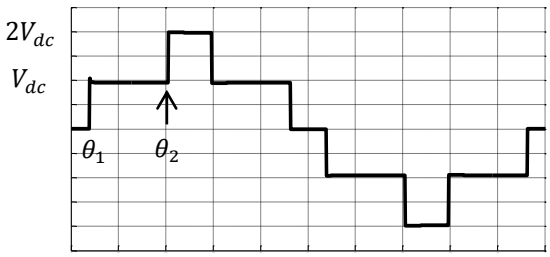
Modulation techniques for MLI can be divided into two well-known categories depending on the switching frequency used to drive the inverter switches: (a) fundamental frequency modulation technique, (b) Sinusoidal Pulse-width modulation (SPWM) technique. Fortunately the proposed topology can be controlled and implemented using both control schemes as explained in details in the following paper section.

(A) FUNDAMENTAL FREQUENCY CONTROL SCHEME

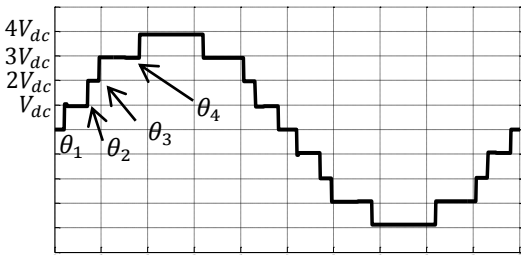
The fundamental frequency control technique is very efficient for MLI because of its superior performance in reducing switching losses and stresses especially in case of using many switches like this proposed MLI. In this case either selective harmonic elimination (SHE) or harmonic minimization technique can be used to determine the switching angles of different switches. Eq. (1) defines the modulation index, it is defined as the output ac fundamental frequency voltage divided by the total dc voltage. For very low mi, a three levels output voltage waveforms (0, V_{dc}, -V_{dc}) is constructedsimilar to the conventional H-bridge inverter. As the miincreases, the inverter generated levels increases. Eqs. (2) and (3) give the fundamental voltage of both cases of mi in figure 1(b) and (c). Eqs. (4) and (5) give the harmonic voltage of the same two cases. It could be noticed that for high mi, an eight switching angles will be emerged and need to be solved. Also as the modulation index increases the switching angles ($\theta_1, \theta_2, \ldots$) increase. The general equation of the harmonic components for the eight switching angles is given in Eq. 6.



(a) Inverter topology.



(b) Generated output voltage for low modulation index.



(c) Generated output voltage for medium modulation index.

Figure 1. Proposed 17 levels single phase asymmetrical cascaded inverter.

Table 1: Output voltages of two modules

Ratios: upper module $2V_{dc}$ divided V_{dc}&V_{dc} Lower module 6 V_{dc} divided 3 V_{dc}& 3 V_{dc}	States No.	Upper module voltage $[v_{o1}]$	Lower module voltage $[v_{o2}]$	Output voltage $[v_{inv}]$	Q1	Q2	Q3	Q4	QA	Q5	Q6	Q7	Q8	QB
	1	0	0	0	1	1	0	0	0	1	1	0	0	0
	2	V_{dc}	0	V_{dc}	0	0	0	1	1	0	0	1	1	0
	3	2 V_{dc}	0	2 V_{dc}	1	0	0	1	0	1	1	0	0	0
	4	0	3 V_{dc}	3 V_{dc}	1	1	0	0	0	0	0	0	1	1
	5	V_{dc}	3 V_{dc}	4 V_{dc}	0	0	0	1	1	0	0	0	1	1
	6	2 V_{dc}	3 V_{dc}	5 V_{dc}	1	0	0	1	0	0	0	0	1	1
	7	0	6 V_{dc}	6 V_{dc}	1	1	0	0	0	1	0	0	1	0
	8	V_{dc}	6 V_{dc}	7 V_{dc}	0	0	0	1	1	1	0	0	1	0
	9	2 V_{dc}	6 V_{dc}	8 V_{dc}	1	0	0	1	0	1	0	0	1	0
	10	- V_{dc}	0	- V_{dc}	0	1	0	0	1	1	1	0	0	0
	11	-2 V_{dc}	0	-2 V_{dc}	0	1	1	0	0	1	1	0	0	0
	12	0	-3 V_{dc}	-3 V_{dc}	1	1	0	0	0	0	1	0	0	1
	13	- V_{dc}	-3 V_{dc}	-4 V_{dc}	0	1	0	0	1	0	1	0	0	1
	14	-2 V_{dc}	-3 V_{dc}	-5 V_{dc}	0	1	1	0	0	0	1	0	0	1
	15	0	-6 V_{dc}	-6 V_{dc}	1	1	0	0	0	0	1	1	0	0
	16	- V_{dc}	-6 V_{dc}	-7 V_{dc}	0	1	0	0	1	0	1	1	0	0
	17	-2 V_{dc}	-6 V_{dc}	-8 V_{dc}	0	1	1	0	0	0	1	1	0	0

$$mi = \frac{h_1}{8\,V_{dc}} \quad (1)$$

$$h_1 = \frac{4V_{dc}}{\pi}[\cos(\theta_1) + \cos(\theta_2)] \quad (2)$$

$$h_1 = \frac{4V_{dc}}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)] \quad (3)$$

$$h_n = \frac{4V_{dc}}{n\pi}[\cos(\theta_1) + \cos(\theta_2)], \quad n = 3, 5, 7, ... \quad (4)$$

$$h_n = \frac{4V_{dc}}{n\pi}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)], \quad n = 3, 5, 7, ... \quad (5)$$

$$h_n = \frac{4V_{dc}}{n\pi}\sum_{i=1}^{8}\cos(\theta_i), \quad n = 1, 3, 5, 7, ... \quad (6)$$

Where $0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \theta_5 < \theta_6 < \theta_7 < \theta_8 < \frac{\pi}{2}$

The total harmonic distortion (THD) can be calculated as in Eq. (7)

$$\%\,THD = 100 \times \frac{\sqrt{(h_3^2 + h_5^2 + h_7^2 + \cdots.)}}{h_1} \quad (7)$$

In SHE technique, lower order harmonics are selected to be cancelled based on how many switching angles are exist. But in harmonic elimination technique the solution of the switching angles $(\theta_1, \theta_2, ...)$ are generated based on minimizing the value of THD of Eq. (6). It can be noticed that either in SHE technique or THD minimizing technique, the above equations can be solved using iteration method such as Newton Raphson or secant search engine [14 - 16] to satisfy the fundamental voltage and cancel lower harmonics up to 7 orders at the same time. Table 2 provides the lookup table solution for different modulation indexes. It could be noticed that the higher the modulation index (mi) the higher the number of voltage levels are required to achieve the inverter output voltage command. Also the percentage THD of the inverter output voltage decreases rapidly as the modulation index increases. Figures 2(a) and 2(b) give the lower order harmonics beside the fundamental voltage with changing modulation index. In case of very low modulation indexes at 0.1 and 0.2, the lower order harmonics especially the 3rd, 5th and 7th have significant values as compared to the fundamental because the behavior of the proposed MLI is typically similar to conventional two levels inverter. For other modulation indexes greater than or equal 0.3, more output voltage levels will appear and consequently more lower order harmonics can be cancelled. For example $mi = 0.7$ lower harmonic orders 3rd, 5th,7th, 9th are almost vanished.

Although fundamental frequency control scheme has many advantages as previously described, it has some drawbacks. Equations solution of the SHE technique is the main disadvantages of this method because it is a very complex and tedious work in addition the solution is not satisfied at certain modulation indexes. Thus applying this technique will lead to discontinuous range of control.

Table 2: Proposed inverter performance and switching angles for different values of mi at low frequency control

mi	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	h_1/V_{dc}	%THD
0.1	51.0	90	90	90	90	90	90	90	0.8	58.88
0.2	13.5	73.5	90	90	90	90	90	90	1.6	30.43
0.3	13.26	37.93	82.86	90	90	90	90	90	2.4	18.39
0.4	10.74	26.35	52.83	87.98	90	90	90	90	3.2	12.55
0.5	7.0	24.92	34.14	65.5	90	90	90	90	4	10.91
0.6	5.8	16.12	33.0	47.5	69.2	90	90	90	4.8	8.55
0.7	5.3	15.0	26.5	38.31	52.80	81.6	90	90	5.6	7.78
0.8	4.8	13.9	22.9	32.9	43.91	60.8	86.7	90	6.4	6.49
0.9	3.8	11.2	20.4	27.9	39.91	51.5	64	84.8	7.2	6.28
1.0	2.8	11.2	20.4	27.9	35.91	42.5	53.5	68.8	8	5.20

(B) PWM CONTROL SCHEME

The proposed MLI can also be controlled using the well-known sinusoidal pulse width modulation (SPWM) control scheme. SPWM control scheme advantage is that it has a continuous control range of modulation indexes. In SPWM control scheme a number of carriers signals are compared with a rectified sinusoidal signal with amplitude (A_m) to generate the inverter control signals. Eq. (8) gives the modulating signal. In the proposed MLI, 8 carrier signals with same magnitude (A_{cr}) and frequency but shifted by a dc level from each other. This shifted dc level equals to the carrier magnitude (A_{cr}). Boolean signals are generated from this comparison and thus the switches control pulses can be generated.

The comparison generates 8 signals ($L_a, L_b, L_c, L_d, L_e, L_f, L_g, L_h$) with low frequency and 8 signals ($H_a, H_b, H_c, H_d, H_e, H_f, H_g, H_h$) with switching frequency. In addition, zero crossing two signals P & N are generated from comparing the modulating sinusoidal signal with a zero dc value. Figure 3 (a) depicts the 8 carriers and the rectified sinusoidal signal. Figure 3(b) shows the 8 low frequency signals while figure 4(c) provides the 8 high frequency signals. Eq. (9) gives switches on/off control Boolean formula. As explained before the output voltage levels increases with increasing modulation index and its percentage THD decreases rapidly with increasing mitoo as shown in Figure 4.

$$A_m = mi * 6 * A_{cr} \quad (8)$$

$$P_2 = \bar{H}_a P_1 P_1 = P L_a$$

$$Q_1 = \left(H_b L_b + \bar{H}_c L_c + H_f L_f + \bar{H}_g L_g + H_i L_i\right) * P + \left(\bar{H}_a L_a + H_c L_c + \bar{H}_e L_e + H_g L_g + H_h L_h\right) * N + P_2$$

$$Q_2 = Q_6 = P_1 = P L_a$$

$$Q_3 = \left(H_c L_c + \bar{H}_e L_e + H_g L_g + \bar{H}_h L_h\right) * P + \left(H_b L_b + \bar{H}_c L_c + H_f L_f + \bar{H}_g L_g + H_i L_i\right) * N$$

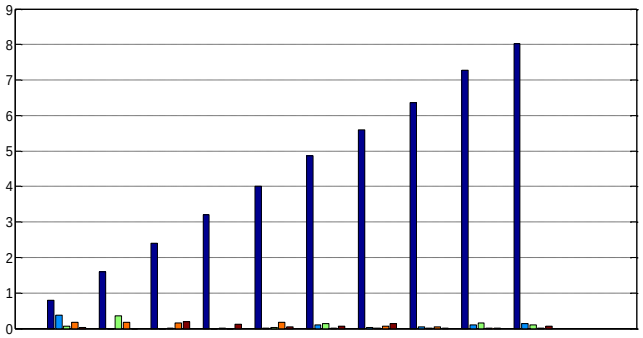
$$Q_4 = S_8 = P\bar{L}_a + \bar{P}_2 P_1$$

$$Q_5 = \left(H_g L_g + L_h + L_i\right) * P + (L_a + L_b + \bar{H}_c L_c) * N + P_2$$

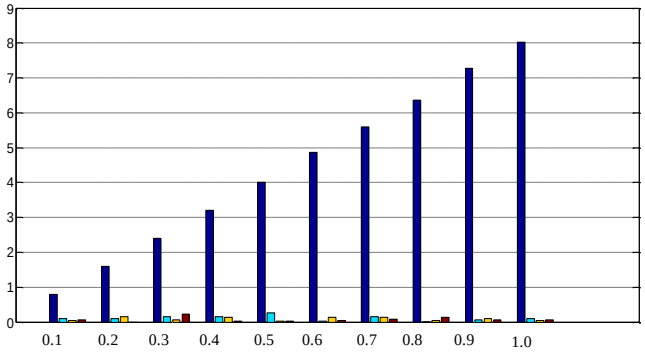
$$Q_7 = (L_b + \bar{H}_c L_c) * P + \left(L_h + L_i + \bar{H}_g L_g\right) * N + \bar{P}_2 P_1$$

$$Q_A = H_a L_a + \bar{H}_b L_b + H_e L_e + \bar{H}_f L_f + H_h L_h + \bar{H}_i L_i$$

$$Q_B = H_c L_c + \bar{H}_g L_g + L_e + L_f \quad (9)$$

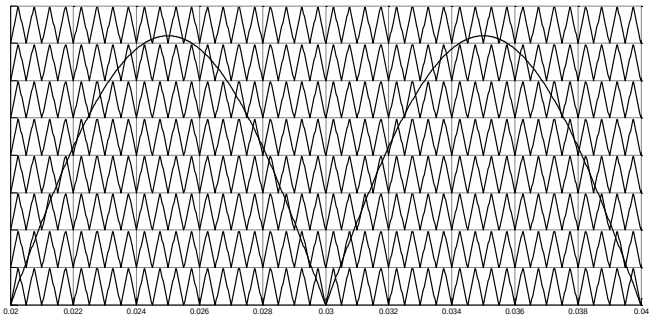


(a) Fundamental combined with 3, 5, 7, and 9 harmonic orders

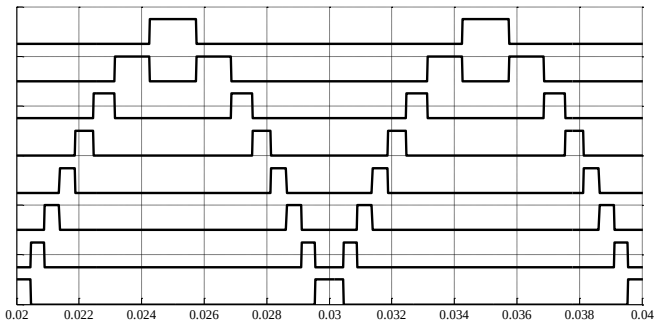


(b) Fundamental combined with 11, 13, and 15 harmonic orders.

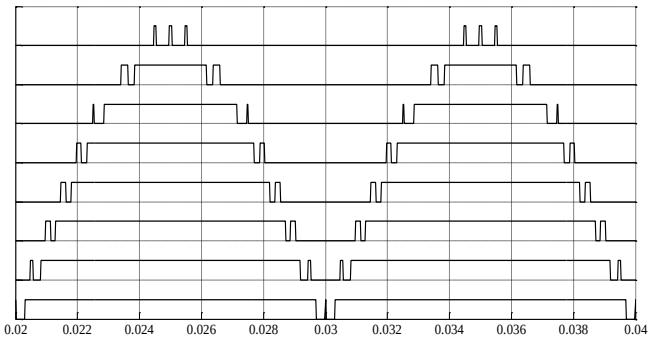
Figure 2. The normalized (v_{inv}/V_{dc}) MLI output voltage spectrum against $mi = 0.1 - 1$.



(a) Eight carriers and single modulating signal.



(b) Signals from bottom to top L1 – L8.



(c) Signals from bottom to top H1 – H8.

Figure 3. Generating of switches pulses using SPWM.

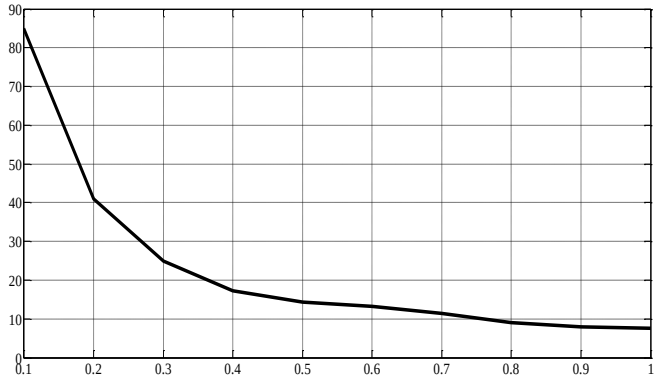


Figure 4. Percentage inverter output voltage THD Against modulation index (mi).

SIMULATION RESULTS

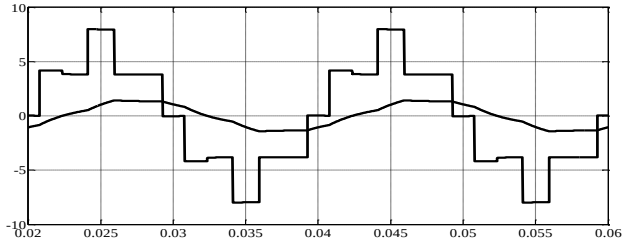
In this section, simulation results are illustrated for both low frequency and SPWM control schemes. The proposed MLI has been built and simulated using MATALB/Simulink package. The dc input voltage are V_{dc}=40V. In addition, the load is R-L with L=100mH and R=30Ω.Furthermore, in case of SPWM control scheme, the employed switching frequency is2kHz. Some selected results are provided to validate the proposed system.

Figure 5 shows the low frequency control scheme results for simulation. The studied cases are chosen to cover wide range of modulation indexes, they are mi = 0.2, 0.5, and 0.9. In this control method, the selected harmonic elimination technique is employed to fix the fundamental frequency and at the same time to cancel lower order harmonics. For example, for mi = 0.2, there are two steps in the output voltage and therefore it can attain the fundamental frequency voltage at a constant value and cancel only the third harmonic as shown in figure 5 (a) and 5 (d). For large mi, higher number of lower order harmonics can be cancelled as shown in figure 5(b) and 5(e) where third, fifth and seventh harmonics are cancelled. Also for mi = 0.9 as illustrated in figure 5(c) and 5(f) all lower order harmonics are cancelled or become less than 3% which can be considered negligible.

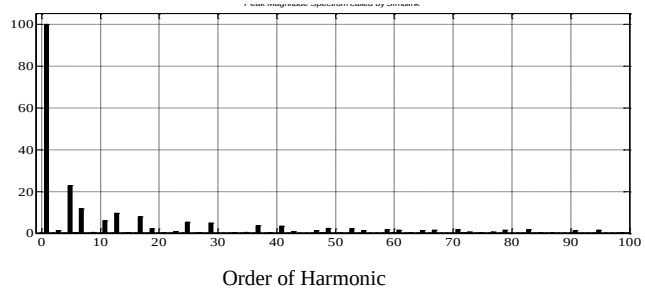
Figure 6 shows the SPWM simulation results. Also the studied cases are chosen to cover wide range of modulation indexes, they are mi = 0.2, 0.5, and 0.9 at switching frequency 2 kHz.

These aforementioned figures validate the proposed SPWM control scheme for the proposed topology and confirm that the proposed MLI can be considered as a high performance MLI from the point of view of power electronic components used because it can generate up to 17 voltage levels using only 10 power switches in addition 8 main diodes. Consequently the level-switch ratio (LSR) is 1.7.

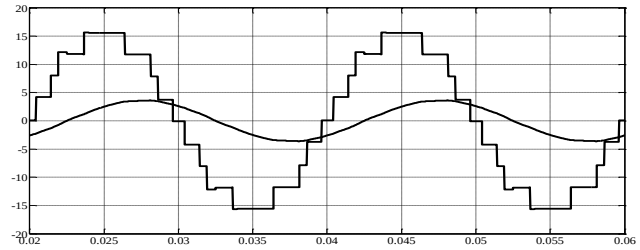
Figure 7 illustrates the output voltage of upper and lower modules in case of SPWM control at mi = 0.9. It can be noticed that upper module switches operate at the switching frequency and low voltage. On the other hand, lower module switches operate at almost power frequency and high voltage. Moreover control signals of switches are shown in figure 8 where upper and lower module switches operate at switching frequencies as previously described. Thus the overall losses of the switches could be reduced and this is one of the main advantages of the proposed MLI.



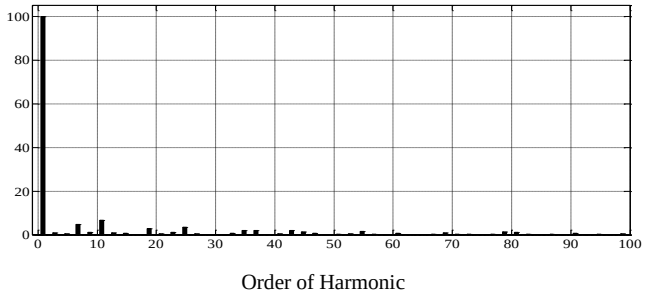
(a) Voltage and current at low switching for mi= 0.2, R= 30 Ohm , L = 100 mH (current scale = 1:1, voltage scale = 1:10).



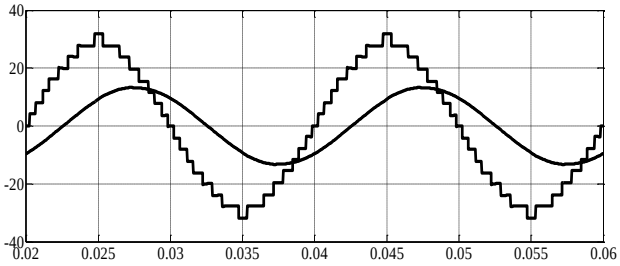
(b) Percentage output voltage spectrum at low switching for mi= 0.2, R= 30 Ohm , L = 100 mH.



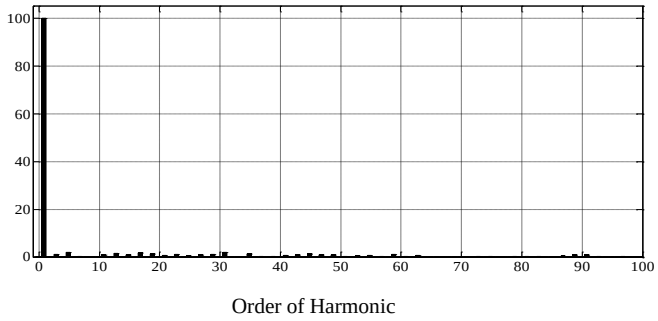
(c) Voltage and current at low switching for mi= 0.5, R= 30 Ohm, L = 100 mH (current scale = 1:1, voltage scale = 1:10).



(d) Percentage output voltage spectrum at low switching for mi= 0.5, R= 30 Ohm , L = 100 mH.



(e) Voltage and current at low switching for mi= 0.9, R= 30 Ohm , L = 100 mH (current scale = 2:1, voltage scale = 1:10).



(f) Percentage output voltage spectrum at low switching for mi= 0.9, R= 30 Ohm, L = 100 mH.

Figure 5. Low frequency simulation results of the proposed MLI for different values of mi.

PROPOSED MLI MODULARITY

The proposed topology in this paper has a modular performance; therefore other modules can be added to figure 1 without changing the main inverter configuration. As a result more levels can be achieved. The ratio among the input dc voltage of inverter modules is 2:6:18: …, which means the general ratio of the inverter is 1:3. Assuming that the output voltages of the modules are $v_{o1}, v_{o2}, v_{o3}, \dots, v_{on}$, the inverter output voltage is given by:

$$v_{inv}(t) = v_{o1}(t) + v_{o2}(t) + v_{o3}(t) + \cdots + v_{on}(t) \quad (10)$$

The number of switches N_{switch} and the number of the diodes N_{diodes} are giving by the following equations

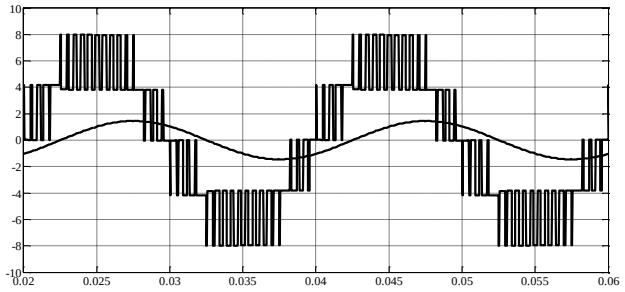
$$N_{switch} = 4\times n + n \quad (11)$$

$$N_{diodes} = 4\times n \quad (12)$$

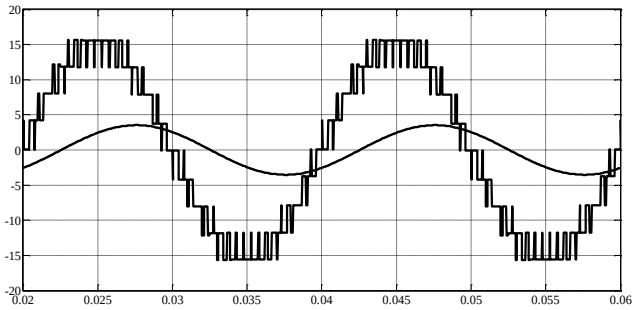
Where n is the number of inverter modules. The number of the output voltage levels is varying according to the symmetrical or asymmetrical voltage. The number of the output voltage levels N_{Levels} for symmetrical and asymmetrical structure is calculated as follows:

$$N_{Levels} = 3^n - 1 \quad \text{(symmetrical)} \quad (13)$$

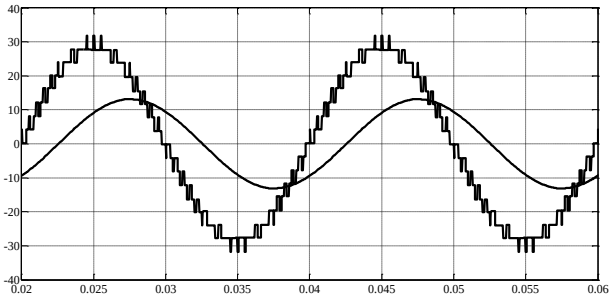
$$N_{Levels} = 2\times 3^n - 1 \quad \text{(asymmetrical)} \quad (14)$$



(a) Voltage and current employing PWM control at mi = 0.2, f_s = 2 kHz, R= 30 Ohm, L = 100 mH (current scale = 1:1, voltage scale =110).



(b) Voltage and current employing PWM control at mi = 0.5, f_s = 2 kHz, R= 30 Ohm, L = 100 mH (current scale = 1:1, voltage scale = 1:10).



(c) Voltage and current employing PWM control at mi = 0.9, f_s = 2 kHz, R= 30 Ohm, L = 100 mH (current scale = 2:1, voltage scale = 1:10).

Figure6. Simulation results for SPMW control of the proposed MLI for different values of mi.

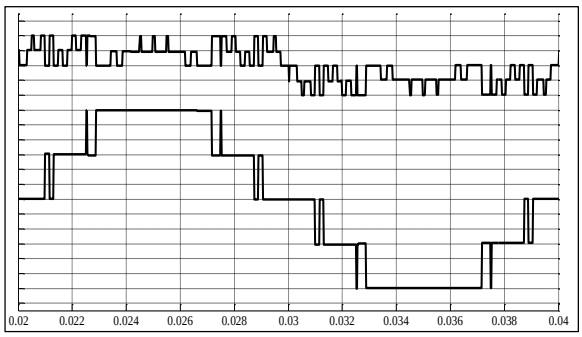


Figure 7. Simulation results of output voltage of upper and lower modules in case of PWM control at mi = 0.9, f_s = 2 kHz (bottom is lower module and top is upper module).

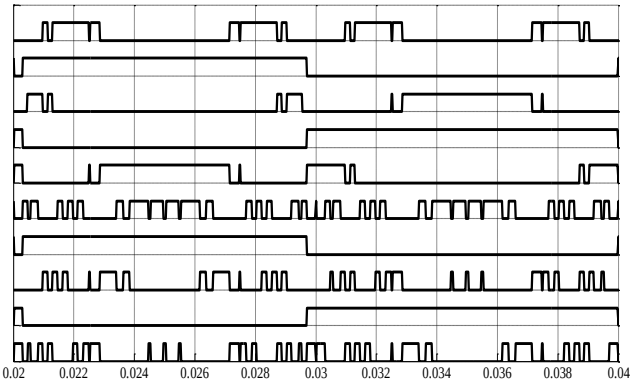


Figure 8. Control signals of switches in case of PWM control at mi = 0.9, f_s = 2 kHz (bottom to top Q1, Q2, Q3, Q4, QA, Q5, Q6, Q7, Q8, QB).

COMPARISON BETWEENTHE PROPOSED MLI AND EXISTING MLI

Comparison between the proposed MLI topology and other existing counterparts MLI topologies have been done in this section. The comparison considers switches number, number of main diodes, output voltage levels, types of MLI configuration, switches voltage stresses and THD performance of output voltage waveform. For fair comparison between the proposed topology and its counterparts existence topologies, the output peak voltage is assumed to be fixed at V_p. The number of the output voltage levels of the proposed topology is about twice that of symmetrical scheme [9]. This comparison is given in Table 3 and it reveals that the proposed topology has higher LSR and less switches voltage stresses. It also has high performance due to low THD value.

CONCLUSION

In this paper, a new asymmetrical cascaded seventeen levels single-phase inverter is proposed. The proposed inverter has extreme levels to switch ratio (LSR) which reaches 1.7 in addition, the proposed MLI is considered as a modular which means it can be extended by adding more modules to achieve more output voltage levels. The proposed inverter operational principles and switches times diagram have been provided. Both fundamental frequency and the multicarrier PWM control techniques have been employed to generate switches pulses. Half of the proposed MLI switches operate at the switching frequency and at low voltage while the other half switches turn on and off at almost power frequency and at high voltage. Consequently the MLI switching losses is decreased. The performance of the proposed topology has been validated using simulation results for an inductive load. The output voltage THD shows that it has as low as 5.2%.

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Table 3. Comparison between the proposed MLI topology and two other systems for fixed peak output voltage.

	Ref. [7]	Ref. [9]	Proposed topology
Number of switches	8	10	10
Number of main diodes	0	8	8
Output voltage level	7	9	17
LSR	0.875	0.9	1.7
Type of MLI	Asymmetric	symmetric	Asymmetric
Switches voltage stresses	4 switches (sw) = $V_p/3$ 4 sw = $2V_p/3$	8 sw = $V_p/2$ 2 sw = $V_p/4$ 8 diodes = $V_p/4$	4 sw = $V_p/4$, 4 sw = $3V_p/4$, 1 sw = $V_p/8$ 4 diodes = $V_p/8$, 1 sw = $3V_p/8$, 4 diodes = $3V_p/8$
Summation of all Switches voltage stresses	$4V_p$	$4.5V_p$	$4.5V_p$
%THD of output voltage at $mi = 0.8$	24.42	10.12	6.49

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