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High Speed VLSI Architecture for Squaring Binary Numbers Using Yavadunam Sutra and Bit Reduction Technique

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Abstract

The boom of high speed recent communication hardly requires the efficient Mathematical operations. The favored performance outcomes of any architecture are possible only by the effective Mathematical operations. Squaring plays an essential role in high speed applications like animation, Digital signal processing, and image processing, etc. where the speed is a crucial performance characteristic. The squaring operation involves more computing time; hence the speed of the squaring operation has to be improved. This paper explains about the proposed squaring architecture using Yavadunam which is one of the sutras of the ancient Indian Vedic Mathematics. The deficiency is obtained from Yavadunam thereby reducing the deficiency bit size to N-1 bits. Here the bit size is constantly sustained to N-1 bits. Thereby N*N bit multiplier is replaced by N-1*N-1. The proposed architecture results in reduced usage of components with reduction in critical path delay and increased speed.

Keywords: Squaring, Vedic Mathematics, Yavadunam Sutra, Bit reduction

INTRODUCTION

The emerging trends in Science and Technology results in high speed applications. Digitalization has made us to concentrate in speed of the devices than other performance outcomes [3]. In most of the high speed applications squaring operation plays an important role. Among all the arithmetic operations the multiplication and squaring operations are the most essential one. To achieve high performance several architectures are being adopted [8].The performance analysis of any circuit is estimated by two main parameters area and speed. In many applications multipliers are used to find the squares or other orders of power operations. Hence to obtain the square of a binary number fast multipliers are used. In many high speed applications some of the prompt multipliers like Braun, Wallace tree, Dadda multiplier; Baugh-Wooley methods of 2's complement, Booth multiplier are being used. In the midst of all Booth's algorithm and Recursive decomposition are more effective [7].Other than the conventional multipliers, the Vedic multipliers are also emerging into the trends. The Vedic multipliers based on Vedic sutras, most likely Urdhava Tiryagbhyam and Nikhilam Sutras are commonly in practice [2], [5]. On comparing Vedic multipliers with the conventional ones Vedic multipliers are fast and takes up less area [1].Yavadunam Tavadunikrtya Vargancha Yojayet, an Upa sutra of Yavadunam sutra is a typical sutra for squaring.

Vedic Mathematics is a very old Mathematic method given to us by our ancient saints. This was revived by Swami Bharati Krishna Tirthaji Maharaj. The entire computations are done with the help of anyone of the 16 Sutras or 13 Upa sutras, the word formulae which assist to solve the whole variety of the mathematical problems [6].Any sutra or Upa sutra can be put together to solve any hassle and it is not essential for the student to stick to any specific formulation. Moreover they can formulate distinct strategies. As a result Vedic maths is speedy, fascinating, contemporary, develops logical thinking and interpretation talents and rational [6].In Vedic Maths the multiplication operation can be certainly be turned around to accomplish one-line division of decimal numbers. Similarly the simple squaring method can be turned into a one line square root of decimal number [6].

RELATED WORK

To attain the square of the binary number multipliers like Braun Array, Baugh Wooley methods of two's complement, Booth multiplier, Wallace trees, Dadda, etc are unbelievable in their performances [7].But at present they ensue to be obsolete due to the raising trends in high speed communication and many novel techniques are promising for further more faster operations. In **[**9**]** Urdhava sutra has been used to perform squaring**.** Here the delay has been reduced as the computation of partial products and addition of the partial products are performed concurrently. However area has been increased as 4 Vedic multipliers are used to square a n bit binary number. [7] Has proposed a high speed binary squaring architecture using Vertical and crosswise method. The delay has been reduced but the implementation used two squaring circuits thereby resulting in increase in device utilisation. [10] Proposed a high speed FPGA based squaring circuit using Peasant Multiplication, an ancient Egyptian technique, means mediation and duplation, which means dividing one number by 2 and doubling-up the other. The

realisation states that it occupies more area. In [4] a 4 bit binary squaring using Dwandayoga sutra is designed. It is quite faster and simple to compute when compared to the traditional techniques. It has been proved only for 4 bits and as the number of bits increases it becomes complicated. Until now there is no standard architecture available for the squaring sutra Yavadunam. It is quite difficult to design a particular architecture as the sources of input will be from various ranges. To overcome this problem the same view can be extended for the binary numbers [11]. In the previous paper [11] a unique hardware has been designed for a squaring sutra, Yavadunam. In this paper the same has been modified by applying bit reduction technique to reduce the delay.

DESIGN OF THE PROPOSED SQUARING ARCHITECTURE

Yavadunam Sutra is one of the squaring sutra of Vedic mathematics .It is a precise method to calculate square of numbers with the specific condition that the number to be squared should be close to the power of 10. The general idea of this sutra is whatsoever the deficits lessen by that amount and set up the square of the deficiency [6].Yavadunam Tavadunikrtya Vargancha Yojayet is an Upa sutra of Yavadunam.

The proposed method is to amend the existing squaring architecture in order to achieve the progress in area, speed and power. To accomplish this uniform transform technique is followed and thereby weight reduction is made by getting rid of the Most Significant Bit. After bit reduction Yavadunam Sutra is implemented to obtain the square of the given number. By proposing this modification to the existing architecture the number of bits to the squaring architecture is reduced. Also the number of components used can be reduced thereby reducing the power and delay.Let us consider a squaring of 4 bits binary number $A_3A_2A_1A_0$ .Weight reduction is made and the MSB is removed. Now the input to the architecture becomes $A_2A_1A_0$, a 3bit binary number. Now the base for the 3 bit number is 8. The output of the squaring architecture will be more than 4 bits. Since the input is 4 bits the output will be 8 bits if the number to be squared is greater than 2^{N-1} and the output will be 6 bits if the number to be squared is less than 2^{N-1}.Squaring of binary numbers involves two modes. One of the modes is when the deficiency is positive i.e. if the given number is greater than 2^{N-1} , the base value. For example if number is 12 the base value is 8 and the deficiency is +4.And the other mode is when the deficiency is negative i.e. if the given number is less than 2^{N-1} , the base value. For example if number is 4 the base value is 8 and the deficiency is -4.

Mode: 1 The given number is greater than 2^{N-1} .

Mode: 2 The given number is lesser than 2^{N-1} .

Algorithm for Mode: 1

INPUT: $A_3A_2A_1A_0$

OUTPUT: $B_{7\ldots}B_2B_1B_0$

Step:1) Reduce the weight of the input by removing the MSB, now input becomes $A_2A_1A_0$ which is the deficiency.

Step:2) Let the deficiency be $D_2D_1D_0 = A_2A_1A_0$

Step:3) Square the deficiency, output of squaring=$X_{5\ldots}X_2X_1X_0$

Carry = $X_5X_4\ X_3$ and now

LHS =$X_2X_1X_0 = B_2B_1B_0$

*Step:4)*Add the deficiency and the input

$A_3A_2A_1A_0 + D_2D_1D_0 = Y_4Y_3Y_2Y_1Y_0$

Step:6) Add the above output to the carry of the LHS

$Y_4Y_3Y_2Y_1Y_0 + X_2X_1X_0 = B_7B_6B_5B_4\ B_3$ =RHS

Step:7) Concatenating LHS and RHS ,the output is

$B_7B_6B_5B_4B_3B_2B_1B_0$ =square of $A_3A_2A_1A_0$

Algorithm for Mode: 2

INPUT: $A_3A_2A_1A_0$

OUTPUT: $B_{5\ldots}B_2B_1B_0$

Step:1) Reduce the weight of the input by removing the MSB, now input becomes $A_2A_1A_0$.

Step:2) Take two's complement of $A_2A_1A_0$,the output is the deficiency. Let the deficiency be

$D_2D_1D_0 = A_2A_1A_0$

Step:3) Square the deficiency,

output of squaring=$X_{5\ldots}X_2X_1X_0$

Carry = $X_5X_4\ X_3$ and now

LHS =$X_2X_1X_0 = B_2B_1B_0$

Step:4) Subtract the deficiency from the bit reduced number $A_2A_1A_0 - D_2D_1D_0 = Y_2Y_1Y_0$

Step:5) If the subtractor output is positive then add the above output to the carry $X_5X_4\ X_3$.

$Y_2Y_1Y_0 + X_5X_4X_3 = B_5B_4\ B_3$ =RHS

Step:6) If the subtractor output is negative then subtract the output Y2Y1Y0 from the carry $X_5X_4X_3$. i.e. $X_5X_4X_3 - Y_2Y_1Y_0 = B_5B_4\ B_3$ =RHS

Step:7) Concatenating LHS and RHS ,

the output is $B_5B_4B_3B_2B_1B_0$ =square of $A_3A_2A_1A_0$

Both the modes are combined into a single architecture. The number greater than or lesser than 2^{N-1} can be identified from the Most Significant Bit of the numbers. The control signal to the multiplexer depends on the Most Significant Bit of the

input i.e.A_{N-1}.If the MSB of the number is 0 then the number is two's complemented after bit reduction and then squared. If the MSB of the number is 1 then the number is directly subject to bit reduction and squared thereby skipping two's complement block. The control signal to select the adder or subtractor depends on the Most Significant Bit of the input i.e.A_{N-1}.When the number is greater than 2^{N-1} , A_{N-1} will be 1 and adder will be selected and the output of the adder will be added with the carry. In other case if the number is less than 2^{N-1}, A_{N-1} will be 0 and the subtractor will be selected. Similarly the control signal to select the carry adder or subtractor depends on the output Y_{N-1}. If Y_{N-1} is 0 then carry will be added else the subtractor will be selected.

RESULT AND DISCUSSION

The hardware implementation of the squaring architecture for binary numbers is designed. The same is implemented with Xilinx Spartan kit. The simulated output of a 4bit weight reduced squaring architecture is shown in the Figure 1. Figure 2 depicts the RTL schematic of the squaring architecture. The device utilisation summary of the proposed method is depicted in the Table 1. The Table 1 reveals that the squaring architecture reported in [11] utilises more devices when compared to our proposed method. Also our proposed method is faster compared to architecture reported by Deepa & Marimuthu in [11]. By this means it is clear that the proposed architecture is efficient in speed and area.

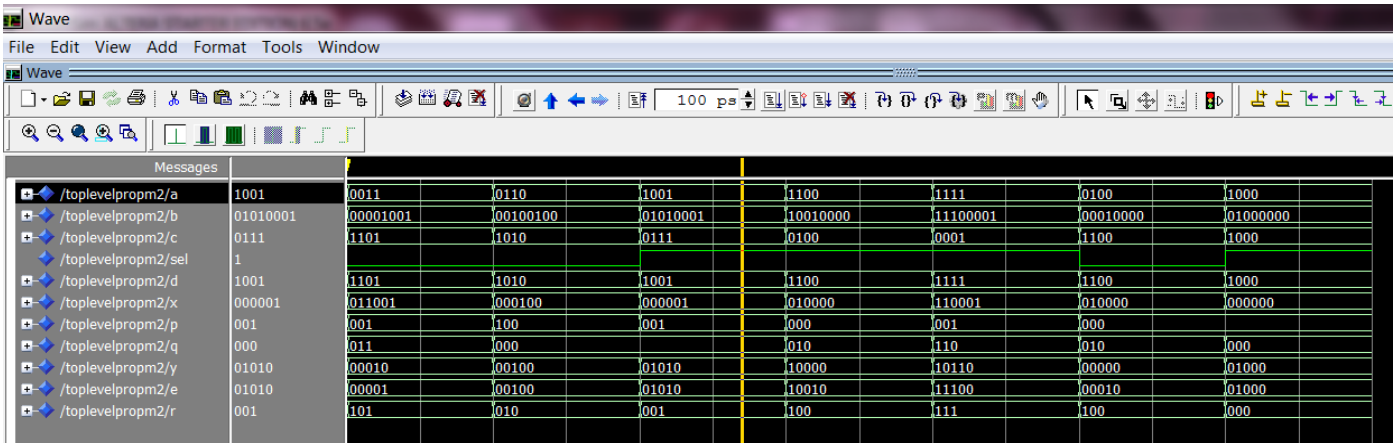

Figure 1. Simulation output

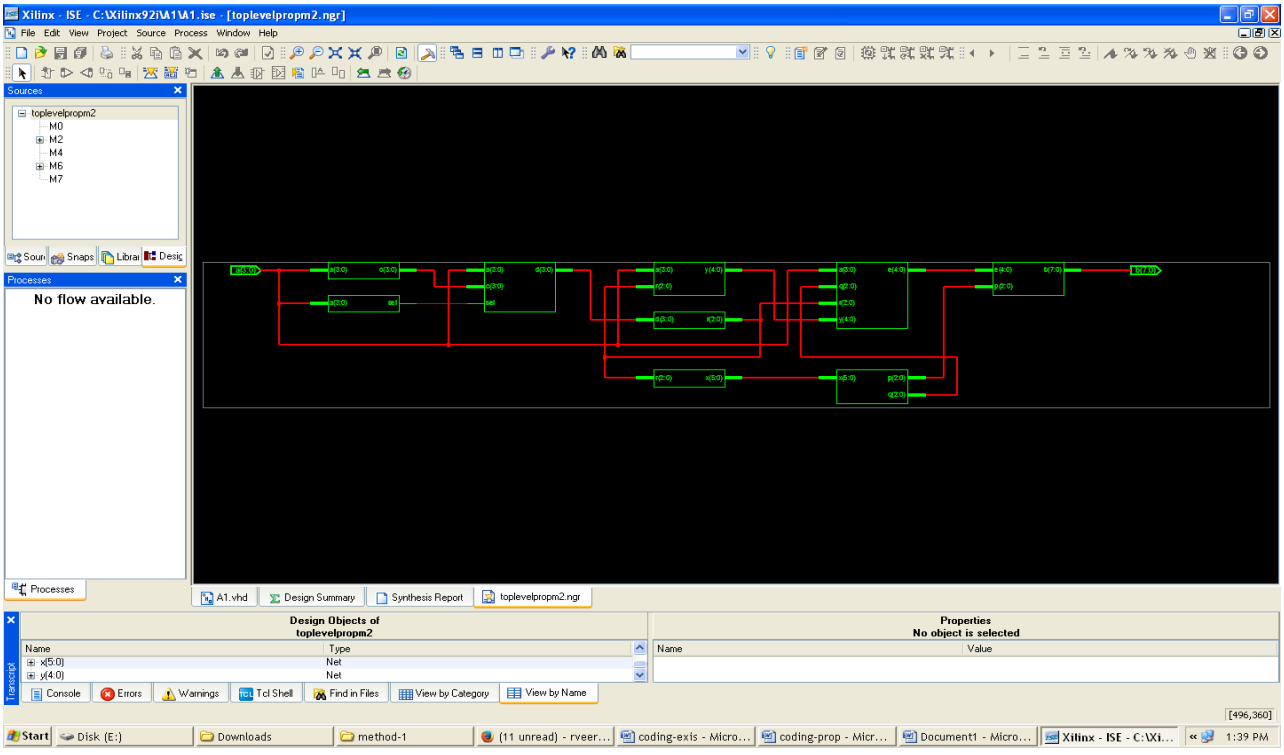

Figure 2. RTL Schematic

Table 1. Device utilisation summary

S.NO	DEVICE UTILIZATION	Deepa & Marimuthu[11]	PROPOSED ARCHITECTURE
1.	Number of slices	10 out of 3584	13 out of 1920
2.	Number of slice FFs	3 out of 7168	4 out of 3840
3.	Number of 4 input LUTs	17 out of 7168	23 out of 3840
4.	Number of IOs	12	12
5.	Number of bounded IOBs	12 out of 141	12 out of 141
6.	Number of mult18*18s	1 out of 16	-
7.	Delay in nS	17.404	17.293

CONCLUSION AND FUTURE WORK

We have presented a Vedic squaring architecture based on the Yavadunam algorithm .The speed of the Yavadunam squaring algorithm is improved. By using the bit reduction technique, number of components used can be reduced, thereby reducing the delay and improving the speed. On the whole this proposed architecture optimises the area and the speed. The future work is to design a proposed architecture for multiplication of the given numbers using Yavadunam Sutra.

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