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PV Based Buck–Boost Voltage/Current Source Inverter using Space Vector Pulse Width Amplitude Modulation Technique

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Abstract

This paper proposes a pv based buck-boost voltage/current source inverter using space vector pulse width amplitude modulation technique. For a voltage source inverter, the switching loss is reduced by 89%, compared to a conventional sinusoidal pulse width modulation (SPWM) method. For a current source inverter, the switching loss is reduced by 65%. In both cases, the power density is increased by a factor of 2 to 3. In addition, it is also verified that the output harmonic distortions of SVPWAM is lower than SPWM, by only using one-third switching frequency of the latter one. A 1-kW boost-converter-inverter prototype has been built and tested using this modulation method. The maxi-mum overall system efficiency of 97.7% has been attained at full power rating. As a result, it is feasible to use SVPWAM to make the buck–boost inverter suitable for applications that require high efficiency, high power density, high temperature, and low cost. Such applications include electric vehicle motor drive or engine starter/alternator.

Keywords: Buck-boost, SVPWAM, switching loss reduction, THD.

INTRODUCTION

URRENTLY, two existing inverter topologies are used **C** for hybrid electric vehicles (HEVs) and electric vehicles (EVs): the conventional three-phase inverter with a high volt-age battery and a three-phase pulse width modulation (PWM) inverter with a dc/dc boost front end. The conventional PWM inverter imposes high stress on switching devices and motor thus limits the motor's constant power speed range (CPSR), which can be alleviated through the dc–dc boosted PWM inverter.

Fig. 1 shows a typical configuration of the series plug-in electric vehicle (PHEV). The inverter is required to inject low harmonic current to the motor, in order to reduce the winding loss and core loss. For this purpose, the switching frequency of the inverter is designed within a high range from 15 to 20 kHz, resulting in the switching loss increase in switching device and also the core loss increase in the motor stator. To solve this problem, various soft-switching methods have been proposed [1]–[3]. Active switching rectifier or a diode rectifier with small DC link capacitor have been proposed in [4], [5], [8]–[12].

Varies types of modulation method have been proposed previously such as optimized pulse-width-modulation[13],improved Space-Vector-PWM control for different optimization targets and applications [14]–[16], and discontinuous PWM (DPWM) [17]. Different switching.

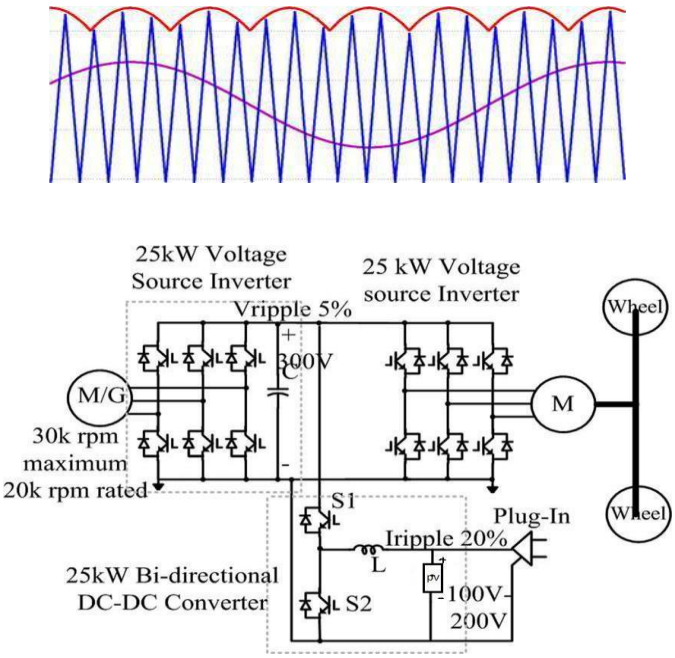


Figure 1. Typical configuration of a series PHEV.

Sequence arrangement can also affect the harmonics, power loss and voltage/current ripples [18]. DPWM has been widely used to reduce the switching frequency, by selecting only one zero vector in one sector. It results in 50% switching frequency reduction. However, if an equal out-put THD is required, DPWM cannot reduce switching loss than SPWM. Moreover, it will worsen the device heat transfer because the temperature variation. A double 120 flattop modulation method has been proposed in [6] and [7] to reduce the period of PWM switching to only 1/3 of the whole fundamental period. However, these papers did not compare the spectrum of this method with others, which is not fair. In addition, the

method is only specified to a fixed topology, which cannot be applied widely.

This paper proposes a novel generalized PV based space vector pulse width amplitude modulation (SVPWAM) method for the buck/boost voltage source inverter (VSI) and current source in-verter (CSI). By eliminating the conventional zero vector in the space vector modulation, two-third and one-third switching frequency reduction can be achieved in VSI and CSI, respec-tively. If a unity power factor is assumed, an 89% switching loss reduction can be implemented in VSI, and a 65% reduction can be implemented in CSI. A 1-kW boost-converter inverter system has been developed and tested based on the SVPWAM method. A 90% power loss reduction compared to SPWM has been observed. The two stage efficiency reaches 97.7% at the full power rating. The power volume density of the prototype is 2.3 kW/L. The total weight of the system is 1.51 lb. Therefore, a high-efficiency, high-power density, high-temperature, and low - cost 1-kW inverter is achieved by using an SVPWAM method.

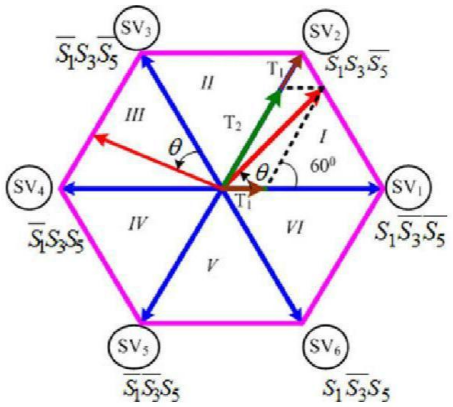


Figure. 2. SVPWAM for VSI.

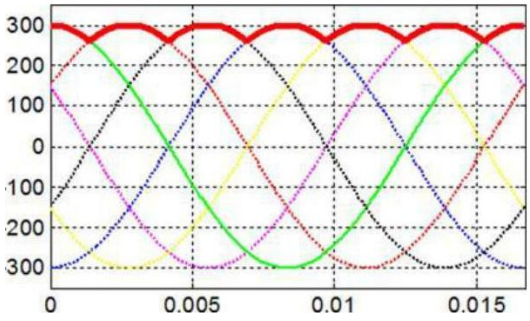


Figure. 3. DC-link voltage of SVPWAM in VSI.

SVPWAM FOR VSI

A. Principle of SVPWAM Control in VSI

The principle of an SVPWAM control is to eliminate the zero vector in each sector. The modulation principle of SVPWAM is shown in Fig. 2. In each sector, only one phase leg is doing PWM Switchin; thus, the switching frequency is reduced by two – third this imposes zero switching for one phase leg in the adjacent two setors. For example, in sector VI and I, phase leg A has no switching at all. The dc link voltage thus is directly generated from the output line to line voltage. In sector I no zero vector is selected. Therefore, *S*1 and *S*2 keep constant ON, and *S*3 and *S*6 are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-line voltage *V*ac at this time. The region In VSI, the device voltage stress is equal to dc-link voltage *V*DC, and the current stress is equal to output current *ia* . Thus the switching loss for each switch is

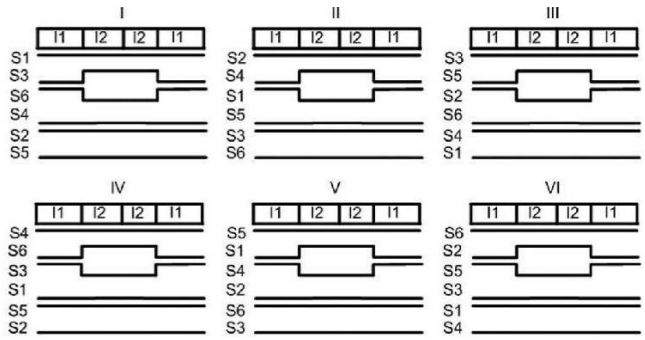


Figure 4. Vector placement in each sector for VSI.

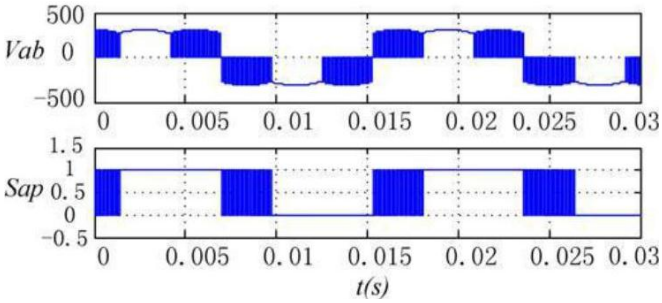


Figure 5. Theoretic waveforms of dc-link voltage, output line-to-line voltage and switching signals.

where $\theta \in [0, \pi/3]$ is relative angle from the output voltage vector to the first adjacent basic voltage vector like in Fig. 2. If the time period for each vector maintains the same, the switching frequency will vary with angle, which results in a variable inductor current ripple and multi frequency output harmonics. Therefore, in order to keep the switching period constant but still keep the same pulse width as the original one, the new time periods can be calculated as

$$T1\text{-}/T_s = T1/(T1 + T2) \qquad (2)$$

The vector placement within one switching cycle in each sector is shown in Fig. 4. Fig. 5 shows the output line-to-line voltage and the switching signals of *S*1 .

B. Inverter switching Loss Reduction for VSI

For unity power factor case, the inverter switching loss is reduced by 89% because the voltage phase for PWM switching is within [-60, 60], at which the current is in the zero crossing.

original equations for time period *T*1 and *T*2 are

$T1=\sqrt{3}/2\ msin(60-\theta)\ T2=\sqrt{3}/2\ msin(\theta)$

$Psw=((2-\sqrt{3})/\pi).(Im VDC/Vref Iref)\ ESR \cdot fsw$ ..... *(3)*

where *E*SR, *V*ref , *I*ref are the references.

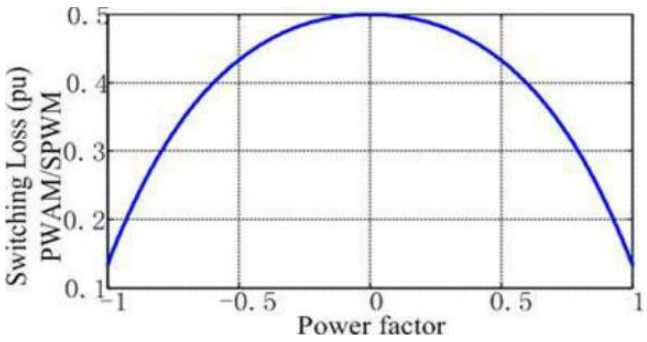


Figure 6. (SVPWAM power loss/SPWM power loss) versus power factor in VSI.

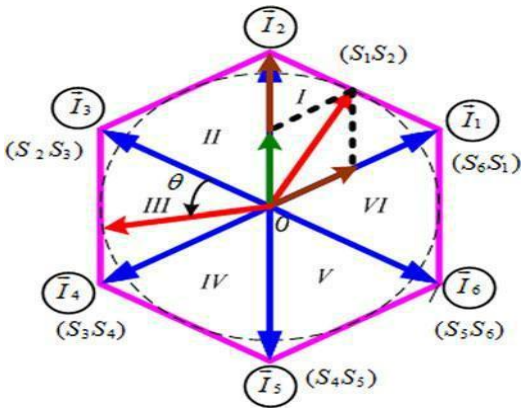


Figure 7. Conventional CSI and its corresponding SVPWAM diagram.

Since the SVPWAM only has PWM switching in two 60° sections, the integration over 2π can be narrowed down into integration within two 60°

$PSW\ I = (2\sqrt{3})/\pi \cdot (Im\ VD\ C/(Vref\ Iref)) \cdot$

$ESR \cdot fsw .$ (4)

The switching loss for a conventional SPWM method is

$PSW\ I\_ = (2/\pi) \cdot (Im\ VD\ C/(Vref\ Iref)) \cdot ESR \cdot fsw .$

……..(5)

In result, the switching loss of SVPWAM over SPWM is f = 13.4%. However, when the power factor decreases, the switching loss reduction amount decreases because the switching current increases as Fig. 6 shows.

As indicated, the worst case happens when power factor is equal to zero, where the switching loss reduction still reaches 50%. In conclusion, SVPWAM can bring the switching loss down by 50–89%.

SVPWAM FOR CSI

A. Principle of SVPWAM in CSI

The principle of SVPWAM in CSI is also to eliminate the zero vectors. As shown in Fig. 7, for each sector, only two switches are doing PWM switching, since only one switch in upper phase legs and one switch in lower phase legs are conducting together at any moment. Thus, for each switch, it only needs to do PWM

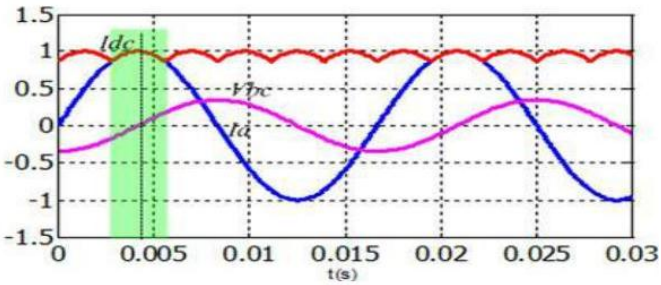
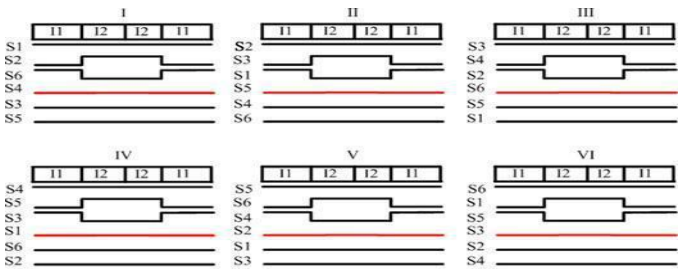


Figure 8. Switching voltage and current when pf = 1.



switching in two sectors, which is one-third of the switching period. Compared to SVPWM with single zero vector selected in each sector, this method brings down the switching frequency by one-third.

Similarly, the dc-link current in this case is a 6ω varied current. It is the maximum envelope of six output currents: *Ia*,

Ib , *Ic* , $-Ia$, $-Ib$, $-Ic$, as shown in Fig. 8. For example, in sector I,

*S*1 always keeps ON, so the dc-link current is equal to *Ia* . The difference between dc-link current in CSI and dc-link voltage in VSI is dc-link current in CSI is overlapped with the phase current, but dc-link voltage in VSI is overlapped with the line voltage, not the phase voltage.

The time intervals for two adjacent vectors can be calculated in the same way as (1) and (2). According to diagram in Fig. 7, the vector placement in each switching cycle for six switches can be plotted in Fig. 9.

The SVPWAM is implemented on conventional CSI through simulation. Fig. 10 shows the ideal waveforms of the dc current *I*dc , the output phase ac current and the switching signals of *S*1 . The switching signal has two sections of PWM in positive cycle, but no PWM in negative cycle at all.

B. Inverter Switching Loss Reduction for CSI

In CSI, the current stress on the switch is equal to the dc-link current, and the voltage stress is equal to output line-to-line voltage, as shown the shadow area in Fig. 8 Thus, the switching loss for a single switch is determined by

$$P_{\mathrm{SW\_CSI}} = \frac{2-\sqrt{3}}{\pi}\frac{\overline{i_{\mathrm{dc}}}\cdot V_{\mathrm{l-lpeak}}}{V_{\mathrm{ref}} I_{\mathrm{ref}}} E_{\mathrm{SR}} f_{\mathrm{sw}}. \qquad (6)$$

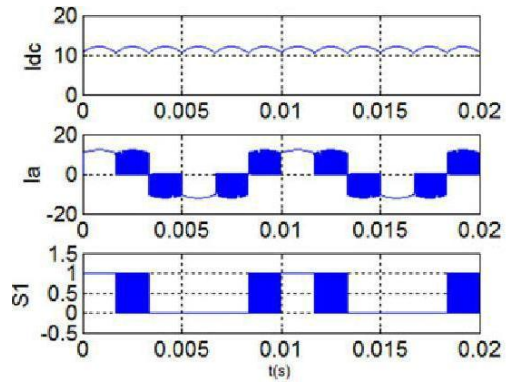


Figure 10. Theoretic waveforms of dc-link current, output line current and switching signals.

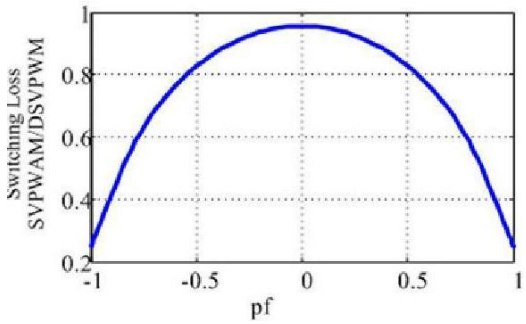


Figure 11. CSI switching loss ratio between SVPWAM and discontinuous SVPWM versus power factor.

When compared to discontinuous SVPWM, if the half switching frequency is utilized, then the switching loss of it becomes half of the result in (6). The corresponding switching loss ratio between SVPWAM and discontinuous SVPWM is shown in Fig. 11.

SPECTRUM ANALYSIS OF SVPWAM

A fair comparison in switching loss should be based on an equal output harmonics level. Thus, the switching loss may not be reduced if the switching frequency needs to be increased in order to compensate the harmonics. For example, discontinuous SVPWM has to have double switching frequency to achieve the same THD as continuous PWM. So the switching loss reduction is much smaller than 50%. Therefore, for the newly proposed SVPWAM, a spectrum analysis is conducted to be compared with other methods on the basis of an equal average switching frequency, which has not been considered in paper [16].

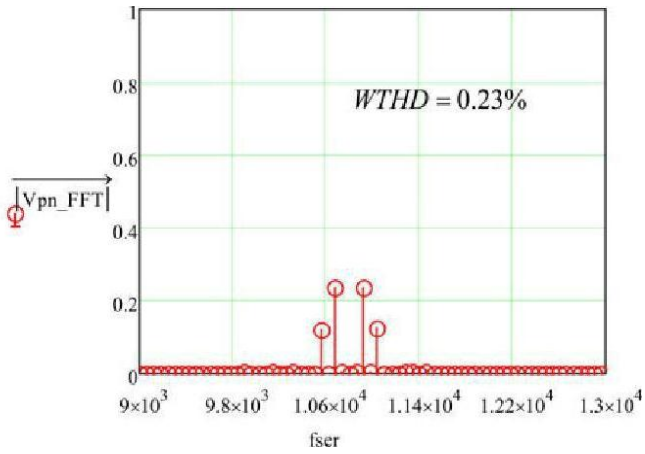


Figure 12. Spectrum of SPWM at switching frequency

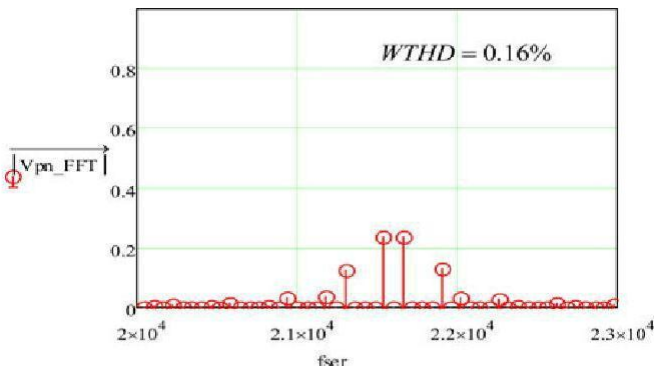


Figure 13. Spectrum of discontinuous SVPWM at switching frequency.

A. Spectrum Comparison Between SVPWAM, SPWM, and SVPWM

The object of spectrum analysis is the output voltage or current before the filter. The reason is that certain orders of har-

monics can be eliminated by sum of switching functions in VSI or subtraction of switching functions in CSI. The comparison is between SVPWAM, DPWM, and continuous SVPWM in VSI/CSI. The switching frequency selected for each method is different, because the comparison is built on an equalized average switching frequency over a whole fundamental cy-cle, in order to make the harmonics comparable at both low modulation and high modulation range. Assume that the base frequency is *f*0

= 10.8 kHz. Thus, 3*f*0 should be selected for SVPWAM, and *f*0 should be selected for continuous SVPWM in VSI. In CSI, 3*f*0 , 2*f*0 , and *f*0 should be selected for SVPWAM, discontinuous SVPWM, and continuous SVPWM, respectively.

The modulation index selected here is the maximum mod-ulation index 1.15, since the SVPWAM always only has the maximum modulation index. Theoretically, the THD varies with modulation index. The dc-link voltage is designed to be a constant for SVPWM and an ideal 6ω envelope of the output six line-to-line voltages for SVPWAM. Thus, the harmonic of the SVPWAM here does not contain the harmonics from the dc–dc converter output. It is direct comparison between two modulation methods from mathematics point of view.

Figs. 12–14 show the calculated spectrum magnitude at first side band of switching frequency range for three methods. It can be concluded that the ideal switching function of SVPWAM has less or comparable harmonics with SPWM and DPWM.

B. Analytical Double Fourier Expression for SVPWAM

The expression of double Fourier coefficient is

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\sum_{1}^{6}\int_{y_s(i)}^{y_e(i)}\int_{x_r(i)}^{x_f(i)} I_{dc}e^{j(mx+ny)}dxdy \qquad (7)$$

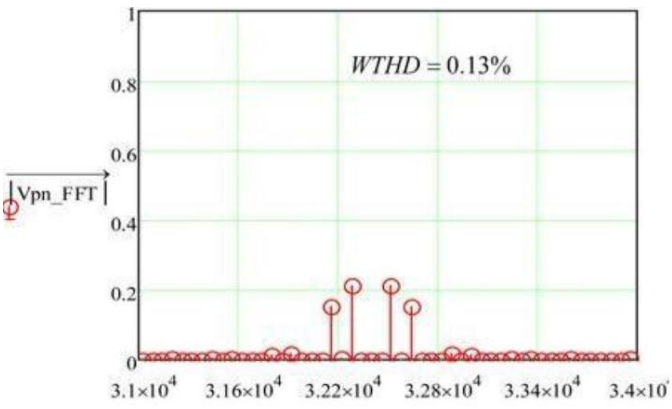


Figure 14. Spectrum of SVPWAM at switching frequency.

Table I: Integration limit for line-to-line voltage *V*a b (*t*)

i	ys(i)	ye(i)	xr(i)	xf(i)	Idc
1	0	$\frac{\pi}{3}$	xr1 = 0; xr2 = $\frac{\sin(\pi/3 - y)}{\sin(\pi/3 - y)}$	xf1 = $\frac{\sin(\pi/3 - y)}{\sin(\pi/3 - y)}$; xf2 = 2π	1
2	$\frac{\pi}{3}$	$\frac{2\pi}{3}$	xr = $\frac{\sin(2\pi/3 - y)}{\sin y}$	xf = $2\pi - \frac{\sin(2\pi/3 - y)}{\sin y}$	-1
3	$\frac{2\pi}{3}$	π	0	2π	-1
4	π	$\frac{4\pi}{3}$	xr1 = 0; xr2 = $\frac{\sin(4\pi/3 - y)}{\sin y}$	xf1 = $\pi \frac{\sin(4\pi/3 - y)}{\sin y}$; xf2 = 2π	-1
5	$\frac{4\pi}{3}$	$\frac{5\pi}{3}$	xr1 = $\frac{\sin(5\pi/3 - y)}{\sin(y-\pi)}$	xf1 = $2\pi - \frac{\sin(5\pi/3 - y)}{\sin(y-\pi)}$	1
6	$\frac{5\pi}{3}$	2π	0	2π	1

where $y \in [0, 2\pi]$ represents the fundamental cycle; $x \in [0, 2\pi]$ represents one switching cycle. The double Fourier expression coefficients can be derived as long as the rising edge of each PWM waveform is known.

$$V\text{ab}(t) = V\text{dc}(S1(t) - S3(t)). \qquad (8)$$

So its double Fourier equation is equal to the subtraction of two double fourier equations for switching functions. The voltage will be adopted during the motor start up as shown in Fig. 16. Hence, the system will achieve optimum efficiency when the motor is operating a little below or around nominal voltage.

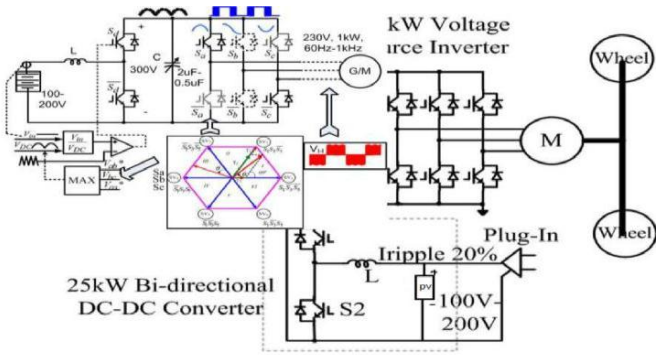


Figure 15. SVPWAM-based boost-converter-inverter motor drive system.

Integration limits for *V*ab (*t*) is shown in Tables I. The coeffi-cients finally could be simplified into a closed-form expression in terms of Bessel functions, which will not be discussed here.

TOPOLOGIES FOR SVPWAM

Basically, the topologies that can utilize SVPWAM have two stages: dc–dc conversion which converts a dc voltage or current into a 6ω varied dc-link voltage or current; VSI or CSI for which SVPWAM is applied. One typical example of this structure is the boost converter inverter discussed previously. However, the same function can also be implemented in a single stage, such as Z/quasi-Z/trans-Z source inverter [37]–[40].The front stage can also be integrated with inverter to form a single stage. Take current-fed quasi-Z-source inverter as an example. Instead of controlling the dc-link current *I*pn to have a constant average value, the the open zero state duty cycle *D*op will be regulated instantaneously to control *I*pm to have a 6ω fluctuate average value, resulting in a pulse type 6ω waveform at the real dc-link current *I*pn , since *I*1 is related to the input dc current *I*in by a transfer function

$$I_1 = \frac{1 - D_{op}}{1 - 2D_{op}} I_{in} \qquad (9)$$

CASE STUDY

1-KW BOOST-CONVERTER INVERTER FOR EV MOTOR DRIVE APPLICATION :

A. Basic Control Principle

The circuit schematic and control system for a 1-kW boostconverter inverter motor drive system is shown in Fig.

15. 6ω dc-link voltage is generated from a constant dc voltage by a boost converter, using open-loop control. Inverter then could be modulated by a SVPWAM method. The specifications for the system are PV input voltage is 100–200 V; the average dc-link voltage is 300 V; output line-to-line voltage rms is 230 V; and frequency is from 60 Hz to 1 kHz.

B. Voltage Constraint and Operation Region

It is worth noting that the SVPWAM technique can only be applied when the batteries voltage falls into the region

$$\sqrt{\quad} \quad \frac{3}{}$$

$Vin \leq \sqrt{2}\, Vl{-}l$ due to the step-up nature of boost converter.

The constraint is determined by the minimum point of the 6ω dc -link voltage. Beyond this region, conventional SPWM can be implemented. However, the dc-link voltage in this case still varies with 6ω because of the small film capacitor we selected. Thus, a modified SPWM with varying dc-link

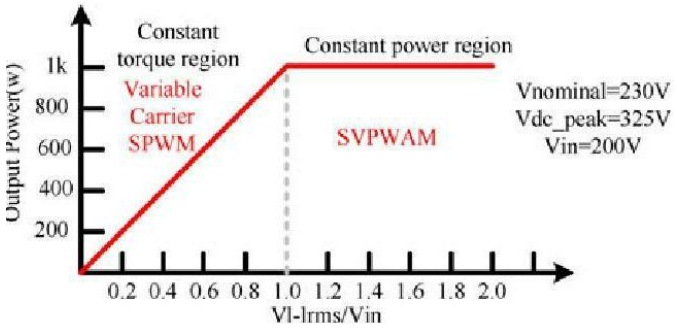


Figure 16. Operation region of boost-converter-inverter EV traction drive.

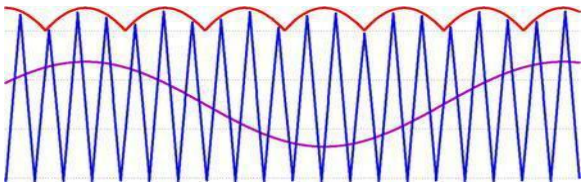


Figure 17. Variable carrier SPWM control in buck mode.

In SVPWAM control of boost mode, dc-link voltage varies with the output voltage, in which the modulation index is always kept maximum. So, when dc-link voltage is above the battery voltage, dc-link voltage level varies with the output voltage. The voltage utilization increased and the total power stress on the devices has been reduced.

C. Variable DC-Link SPWM Control at High Frequency

When the output needs to operate at a relative high frequency, like between 120 Hz and 1 kHz, it is challenging to obtain a 6ω dc-link voltage without increasing the switching frequency of a boost converter. Because the controller does not have enough bandwidth.

Furthermore, increasing boost converter switching frequency would cause a substantial increase of the total switching loss,

because it takes up more than 75% of the total switching loss. The reason is because it switches at a complete current region. Also a normal SPWM can not be used in this range because the capacitor is designed to be small that it can not hold a constant dc link voltage. Therefore, the optimum option is to control the dc link voltage to be 6ω and do a variable dc link SPWM modulation, as explained in Fig. 17.

In this variable dc-link SPWM control, in order to get bet-ter utilization of the dc-link voltage, an integer times between the dc-link fundamental frequency and output frequency is preferred. When the output frequency is in [60 Hz, 120 Hz], a

6ω dc link is chosen; when the frequency is in [120 Hz, 240 Hz], a 3ω dc link is chosen; when the frequency is in [240 Hz, 360 Hz], a 2ω dc link is chosen

D. Experiment Results

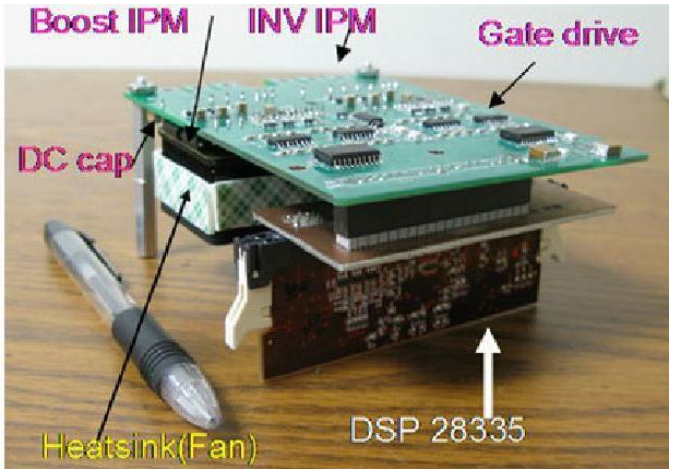


Figure 18. Hardware picture of the 1-kW SVPWAM boost converter inverter.

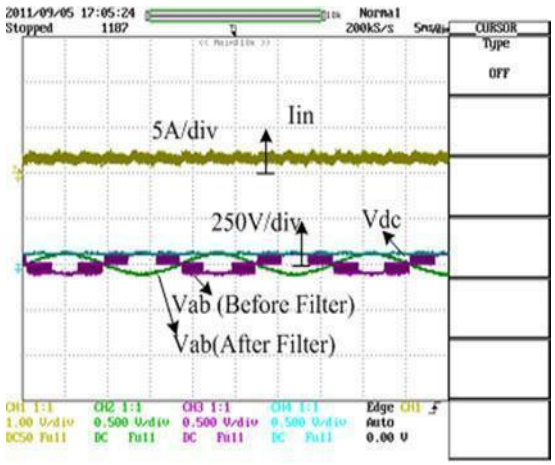


Figure 19. Output voltage and input current at *V*in = 20 V, *V*d c av g = 60 V, *V*lrm s = 46 V, *Po* = 40 W, *fo* = 60 Hz, *f*s w = 20 kHz. order to demonstrate their merits in reducing power loss

and reducing the size compared to traditional methods. The picture of the hardware is shown in Fig. 18. It includes a DSP board, a gate drive board, a boost converter, a three-phase inverter, heat sink, and a fan cooling system. The dimension is 11 cm × 8 cm × 5 cm, and the total weight is 1.5 lb.

The parameters used in the test are rated power: 1 kW; PV voltage: 100–200 V; rated line voltage rms: 230 V; dc-link voltage peak: 324 V; switching frequency: 20 kHz; output frequency: 60 Hz–1 kHz

2) SVPWAM Control at 60 Hz: Figs. 19–20 show the out-put and input voltage, current waveform when PV input voltage increases from 20 to 100 V, while keeping the boost ratio con-stant. In this case, the output voltage increases linearly with input voltage increase. The output power increases in proportion to square of the input voltage.

Fig. 21 shows the efficiency test results by YOKOGAWA WT1600 series power meter when the input voltage increases from 100 to 200 V, while keeping the output power constant at 1 kW. The output line-to-line voltage rms keeps at 230 V, and the dc-link voltage is a 6ω varied waveform with 325 V peak value. In the data record on the power meter, *U*m n6 , and *U*m n1 represent the phase line voltages; *I*rm s6 , *I*rm s4*I*rm s1 represent ten times of phase currents, because ten circles of wires have been wound on the current transducer core of

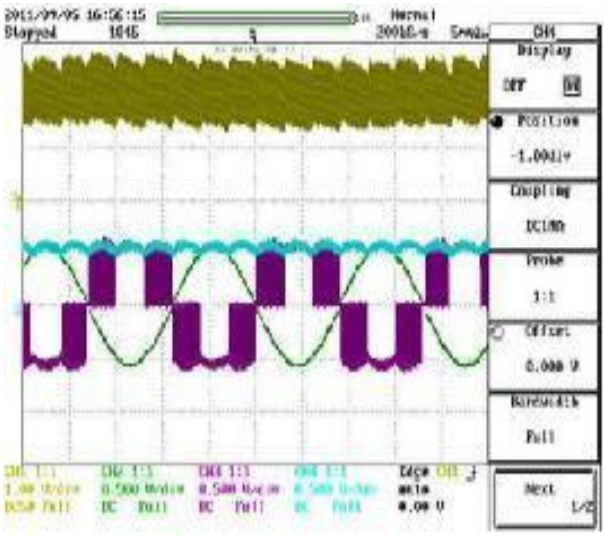
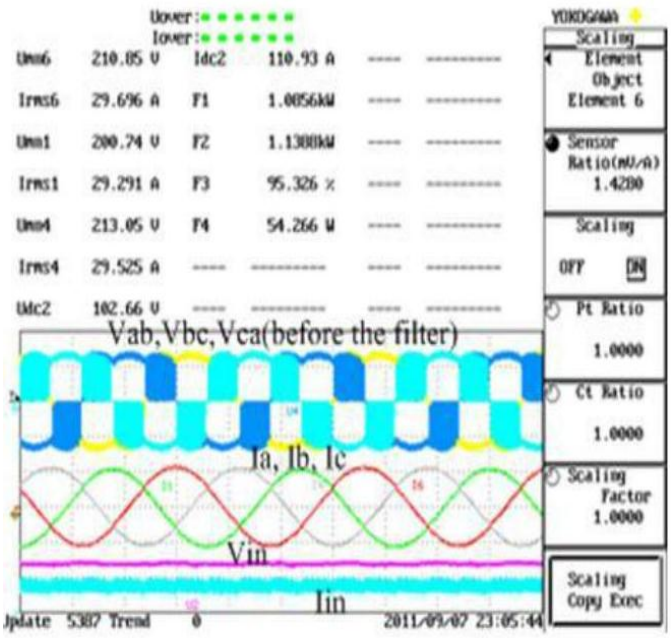
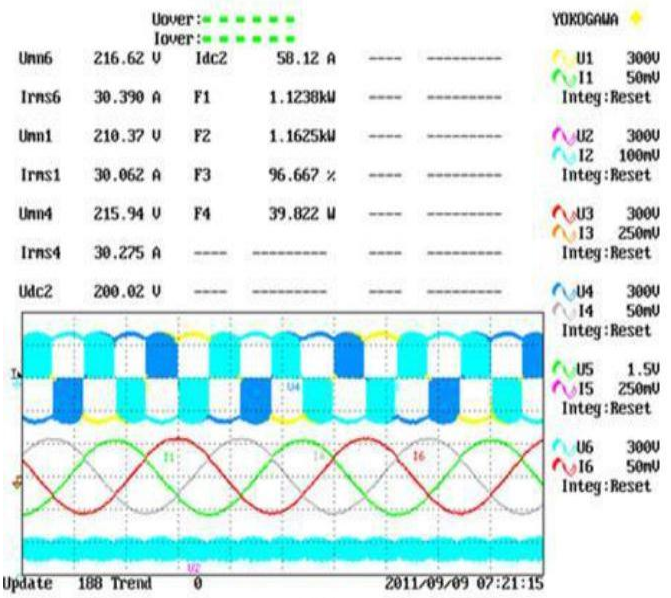


Figure 20. Output voltage and input current at *V*in = 100 V, *V*d c av g = 300 V, *V*lrm s = 230 V, *Po* = 1 kW, *fo* = 60 Hz, *f*s w = 20 kHz.

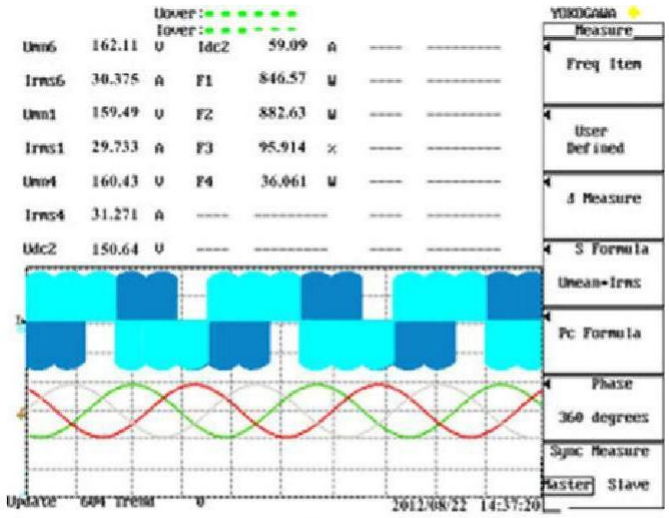


(a)

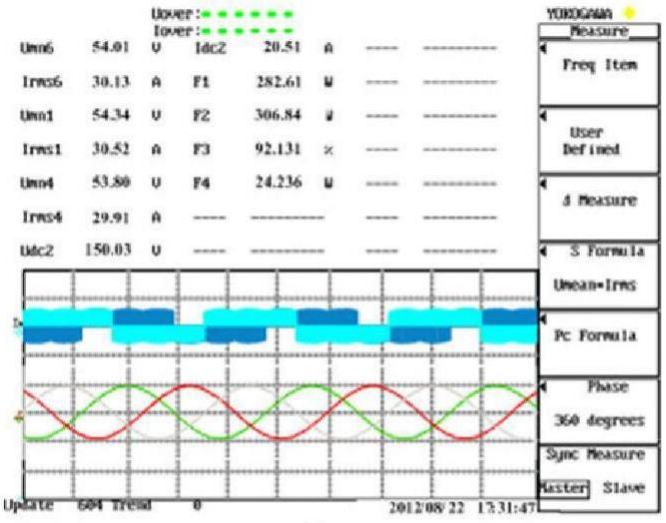


(b)

Figure 21. Results of efficiency test at constant full power rating 1 kW but different input voltage by YOKOGAWA WT1600 series power meter. Wave-forms from the top to bottom: output line-to-line voltage before *LC* filter, output current, input voltage, input current. The numbers displayed on the screen repre-sent: *U*m n 6 , *U*m n 1 , *U* m n 4 : RMS value of output line-to-line voltage before *LC* filter, like the first waveform shows; *I*r m s 6 , *I*r m s 1 , *I*r m s 4 : ten times of output line current; *U*d c 2 : input voltage; *I*d c 2 : 10 times of input current; F1: output power; F2: input power; F3: efficiency calculated from F1/F2; F4: total power loss: (a) *V*in = 150 V, *V*d c av g = 300 V, *V*lrm s = 230 V, *Po* = 1 kW, *fo* = 60 Hz, *f*s w = 20 kHz; (b) *V*in = 200 V, *V*d c av g = 300 V, *V*lrm s = 230 V, *Po* = 1 kW, *fo* = 60 Hz, *f*s w = 20 kHz.



(a)



(b)

Figure 22. Results of efficiency test at constant torque region by YOKOGAWA WT1600 series power meter. Waveforms from the top to bottom: output line-to-line voltage before *LC* filter, output current. The input voltage keeps at 200 V constant; the dc-link voltage keeps at 300 V 6ω voltage; the output voltage changes from 54 to 162 V, thus the power also changes from 280 to 850 W proportionally. When power is equal to 1 kW, the voltage reaches at nominal value 230 V. (a) *V*in = 200 V, *V*d c av g = 300 V, *V*lrm s = 162 V, *Po* = 850 W, *fo* = 60 Hz. (b) *V*in = 200 V, *V*d c av g = 300 V, *V*lrm s = 54 V, *Po* = 280 W, *fo* = 60 Hz.

the power meter. *U*dc2 is input dc voltage and *I*dc2 is ten times of average input dc current. F1 and F2 are the measured out-put and input power, respectively. F3 is the efficiency that is calculated using F1/F2. F4 is the overall power loss. Fig. 22 shows the efficiency test results when the power increases in proportional to output voltage below the maximum power while keeping the input voltage and dc-link voltage constant, which is corresponding to the constant torque region in Fig.

16. The input voltage keeps at 300 V 6ω voltage; the output voltage changes from 54 to 162 V; thus, the power also changes from 280 to 850 W proportionally. When power is equal to 1 kW, the volt-age reaches at nominal value 230 V; this waveform is shown in Fig. 21(b).

3) Output Three-Phase Voltage at 1 kHz: When the output frequency increases to 1 kHz, the measured voltage and current waveforms and efficiency are shown in Fig. 23 at input voltage

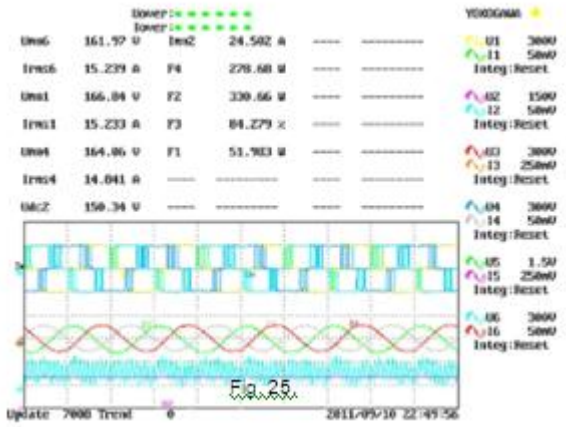


Figure 23. The efficiency test at *V*in = 150 V at *fo* = 1 kHz: from top to bottom:output line voltage, output current, and input current

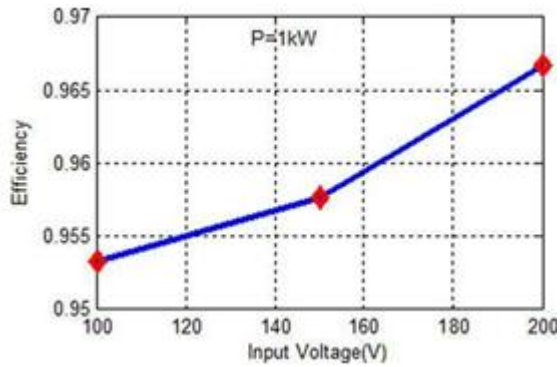


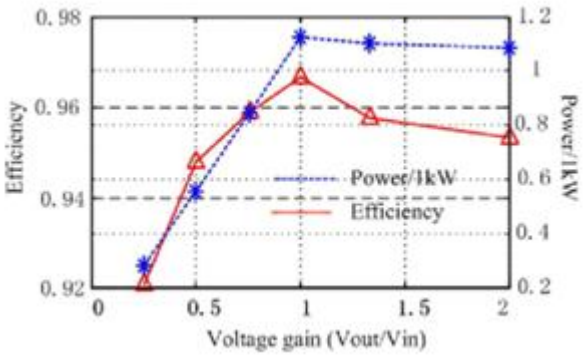
Figure 24. Measured overall efficiency when input voltage changes from100 to 200 V at 1-kW power rating Corresponding to Fig. 23 (*fo* = 60 Hz, *f*s w = 20 kHz, *V*d c p e a k = 325 V, *V* ol -lrm s = 230 V).

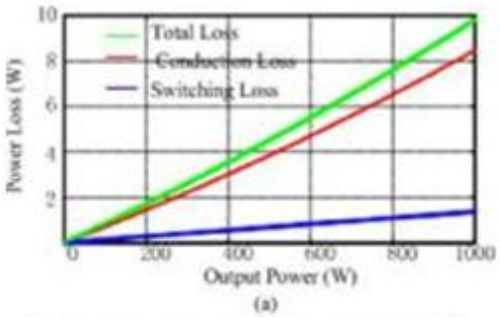
150 V. The efficiency is around 84% for both cases, lower than 60 Hz case.

E. Overall Efficiency and Power Loss Comparison Between SVPWAM and SPWM

Fig. 24 shows the measured efficiency when the pv input voltage increases from 100 to 200 V, all at 1-kW power rating. The over-all efficiency increases as the input voltage increases, because the efficiency of a boost converter increases when the input volt-age increases. The maximum efficiency at 1 kW reaches 97.7% at input voltage 200 V. Fig. 25 shows the joined results of the constant torque region and constant power region in Fig. 16. It can be seen that the maximum efficiency at constant torque region happens at its maximum output voltage where the volt-age gain is equal to 1, and the maximum efficiency at constant power region power happens at its minimum voltage gain point, which is also equal to 1. At constant power region, the efficiency decreases as the voltage increases while keeping the power constant.

Fig. 26(a) and (b) shows the power loss estimation (from the loss model mentioned before) of the inverter when the power Efficiency versus voltage gain results corresponding to Fig. 19. increases from 0 to full rating under two methods. Since the research target is only inverter, the test condition is based on varying the output power by changing output voltage from 0 to 230 V. It is observed that in the SVPWAM method, conduction loss accounts for 80% of the total power loss, but in the SPWM method, switching loss is higher than conduction loss. The switching loss is reduced from 10 to 1.4 W from SPWM to SVPWAM. An estimated 89% switching loss reduction has been achieved.





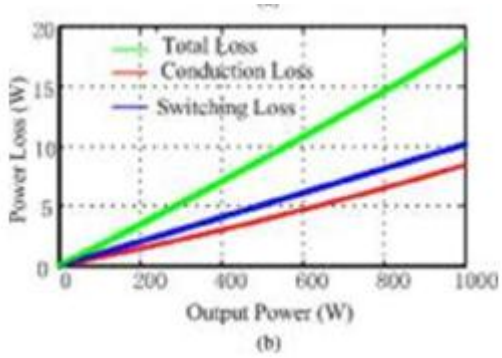


Figure 26. Comparison between inverter power losses in the condition that dc-link voltage changes from 0 to full rating at 300 V: (a) SVPWAM, (b) SPWM.

CONCLUSION

He PV SVPWAM control method preserves the following ad-vantages compared to traditional SPWM and SVPWM method.

1) The switching power loss is reduced by 89% in VSI and 65% in CSI, compared with the conventional SPWM inverter system.

2) The power density is increased by a factor of 2 because of reduced dc capacitor (from 40 to 6 μF) and small heat sink is needed.

3) The cost is reduced by 30% because of reduced passives, heat sink, and semiconductor stress.

High-efficiency, high-power density, high-temperature, and low-cost 1-kW inverter engine drive system has been developed and tested. The effectiveness of the proposed method in reduc-tion of power losses has been validated by the experimental results that were obtained from the laboratory scale prototype

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