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The Study of Electrophysical Characteristics of SOI MOSFETs in the Temperature Range from -60 to 250 °C

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Abstract

The results of research, which aimed at developing high-temperature SOI MOSFETs, are presented. The possibility of stable MOSFETs work at the temperatures above 125°C was investigated. The TCAD simulation of the states of fully and partially depletion in the pockets of MOS transistors is carried out. According to research results and simulation, the parameters of the MOSFETs were changed for increasing its reliability at the high temperatures.

Keywords: High-temperature electronics, silicon on insulator, leakage currents, MOSFET, threshold voltage, saturation current

INTRODUCTION

The high temperature electronics is a class of electronics which includes electronic components designed for stable work in the temperature range from -60 to 225°C (Fig.1)[1,2].

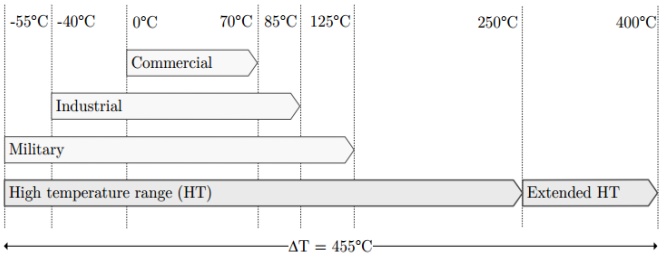


Figure 1. Operating temperature ranges according to their specific application.

For the development high temperature components structures based on Silicon On Insulator (SOI), silicon carbide (SiC) or gallium nitride (GaN) are suitable [1, 3, 4]. At the same time SOI-based electronic components are cheaper than other, and this technology is verified in the production of radiation-resistant integrated circuits [4]. Due to low cost and high technological efficiency, the element base based on SOI is relevant in the applications of aviation, automotive, oil and gas, space and nuclear industries [1, 4, 5].

For the research and development of high-temperature transistors, the radiation-resistant electronic components on SOI-structures from KNI180 (PJSC «Mikron») technology was chosen. The choice of this transistors for high-temperature studies is due to the research of MOSFETs carried out by Honeywell [6], XFAB [7] and IBM [8].

Peculiarities of SOI MOSFETs

Consider the cross section of the metal-oxide-semiconductor-oxide-semiconductor structure (Fig. 2).

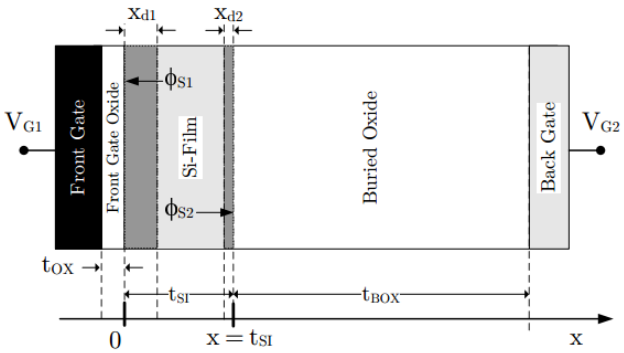
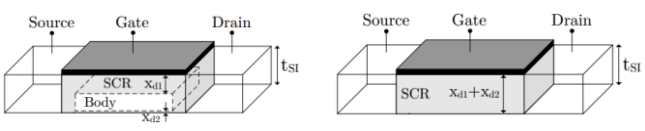


Figure 2. Metal-Oxide-Semiconductor-Oxide-Semiconductor structure.

In the figure 2, the zero of the *Ox* axis coincides with the Si-SiO_2 interface near the front gate, and the positive direction of the *Ox* axis is perpendicular to the layers of the structure. The values of x_{d1} and x_{d2} denote the thicknesses of space-charge regions, such regions in the silicon layer, in which there are no free charge carriers. The surface potentials are denoted by ϕ_{S1} ($x = 0$) and ϕ_{S2} ($x = t_{SI}$), and V_{G1}, V_{G2} are the voltages which applied to the front and back gates.

Usually, two basic states of depletion by charge carriers of SOI MOSFETs are distinguished: partially depleted (Fig. 3a) and fully depleted (Fig. 3b). According to the notations from figure 2, the case of partial depletion characterizes the inequality $(x_{d1} + x_{d2}) < t_{SI}$, and the case of full depletion characterizes the inequality $(x_{d1} + x_{d2}) \geq t_{SI}$. In addition, in the case of partial depletion in silicon region between drain and source, there is an electrically neutral region called the body.



a b

Figure 3. a – partially depleted transistor; b – fully depleted transistor.

The switching between the partial and full depletion states occurs depending on voltages on the gate V_{G1} and V_{G2}, drain-source voltage V_{DS} and temperature. For high temperature MOSFETs maintaining the full depletion state in wide temperature range is actual. In contrast to the state of partial depletion, in the full depletion state there are next features:

- lowering the built-in potential of p-n junctions, which makes it possible to compensate for the effect of a floating substrate, manifested as the temperature rises [9];
- MOSFET's threshold voltage is not depend on temperature [9];
- minimal leakage current at high temperatures due to body exclusion [9];
- reduction of the effects of floating voltage effects, including the kink effect and parasitic bipolar transistor effect [9].

Since the depletion region thicknesses depends on silicon impurity concentration, the problem of development high temperature SOI MOSFETs solves via studying of various dispersions of doping impurities in the space between drain and source.

The study of MOSFET's work at high temperatures

For study double-dimention TCAD model of NMOS and PMOS transistors are chosen. This transistor are part of radiation-resistant technology KNI180 by PJSC «Mikron». The main features of this transistors there are below:

- minimal transistor's channel length: 0,5 μm;
- transistor's supply voltage: 5 V;
- buried oxide (BOX) thickness: 0,146 μm;
- top silicon layer thickness: 0,088 μm;
- gate layer SiO_2 thickness: 100 Å;

From the experiment we obtained the output current-voltage characteristics for different temperatures from -60 to 250ºC and temperature dependencies for threshold voltage, saturation current, leakage current. Temperature dependencies are correlated with results of measurement of MOSFETs on chip with A- and H-gate at the high temperatures.

Temperature dependencies of the saturation currents for NMOS and PMOS transistors are shown at Fig. 4a and 4b and allows to calculate changes of current by 1ºC temperature changes (Table 1). These values of changes of current are valid also for on-chip MOSFETs with A-type gate. At the same time, MOSFETs with H-type gate have saturation currents 1. 2×10^{-4} A larger than saturation currents of double-dimension model.

Temperature dependencies of leakage currents are shown in logarithmic scale at Fig. 5. As for NMOS transistor (Fig. 5a) and PMOS transistor (Fig 5b) leakage current is maximal at 250ºC and equal $2{,}14 \times 10^{-9}$ A for NMOS model and $3{,}56 \times 10^{-10}$ A for PMOS model. These values coincide in value order with the same values for on-chip MOSFETs.

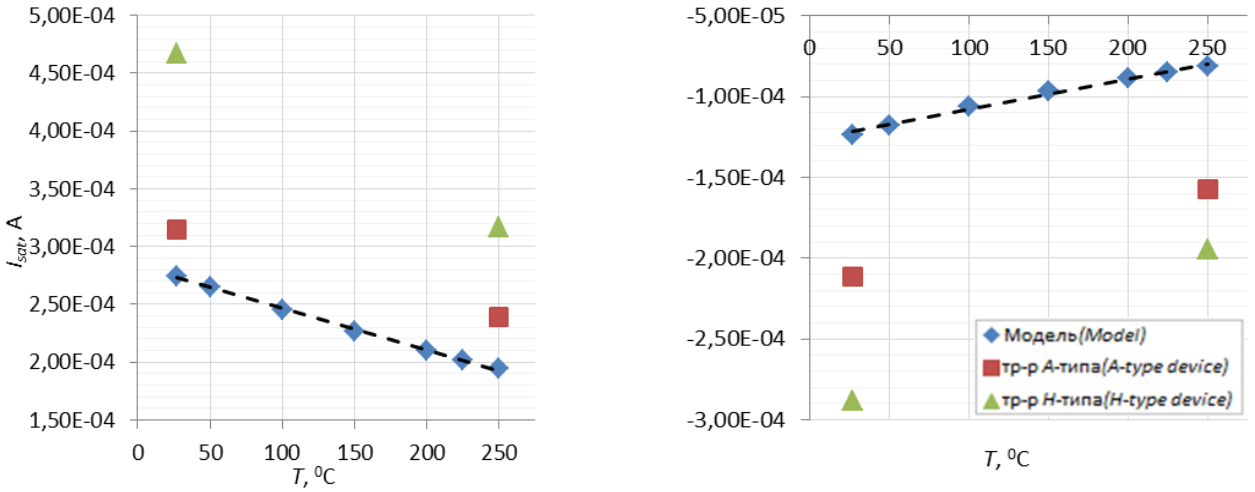


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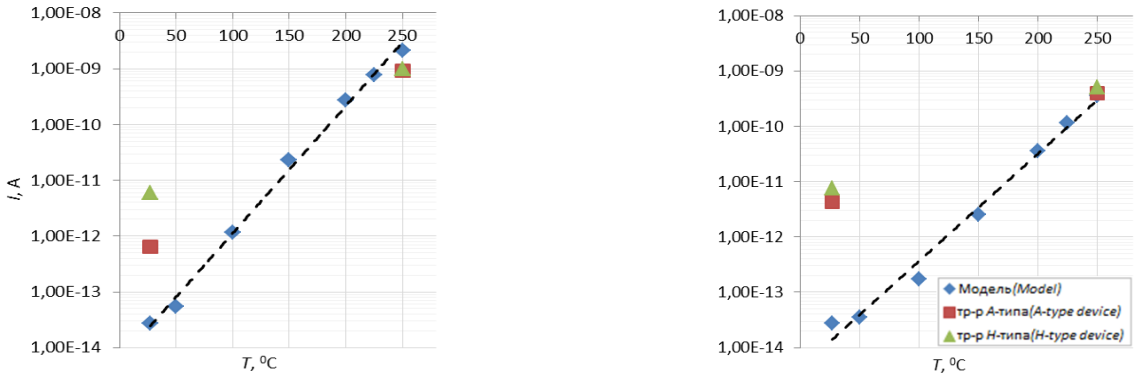
Figure 4. Temperature dependencies of saturation currents I_{sat} for: a – NMOS transistor; b – PMOS-transistor.



a b

Figure 5. Temperature dependencies of leakage currents *I* for: a – NMOS transistor; b – PMOS-transistor.

Table 1. Changes of threshold voltage and saturation current by 1ºC temperature change

Transistor	Threshold voltage, $V_{th}/T \times 10^{-3}$ V/ºC	Saturation current, $I_{sat}/T \times 10^{-7}$ A/ºC
NMOS	1,67	3,6
PMOS	1,65	1,9

As for TCAD model, and for on-chip MOSFETs the maximal leakage currents 5-6 decades times smaller than minimal saturation currents (0,5 .. 2 × 10^{-4} A) at the temperature of 250ºC. Consequently, leakage currents, that smaller than saturation currents, allows to conclude that studied SOI MOSFETs retain its amplifying properties at high temperatures.

Optimization of the SOI MOSFET technology

For study of MOSFET's depletion states double-dimensional TCAD model is used. In this first model the dose of implanted in NMOS well ions of BF_2, is changed from 2,6 × 10^{12} cm^{-2} to 5 × 10^{12} cm^{-2}. At the same time similar parameter for PMOS transistor was left former (1,5 × 10^{12} cm^{-2}). The dose is changed for decrease the value of NMOS threshold voltage change by 1ºC temperature change. In tables 2 and 3 threshold voltages values before and after dose change are shown.

Table 2. Threshold voltage values before change of impurity concentration

Temperature, ºC	NMOS	PMOS
	Vth, V	Vth, V
0	0,949	-1,137
27	0,911	-1,100
50	0,878	-1,068
100	0,803	-0,996
150	0,725	-0,919
200	0,641	-0,837
225	0,596	-0,794
250	0,550	-0,750

Table 3. Threshold voltage values after change of impurity concentration.

Temperature, ºC	NMOS	PMOS
	Vth, V	Vth, V
0	1,273	-1,137
27	1,229	-1,100
50	1,191	-1,068
100	1,106	-0,996
150	1,016	-0,919
200	0,920	-0,837
225	0,870	-0,794
250	0,818	-0,750

Thus, in comparison with initial model of MOSFETs, changed model demonstrates slow falling of threshold voltage when temperature rises. Moreover, comparison shows that changed model has increased switching temperature from full depletion state to partial depletion state. This result shows the increase of MOSFET's reliability at high temperatures.

CONCLUSION

The study of SOI MOSFETs at the temperatures from -60 to 250ºC is carried out. As a result, the possibility to develop the high temperature SOI MOSFETs was confirmed. The SOI MOSFETs with the 0.5 µm minimal length and with supply voltage of 5 V were investigated. In the studies, the temperature dependencies of saturation current, leakage current and threshold voltage was obtained.

Analysis of temperature dependencies has shown the need to reduce the NMOS transistor's threshold voltage changing at the investigated temperature range. It was also found necessary to increase the value of the switching temperature from full depletion state to partial depletion. To do this, the doping dose of ions for NMOS transistor well were changed, and that resulting in a reduction of the change the threshold voltage at the operating temperature range and an increase in the switching temperature.

As a result of studies and changes in technological route of SOI MOSFETs with minimal length 0,5 μm and supply voltage of 5 V SOI MOSFETs reliable up to 225ºC were obtained.

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