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A Low Power Hamming Code Based Controller with Splitting Logic Built-in Self Test Scheme

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Abstract

Network on Chips (NOC) system consists of memory chips, which improve the scalability of System on Chips (SOC) and power efficiency of complex SOCs when compared to other designs with synchronous & asynchronous clock domains.

In this paper, we focused on fault diagnosis & removal of errors in a Memory Core System with a Hamming processor based data handling system utilizing less testing power. For this, modified Built-in self-Test (BIST) and Automatic Test pattern Generator (ATPG) are used. Here, by using clock splitting logic in novel Linear Feedback Shift Register (LFSR), we are reducing the power by decreasing the switching activity. Testing embedded Memory chips is a complex and costly affair in recent times, as Fault finding and correction is a delicate task without losing data. Parity bit generation to locate the error by Hamming code Encoder is the first step of this process. Automatically fault recovery is done using Hamming Data decoder. In this, Result part shows how best our proposed model is, when compared to existing models. 99% faults are identified and corrected, so fault coverage ratio is high. 30% less power is consumed when compared to existing counterpart. Xilinx 14.2 IDE and CAD tools are used to get experimental results.

Keywords: Built-in self-Test (BIST), Clock Splitting logic, Hamming Data Encoder, Hamming Data decoder, LFSR, ATGP.

INTRODUCTION

During Memory IC manufacturing and writing or reading of Memory, many types of errors (or) faults will occur. It is very difficult to diagnose all the errors. There are many methods available to find these errors; but they are not perfect in identifying all types of errors.

Most common types of errors are generally treated using ECC (Error Correcting Codes) of memory. This is an integrated system in memory storage itself.

Repeatable (or) hard errors occur when a piece of hardware is broken and will consistently produce in correct words. Struck at "0" and struck at "1" faults are also called as "Struck at faults" where 0 or 1 got struck in it.

Bridging Faults in electronic circuits means two signals are connected when they are not supposed to be connected.In MOS memories (or) in VLSI designs, mostly dominant AND (or) dominant OR bridging model is used.

Generally, delay faults occur in multifunction chips. If the first function is delayed, it will be added to the next function – causing increase in total delay.

Demand for testing (DFT) is a recently developed field. Technology enhancement leads to increment in IC production, whereas cost of IC production comes down; but testing of ICs is costly and complex.

There are two testing schemes, 'Built-in Test scheme' and 'Joint Test action Scheme'. In both the schemes, Fault coverage is high.

No memory system is perfect. These errors lead to system crash (or) alter the output. Soft errors means one bit change in the memory, may be due to unexpected / unwanted changes. It could be due to noise that stored in place of valid data. In such a case, one (or) more bits get altered to other values than what they are supposed to be; possibly changing an instruction (or) data value in a program.

An open circuit fault may occur due to short-circuit power (or) earthing fault.

Transition fault may occur due to fault of a cell that fails to undergo while 0 to 1 transition (or) 1 to 0 transitions.

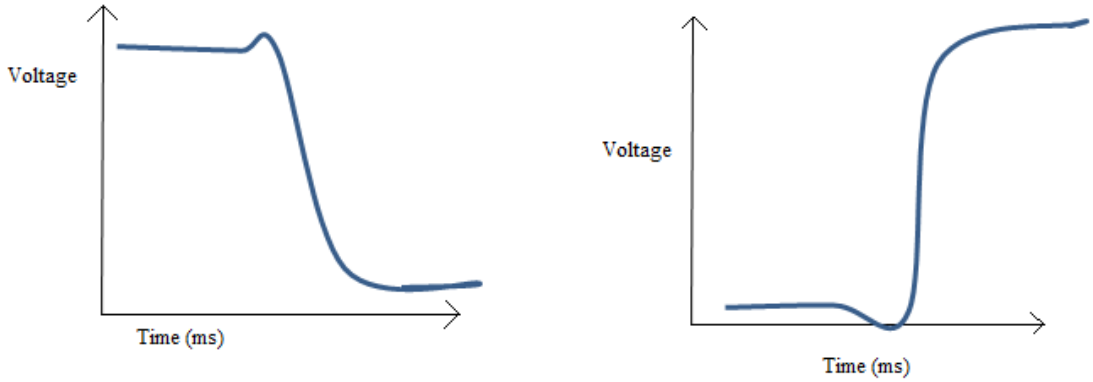

Figure 1. Transition state of Data Curves

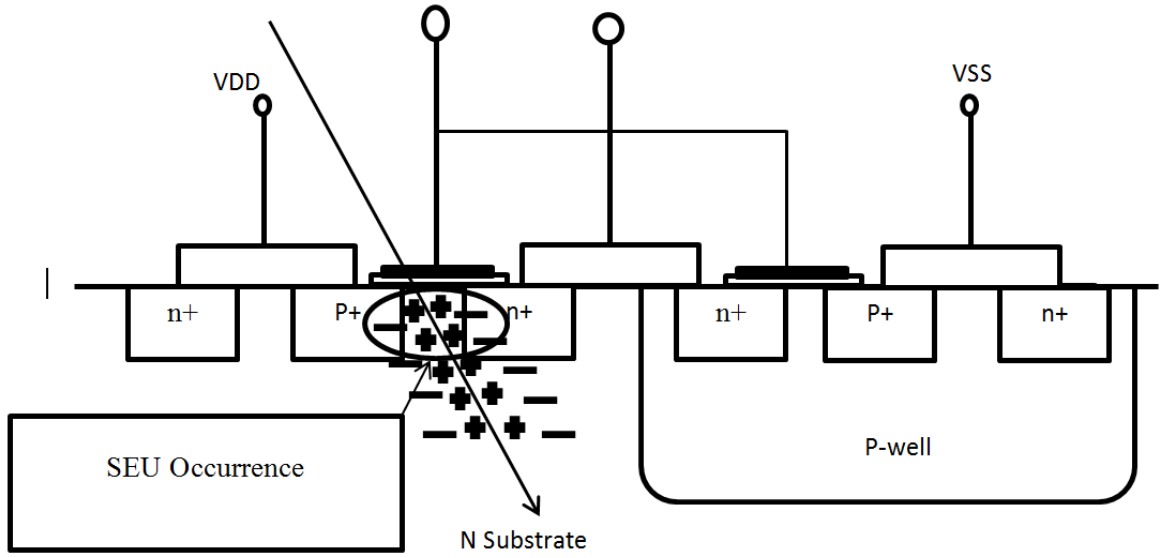

Figure 2. SEU error representation in Memory Cell

Figure 1 shows data change due to ionized charged particles agitation with memory. The affecting area causes the data loss in Memory chips.

Transient (or) Soft error is the error which doesn't destruct system's hardware. But, it will destroy the data (or) instruction in a program. The two types of soft errors are equally cause damage to the system. When the particle hits the chip, the bit value changes, this soft error is called 'chip-level soft error'. Sometimes, computer interprets noise bit as data bit, and the noise bit causes problem at the later stage. This type of error is called as 'System-Level Soft error'. This error can be corrected by re-writing the data in place of erroneous data and rebooting. These are also called as '**Single Event Upset'** faults.

Figure 2 corresponds to the Single Event Upset Error (SEUE). The polarity of the positively charged particles converted into negatively charged particles as they travel through the semi conductor element. The memory core stored values will change due to above Single Event Upset Error.

Kono developed a Josphson-CMOS hybrid memory aimed to minimize the power of 64-kb CMOS Static RAM using 3 approaches: miniaturization of the memory cell, the improvement of the data driver and binary tree decoder. Simulation Results were showing that 54% write operation and 8% Read operation power reduced when compared to previous Models. Josephson-CMOS hybrid memory is a fully functional large-scale memory for high performance computing.

Ebrahim proposed a 6T-SRAM with quasi schotkey-barrier ultrathin body and ultrathin buried oxide (UTBB) silicon-on-insulator (SOI) device. It is power efficient as 18% leakage power at VDD = 1V minimized when compared to conventional symmetric UTBB SOI device. It not only reduces the drain-induced barrier lowering (DIBL) but also improves RSNM (read static noise margin) by 54%, improves write Margin (MW) by 6.6% i.e., the asymmetric nature of QSB UTBB SOI minimizes the read-write conflict of 6T-SRAM cell.

Daeseok investigated & demonstrated about the energy storage & memory in conducting bridge RAM (CB RAM) cell. In memory mode, Ag bulk diffusion formed in GeS_2, while for energy storage, Ag bulk diffusion integrated & fabricated with the same volume, same fabrication process. It is used in autonomous and low power applications.

Conventional Methods:

In this, linear feedback shift register is shown that uses 4 flip flops to store the 4 bit data. Common clock is given to each flip flop operation and each stage of output of d-flip flop XOR-ed with previous state of flip flop.

In conventional BSIT scheme, power consumed for testing and area occupation for testing are high. Power consumption for testing of memory core is almost double to that of memory usage.

Use of Automatic Test Pattern Generator (ATPG) is to release random data, which is stored in memory core. This data will be compared with input data.

Figure 4 shows the testing of Memory data using conventional BIST scheme. Here ATPG (Automatic Test Pattern Generator) generates random data and transfers into Memory under Test. Controller generates control signals. By using Bi directional data flow, information (bits) is stored in Memory under test and recovered. Comparator compares the stored values with Random data. When faults are detected, automatically fault alarm cautions the controller circuit to stop the process. After some time, again the process starts. However, this existing method is oblivion because it is not revealing the Fault area and fault type and recovery.

This paper is organized as follows. In Section 1, introduction relates to different types of errors and briefly discuss about the conventional methods. Section 2 describes the recent works related to proposed model. Section 3 gives the problem definition and methodology. Section 4 gives the detailed explanation and structure of the proposed model and Section 5 simulation results compare the proposed model with other existing models in terms of dynamic power, total average power and fault coverage and correction; and the superiority of our model is shown. Finally the paper concludes in Section 6.

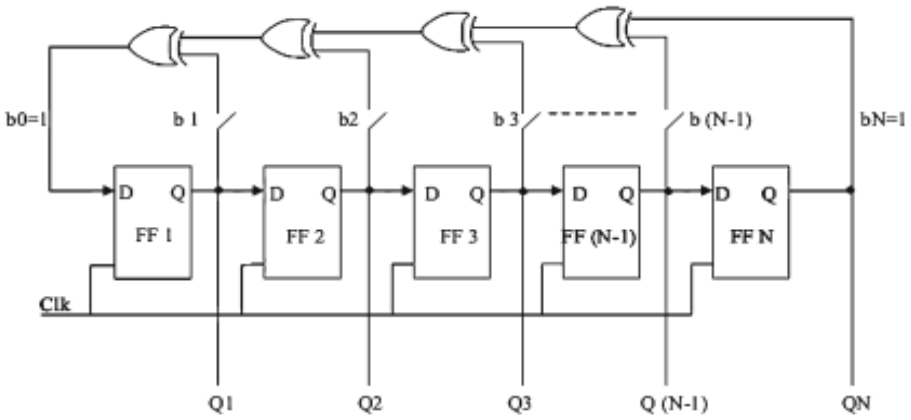

Figure 3. Conventional Linear Feedback Shift Register (LFSR)

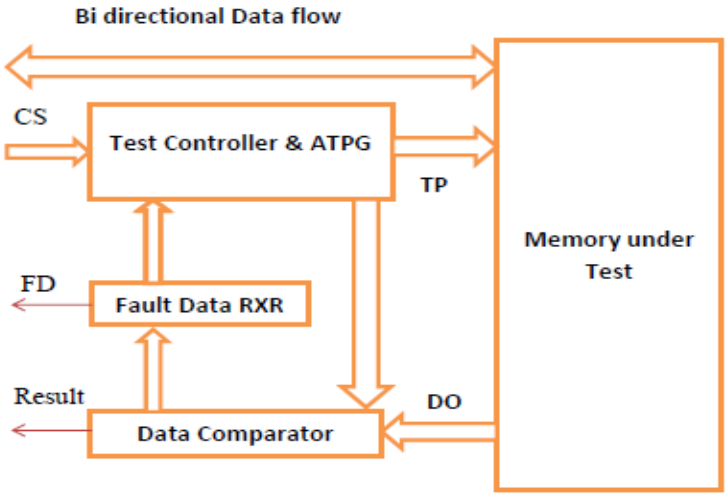

Figure 4. Conventional Block Diagram of Memory BIST scheme.

LITERATURE REVIEW

1. Zijian [1] proposed a coding method of SOC, which is power efficient method which condenses test data volume. Preliminarily testing & verification for on-chip is done by 2D reordering scheme. Later, don't care bits are replaced by 4m filling scheme and is encoded by ASRL coding scheme. When compared to others, this coding method has great compression ratio and low testing power and low testing time.
2. Rehman [2] developed a BIST scheme, which is scalable to any FGPA array size and a set of automated tools is developed to generate these files required to produce the sequence of test configuration bit streams. In this, fully and partially configured FPGA tests are performed. Under comparison of these stuck at faults, 100% detected and 43-57% test time saved for partial reconfiguration scheme of FPGA.
3. Awad [3] reduced the switching activity in the address bus i.e., testing power reduced in MBIST (Memory Built-in Self Test) when testing SRAM devices. He designed & programmed using VHDL coding and then five address generators were simulated using Xilinx ISE tools and compared with other models.
4. Chun-Lung [4] designed BIST (Built-in Self Test) with SRAM based FPGAS, which is capable of testing interconnects, LUTs in CLBs. This gives 100% fault identification and automatic fault correction without area overhead.
5. Liu [6] suggested a scan-based testing on SOCs, which is an independent Test Compression Technique. In this, block merging and eighty encoding (BM-80) reduce the test data volume i.e., saving of testing time.
6. Abu-Issa [7] offered a design of BS-LFSR (bit-swapping LFSR), which reduces the scan shift operations by 50% in scan based built in self-test when compared to normal LFSRs. Here 65% and 55% of average and peak power saved without effecting fault coverage and speed.
7. Padmavathy [8] presented two multistage compression methods to minimize the test data volume and simple decoder to decode the huge volume of data.
8. Mukherjee [9] presented a BIST (Built-In self Test) scheme to find permanent faults in embedded ROMs. In this speed and accuracy are high.
9. Hunter [10] extended the integration of diagnostics in a Memory BIST scheme, which minimizes the test time, ease of testing, limited area of operation, Reuse of design. And it can be extended to manufacturing faults throughout manufacturing process.
10. Dubrova [11] created a Logic Built-In Self Test (LBIST) method, which can test the machine to machine (M2M) devices' communication end points. Additional advantage of this is, it protects the random & malicious faults.
11. Wang [12] proposed a dual speed LFSR (DS-LFSR), in which two LFSRs are presented; one is slow LFSR and other one is normal LFSR. This is superior to LFSRs with primitive feedback connection. Here power consumption is lowered as switching activity is reduced. In addition, high transition delay fault coverage is also achieved through DS-LFSR.

PROBLEM DEFINITION & METHODOLOGY

There are many schemes available to find fault identification and recovery. One of the conventional Research schemes is 'unwanted test seed skipping scheme'. But the fault identification ratio is low.

While performing high fault diagnosis, consumption of lesser power is also an important factor. By reducing switching (or) clocking activity, power consumption can be reduced. Here, our New Hamming code based Clock Splitting BIST (HCS-BIST) scheme is very much useful in fault identification & recovery of Single Event Upset (SEU) faults, when compared to other existing schemes. Here, HCS-BIST scheme, not only performs high fault coverage & correction, but also minimizes the overall testing power. Instead of using one clock generator, two clock generators are used. So, clocking & switching activities minimize the power consumption.

MOS Memory devices have been found to be integral part of Electronic circuits and systems. In other words, any system without memory devices is incomplete. Testing of chips is an important aspect for right data transfer. The three important parameters used to characterize Memory devices are Area, Speed and Power. If the speed and number of active devices in the chip increases, power increases.

As switching activity decreases dynamic power reduces. Here, we are reducing the clocking activity by clock splitting logic. Instead of using single clock generator, two clock generators are used to produce the 4-bit word.

While diagnosing the data faults, it is noticed that stuck-at faults and open circuit faults are major in number. The conventional Memory testing schemes are also concentrating on these errors, however, the fault coverage ratio is low. Whereas, with our HCS-BIST scheme, fault location, fault coverage, fault type and fault recovery are significant.

WORK FLOW AND SYSTEM MODEL OF PROPOSED DESIGN.

The HCS-BIST scheme not only identifies the single event upset (SEU) errors, but also corrects them automatically and by using Clock-splitting logic based LFSR, total Testing Power gets reduced.

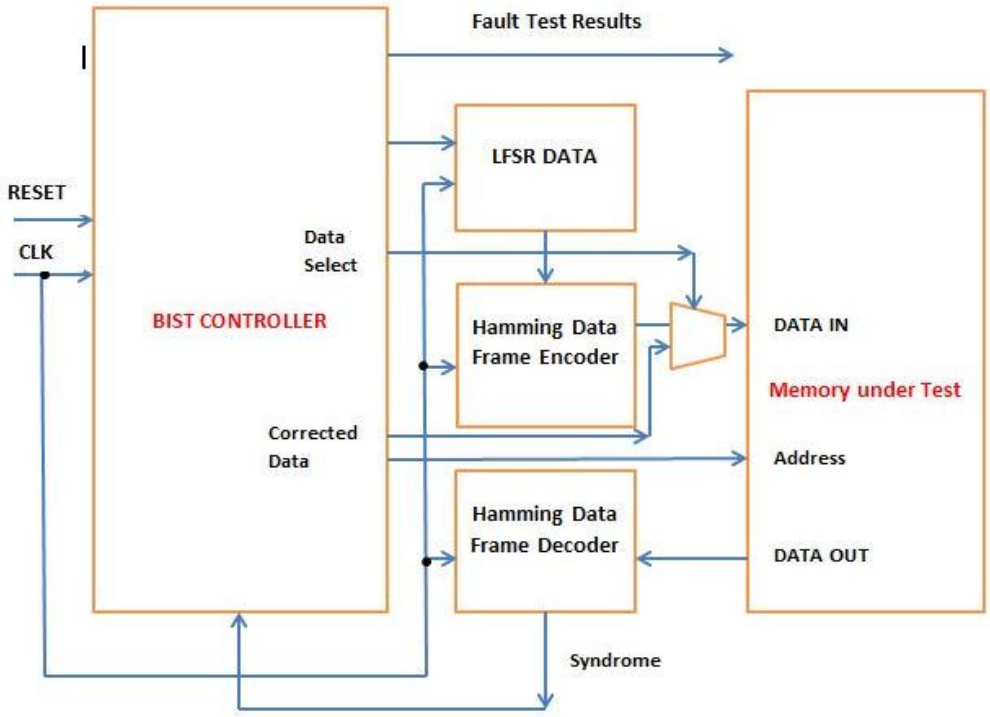

Figure 5. Block Diagram of HCS-BIST System

The above figure represents the hamming code based BIST memory system. In this, the 5 major blocks are: BIST Controller, LFSR Data, Hamming Data frame Encoder, Hamming data Frame Decoder and Memory under Test.

The common clock synchronizes all the activities in the above system, so that all activities can be performed in parallel.

BIST Controller:

It is the main block, which controls all the other blocks. Information is given to LFSR DATA unit. Through Data Select Signal, BIST controller controls the Multiplexer and provides the Hamming code word to Memory under Test. It gets the syndrome value from Hamming decoder for data correction and sends the corrected word into Memory under Test. Fault Test results are sent out for fault analysis.

Clock splitting Logic Based LFSR Model:

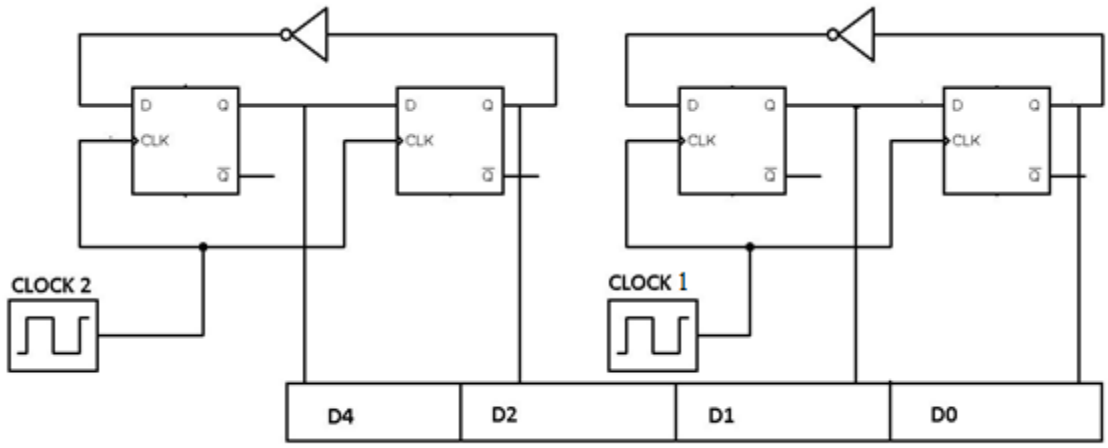

Figure 6. A Low Power LFSR Design with two clock generators.

Figure 6 represents the clock splitting logic based LFSR design. The difference between the conventional LFSR and clock splitting logic is that here, double data bits are shifted instead of single data bits. Our proposed LFSR design works with N-2 logic (means if 2N=8, N=4), i.e., 4 bits of data is generated. The 4 bits are divided into 2, 2 bits. The individual 2, 2 bits are connected to clock generators (Clock 1 and Clock 2). The testing power is reduced to half because clocking activity is reduced to half.

Hamming Data Encoder:

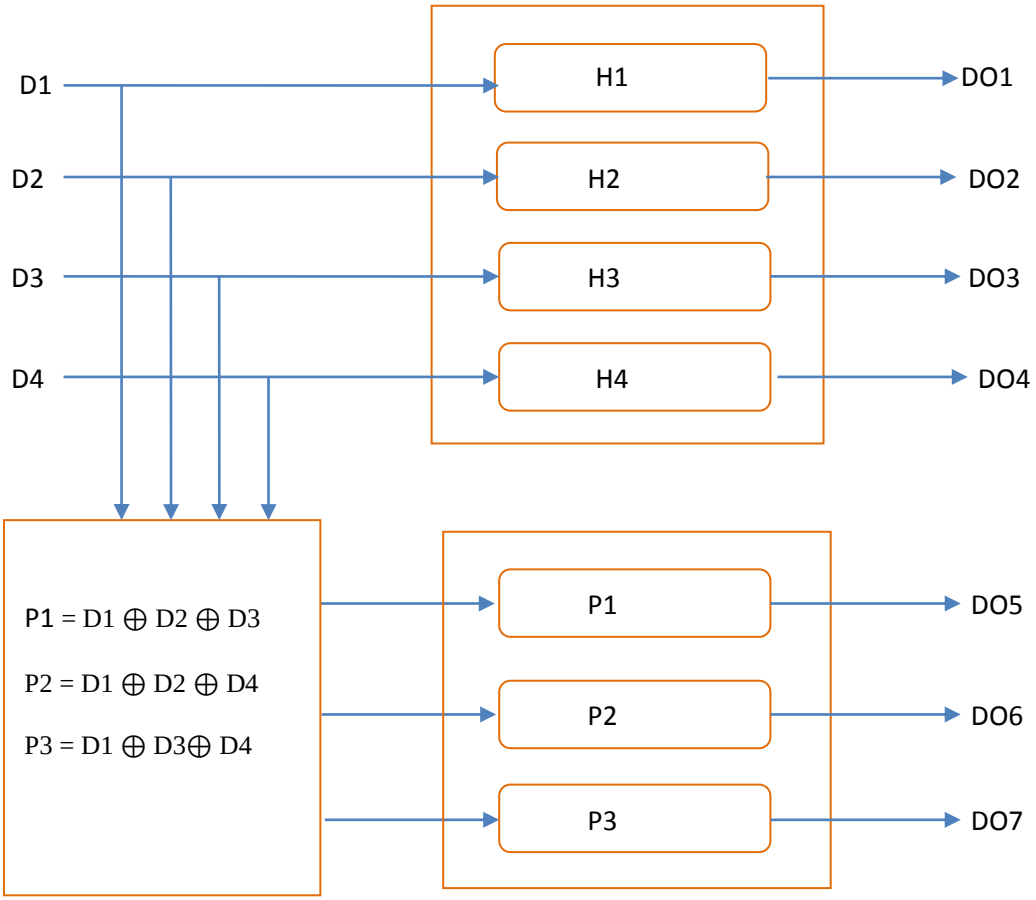

Figure 7. Hamming Data Frame Encoder

Figure 7 desrcibes the activities in hamming data frame encoder. Here, three parity bits are located in 2^0, 2^1 and 2^2 positions. Using the below formula, number of parity bits can be calculated.

$$2^P \geq P+M+1$$

where,
M is number of data bits
P is number of parity bits.

Data bits and parity bits are arranged in the following way.

DO1	DO2	DO3	DO4	DO5	DO6	DO7
D4	D3	D2	P3	D1	P2	P1

Using the random test data of 4-bits, 3 parity bits are calculated by following XOR operations.

P1 = D1 ⊕ D2 ⊕ D3

P2 = D1 ⊕ D2 ⊕ D4

P3 = D1 ⊕ D3 ⊕ D4.

This 7-bit encoded Hamming code is stored in Memory under test through Hamming encoder and this code is analyzed again in hamming code decoder circuit to find the syndrome value. Fault location through syndrome value is generated using the following way.

Hamming Data Decoder

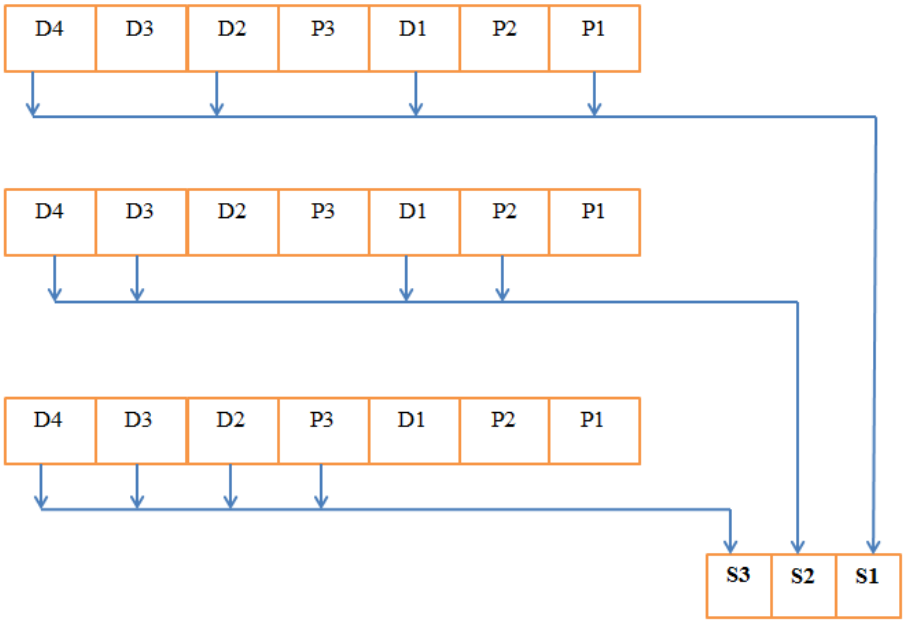

Figure 8. Hamming data decoder Circuit

Using the above hamming decoder circuit, syndrome value is generated

S3 S2 S1

If any of the three parity bits causes error, D1 will show the error. Similarly, if D2 showing error means, P1 and/ or P2 have an error. If P1 and/or P3 have an error means, D3 will be showing the error.

The syndrome value decides the fault bit location. Immediately, BIST controller corrects the bit value by inverting the error contained position. The corrected word is sent to Memory under Test for storage. Using the Result analysis, one must know whether it is a stuck-at fault, single event upset (or) Delay fault.

Memory under Test:

Basic Memory under Test unit in embedded memory has three inputs: Address line, Input data line, and Read/write line. Output data line takes the information from Memory under Test.

Using address line, random data from ATPG (Automatic Test Pattern Generator) is stored in Memory core and output is given to Memory under Test. If there are no faults given, data is given to output. Otherwise, output is forwarded to Response Analyzer, which analyzes the data and gives the fault rate (or) type of error.

In this conventional memory under test, automatic fault correction is not found. But here, Memory under Test is connected to Hamming code encoder through Multiplexer to take Hamming code based word, which includes parity bits for fault identification. And that word is sent to Hamming Decoder as DATA OUT. Hamming Decoder sends the syndrome value to BIST controller to identify the error position in Hamming code. After automatic correction of the word in BIST Controller, the corrected WORD is again sent to storage in Memory Under Test.

RESULT ANALYSIS

The New Memory BIST (HCS-BIST) scheme has been implemented and synthesized by Xilinx 14.2 tool for fault identification and correction. The Simulated Result is shown in Figure 9 with an example. The RTL layout for this scheme with clock splitting logic with Hamming code process is also shown in the Figure 10 for Fault identification and correction. As we know, clock splitting logic helps to reduce the Testing power. Hamming encoder & decoder is used in HCS-BIST scheme for better fault coverage and automatic correction.

Table 1: Power comparison of existing memory BIST schemes with proposed (HCS BIST) scheme

BIST Scheme	Dynamic Power(nW)	Saving %	Total Average Test Power(nW)	Saving %
LFSR	0.222	-	0.402	-
BS-LFSR	0.199	10.36	0.378	5.97
HCS-BIST	0.146	34.23	0.279	30.6

When compared with the existing BIST schemes, our proposed HCS-BIST scheme consumes lesser dynamic power (34% less) and lesser total average Test Power (30% less).

Table 2: Fault Coverage comparison of existing memory BIST schemes with proposed (HCS-BIST) scheme

BIST Scheme	Average Faults Covered (100 Read Operations)	Fault Coverage Ratio
LFSR	80	80%
BS-LFSR	85	85%
HCS-BIST	99	99%

Generally, stuck-at Faults (either stuck-at 1 fault, stuck-at 0 fault or hard errors) are more (nearly 60%) in embedded memory core faults. Leftover 40% faults are others. In this also, major faults are of single event upset errors. Single bit faults may occur due to many reasons. These may be due to glitch, voltage fluctuations, external noise, etc.

When compared to the existing BIST schemes, HCS-BIST scheme is superior in fault coverage and recovery which is 99%. When compared to the existing leading counterpart, it is 14% more.

Table 3: Area Utilization of Proposed Memory BIST Scheme

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	19	768	2%
Number of Slice Flip Flops	7	1536	0%
Number of 4 input LUTs	35	1536	2%
Number of bonded IOBs	3	63	4%
Number of GCLKs	1	8	12%

Table-3 gives clear picture of area utilization of HCS-BIST scheme which is very less. Because of less utilization of Flipflops, Look-up Tables, Input-Output Blocks and GCLs power consumption through them is also less.

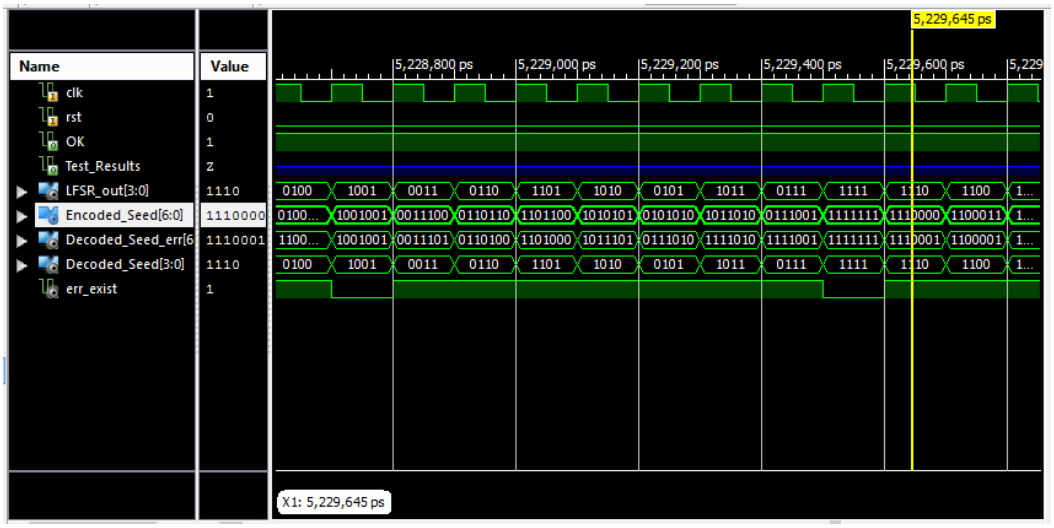

Figure 9. HCS-BIST system simulation Result

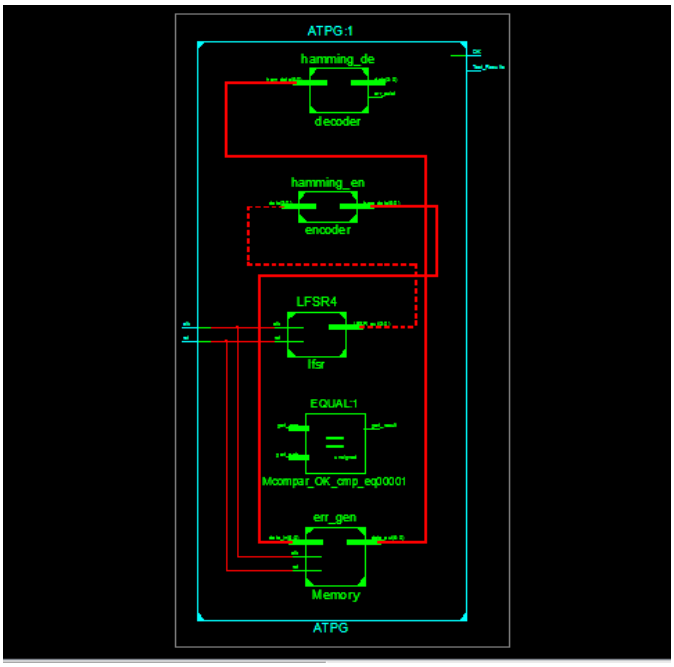

Figure 10. RTL Layout of HCS-BIST Scheme

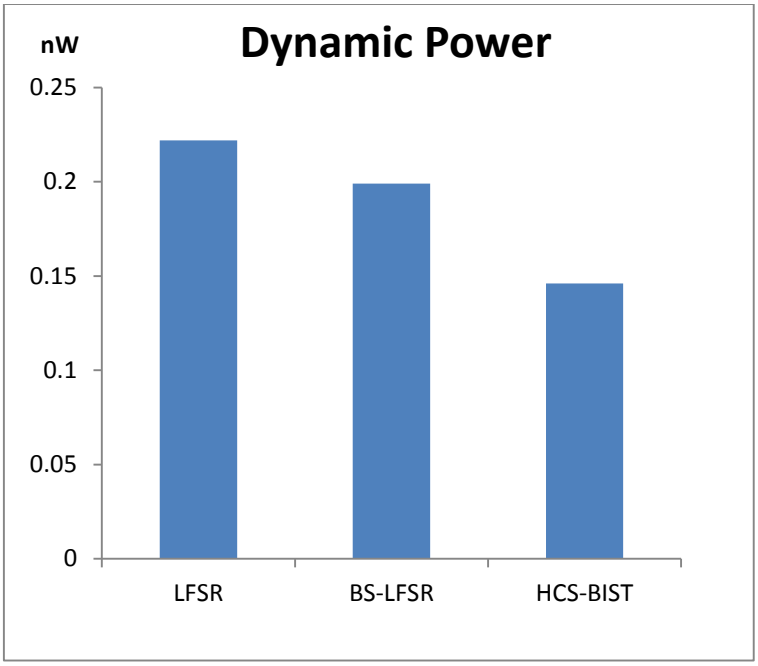

Figure 11. Dynamic Power consumption comparison with different BIST schemes.

When compared to the leading counterpart, 34% power saving is done with our proposed HCS-BIST scheme.

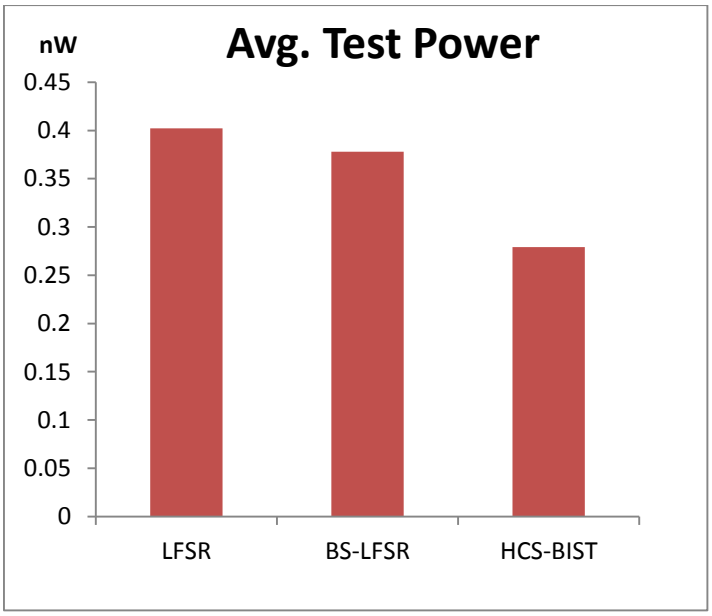

Figure 12. Average Test Power consumption comparison with different BIST schemes.

When compared to the leading counterpart, 30% power saving is done with our proposed HCS-BIST scheme.

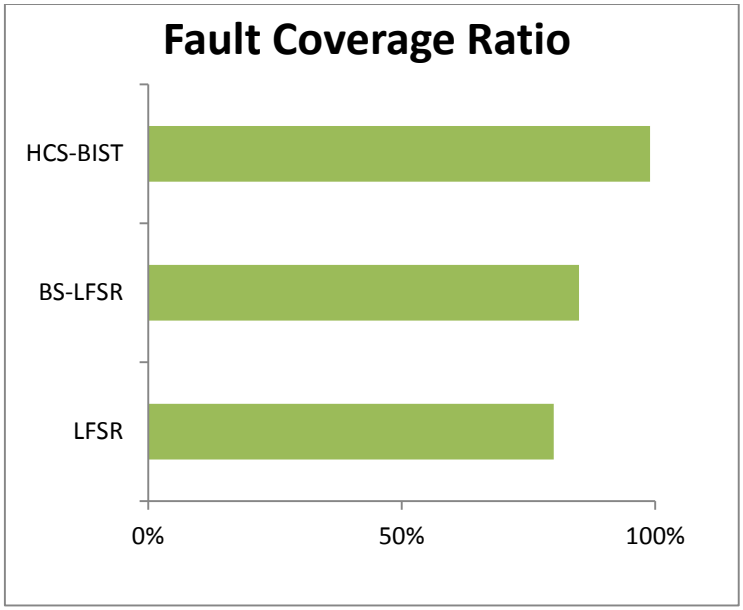

Figure 13. Fault Coverage % comparison with different BIST schemes.

Fault identification and correction of our proposed HCS-BIST scheme is 99%, which is much higher. When compared to leading counterpart, it is 14% more.

CONCLUSION

In this paper, we presented a novel clock divider based LFSR Design exhibiting power reduction and by employing a hamming based BIST system is demonstrating excellent fault coverage with automatic fault correction. Our proposed BIST model, compared to the existing models reduces the power by 30% and fault coverage and correction by 14%. The overall power saving is due to reducing the switching activity of the clock in LFSR. The overall fault coverage with automatic fault correction is improved by 99%. It is also capable of utilizing low area when compared to the existing schemes. For this, the hamming code based clock splitting memory scheme has been implemented and synthesized using Xilinx 14.2 IDE tool. Therefore the proposed BIST scheme is quiet suitable for Ultra Low Power Applications in VLSI memory based design for fault coverage and correction.

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