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Unbalanced Voltage Compensation of Grid Integrated PV System with Fuzzy based Novel Seven Level Inverter

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Abstract

This paper describes a novel 7 level converter based PV grid integration during unbalanced grid condition. The proposed 7 level converter can reduce no. of power electronic devices required and power consumption also. The distorted components of +ve and –ve sequences are regulating by controlling the power injected by the PV in to grid to maintain voltage under balance. A fuzzy based controller is used to control the PV inverter. The combination of multi-level converter with fuzzy controller can reduce the voltage stresses and switching losses of devices. The proposed fuzzy logic controller (FLC) can reduces the time delays compared with proportional plus resonant controller during the dynamic conditions. The proposed 7 level converter with fuzzy controller reduces filtering requirements it can improves system performance to a greater extent.

INTRODUCTION

Now a day's renewable energy sources play a key role to converge conventional sources to future generations. Generally, PV, Wind and fuel sources are the widely used distributed generation (DG), here the integration of DG's facing a challenging issues to maintain grid stability [1]. Here the considerable issues are sag/swell and unbalanced voltage conditions, due to the voltage unbalance grid +ve and –ve sequence voltages are distorted. To maintain system balanced condition; need to control the DG inverter for regulating injection into the grid to compensate –ve sequence components. Here voltage source converter (VSC) is using for power conversion; by providing an effective current controller to VSC the ride through capability of system increases to a greater extent under variety of fault conditions. The VSC with current controller can provides required reactive power to control the fault current under fault condition [2]. Different control strategies are available for regulate symmetrical components defined in [3]-[4]. Here a FLC based multi variable current controller is proposed.

Many researchers designed different types of current controllers, such as current reference without dual Vector [5] and predictive current controllers explained in [6] etc. The FLC controller based controlling is adapted to the system to maintain voltage balance, the FLC based current controller is defined in [7]. The FLC controller can maintain error closer to zero and time taken to respond for error reduction is reduces to a greater extent, due to this stability of the system increases and losses reduces. The performance comparison of proportional plus resonant (PR) controller and FLC is described in [8]. The FLC robust in nature and it have extended dynamic response, due to this the unbalanced voltage are compensated to a greater extent.

The PV generation is integrated with utility grid; in traditional way normal two-level inverter is used for DC to AC power conversion. Here the use of conventional two level inverters for power conversion requires high capacity filtering components to compensate harmonics. The two level converter have high harmonic content, due to this the power consumed by filtering components is increased, power factor reduces, losses increases and cost of filters is also increases. To overcome these disadvantages a novel multi-level converter is introduced. The multi-level converter facilitates to meet high power ratings with low power devices. It can achieve by adding each device voltage and it can reduce the dv/dt effect on device, switches with reduced frequency. Different types of multi-level converter topologies are invented for conversion [9], [10].

Here a novel topology is proposed with reduced no of power electronic devices. The proposed topology contains a seven level inverter; it can convert DC to AC with seven levels in its AC output. The advantages of multi-level converters are due to the steps present in the output can reduces the harmonic percentage, stresses on power electronic devices increases, power conversion capability increases, power factor increases, losses reduce and filtering components required for harmonic compensation is reduces. However, from these, by introduction of multilevel converter in power conversion enhances the system performance greatly.

VSI DESCRIPTION AND FUNDAMENTALS

A. PLL based sequence analyzer

In grid synchronization preferably synchronous reference frame (SRF) based PLL is used for calculate angle and frequency. Where, the SRFPLL have poor performance while detection of angle and frequency under unbalanced grid condition due to distorted frequency. The research on PLL for sequence analysis under unbalanced condition is proposes many techniques, those are explained in [11]-[12]. Behalf of that one new PLL topology was taken for angle detection and explained in [13]. The new PLL includes a concept of moving average filters (MAFs) for enhance speed of detection.

B. Reference current calculation

However, in grid integrated VSC, +ve sequence is regulated; the current of active components is calculated from link voltage of the VSC input and reactive component of current can control using droop controllers [3]. The effective controlling of DC-link voltage achieved by regulating +ve and –ve sequence components of voltage.

The active and reactive components of unbalanced voltage sags are [14]:

$$P = P_0 + P_{c2}cos(2\omega t) + P_{s2}sin(2\omega t) \quad (1)$$

$$Q = Q_0 + Q_{c2}cos(2\omega t) + Q_{s2}sin(2\omega t) \quad (2)$$

Here the average active and reactive powers are P_0, Q_0 and P_{c2}, P_{s2}, Q_{c2} *and* Q_{s2} are the second order components of active and reactive power. The average and second order components of active power are expressed in terms of direct axis and quadrature axis components of current and voltages are

$$P_0 = v_d^+ i_d^+ + v_q^+ i_q^+ + v_d^- i_d^- + v_q^- i_q^- \quad (3)$$

$$P_{c2} = v_d^- i_d^+ + v_q^- i_q^+ + v_d^+ i_d^- + v_q^+ i_q^- \quad (4)$$

$$P_{s2} = v_d^- i_d^+ - v_q^- i_q^+ - v_d^+ i_d^- + v_q^+ i_q^- \quad (5)$$

$$Q_0 = v_q^+ i_d^+ - v_d^+ i_q^+ + v_q^- i_d^- - v_d^- i_q^- \quad (6)$$

$$Q_{c2} = v_q^- i_d^+ - v_d^- i_q^+ + v_q^+ i_d^- - v_d^+ i_q^- \quad (7)$$

$$Q_{s2} = -v_d^- i_d^+ - v_q^- i_q^+ + v_d^+ i_d^- + v_q^+ i_q^- \quad (8)$$

Here v_d^+, v_q^+, v_d^-, and v_q^- *and* i_d^+, i_q^+, i_d^- and i_q^- are the +ve and –ve sequence components of grid voltage and current. Here the terms P_{c2} *and* P_{s2} are varies with unbalanced sags. To compensate these terms the injection is such a way that to maintain P_{c2} *and* P_{s2} are closer to zero.

The injected current defined as follows:

$$\begin{bmatrix} i_d^{+*} \\ i_q^{+*} \\ i_d^{-*} \\ i_q^{-*} \end{bmatrix} = \begin{bmatrix} v_d^+ & v_q^+ & v_d^- & v_q^- \\ v_d^- & v_q^- & v_d^+ & v_q^+ \\ v_q^- & -v_d^- & -v_q^+ & v_d^+ \\ v_q^+ & -v_d^+ & v_q^- & -v_d^- \end{bmatrix}^{-1} \begin{bmatrix} P_0^* \\ P_{c2}^* = 0 \\ P_{s2}^* = 0 \\ Q_0^* \end{bmatrix} \quad (9)$$

FUZZY-PI CONTROLLER (FPIC)

The time domain representation of PI-controller is as follows

$$y(t) = K_p\left(e(t) + \frac{1}{T_n}\int_0^t e(\tau).d\tau\right)$$

$$\int y(t) = K_p\left(e(t) + \frac{1}{T_n}e(t)\right)$$

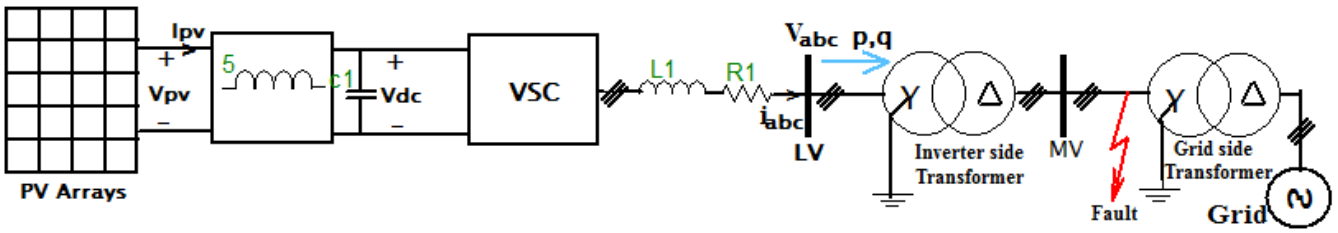


Fig. 1. Single line representation of test system

Applying

$$e \approx \Delta e = e(t) - e(t-1)$$

$$\Delta y \approx \int y(t) \approx y(t) + y(t-1)$$

Fuzzy logic controller with PI is as shown in fig.2. The factors considered for desired operation are e (error), ∆e (change in error) and ∆y (change in output).

An FPI-controller can be handled as a fuzzy inference system, which maps given inputs to an output using fuzzy logic and is interfaced to the other system components with two input variables; *error*, *error change* and one output variable *output change*. The two inputs as well as the output of the FPI controller have normalized universe of discourse ranging from [-1, 1] and represented by seven equally-distributed triangular-shaped membership functions: *NB* (negative big), *NM* (negative medium), *NS* (negative small), *Z* (zero), *PS* (positive small), *PM* (positive medium), *PB* (positive big), Fig. 2-b. The operation of Fuzzy inference systems can be divided into three main steps: fuzzification, rulebase/ inference and finally defuzzification. Fuzzification is the process of converting the crisp input passed to the controller from previous states into fuzzy values, where each crisp value is given a degree of membership to all the membership functions covering the universe of discourse. The inference engine in conjunction with the rule-base (If/Then rules) concludes useful results from the fuzzified inputs; i.e. each fuzzy input is mapped to a fuzzy output according to the used rule-base. Aggregation and accumulation are then performed in order to calculate the fuzzy

output. After the input variables to the fuzzy system are processed by the inference engine and the rulebase, the result is a fuzzy output ⌈*-out(y),* where ⌈-out is the fuzzy set of an output variable *y*. Selecting a crisp number *y** representative of ⌈*-out(y)* is a process known as defuzzification. Several defuzzification techniques exist and the choice of a defuzzification method may have an impact on the speed and accuracy of the inference system. The *center of area* or *centroid* defuzzification is the most commonly used technique [2] and is also used in this work. In this method, the crisp output value is taken to be the geometrical center of the output fuzzy value.

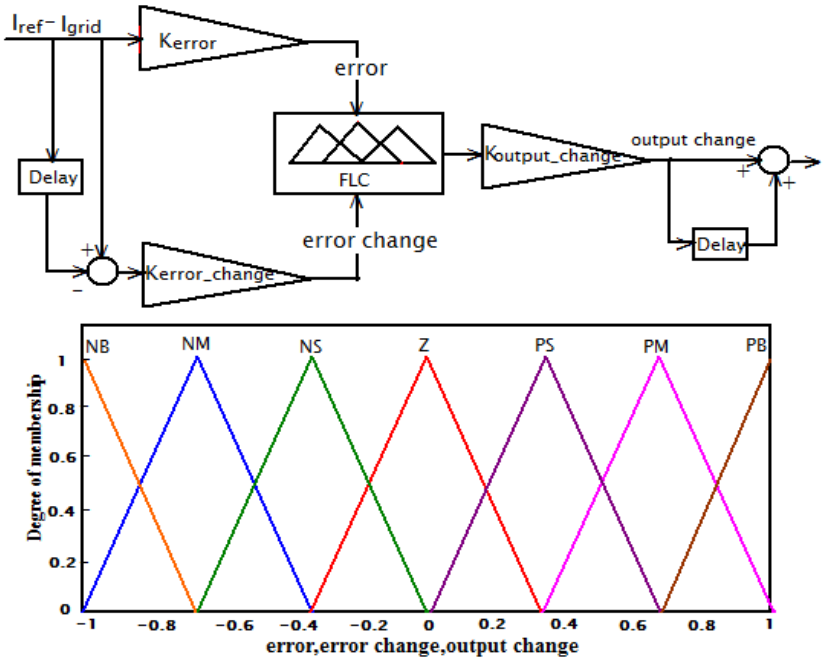


Figure 2.(a) Fuzzy-proportional-integral Controller, ***(b)*** Input/output fuzzymembership functions

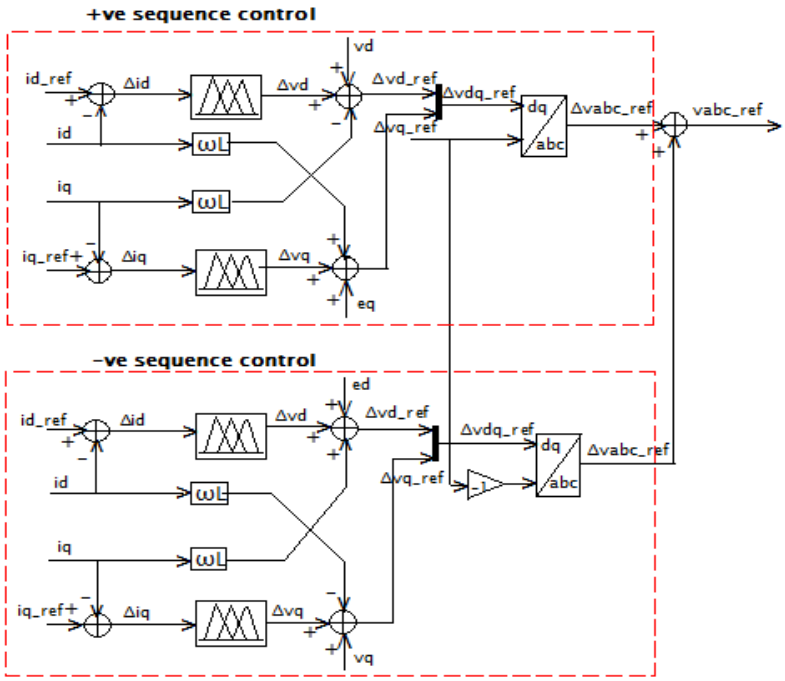


Figure 3. Inner Current control loop with fuzzy logic controller

POWER STAGE

A. Circuit Configuration

Fig. 4 shows the proposed novel topology used in the seven-level inverter. An input voltage divider is composed of three series capacitors *C*1, *C*2, and *C*3. The divided voltage is transmitted to H-bridge by four MOSFET, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFET. The proposed multilevel inverter generates seven levels AC output voltage with the appropriate gate signals design.

B. Operating Principles

The required seven voltage output levels (1/3*V*dc, 2/3*V*dc, *V*dc, 0) are generated as follows:

1) To generate a voltage level *V*o= 1/3*V*dc, *S*1 is turned on at the positive half cycle. Energy is provided by the capacitor *C*1 and the voltage across H-bridge is 1/3*V*dc. *S*5 and *S*8 is turned on and the voltage applied to the load terminals is 1/3*V*dc..

2) To generate a voltage level *V*o= 2/3*V*dc, *S*1 and *S*4 are turned on. Energy is provided by the capacitor *C*1 and *C*2. The voltage across H-bridge is 2/3*V*dc. *S*5 and *S*8 is turned on and the voltage applied to the load terminals is 2/3*V*dc.

3) To generate a voltage level *V*o= *V*dc, *S*1 and *S*2 are turned on. Energy is provided by the capacitor *C*1, *C*2, and *C*3. The voltage across H-bridge is *V*dc. *S*5 and *S*8 is turned on and the voltage applied to the load terminals is *V*dc.

4) To generate a voltage level *V*o= -1/3*V*dc, *S*2 is turned on at the negative half cycle. Energy is provided by the capacitor *C*3 and the voltage across H-bridge is 1/3*V*dc. *S*6 and*S*7 is turned on and the voltage applied to the load terminals is -1/3*V*dc.

5) To generate a voltage level *V*o= -2/3*V*dc, *S*2 and *S*3 are turned on. Energy is provided by the capacitor *C*2 and *C*3. The voltage across H-bridge is 2/3*V*dc. *S*6 and *S*7 is turned on, the voltage applied to the load terminals is -2/3*V*dc. Fig.

6) To generate a voltage level *V*o= -*V*dc, *S*1 and *S*2 are turned on. Energy is provided by the capacitor *C*1, *C*2, and *C*3, the voltage across H-bridge is *V*dc. *S*6 and *S*7 is turned on, the voltage applied to the load terminals is -*V*dc.

7) To generate a voltage level *V*o= 0, *S*5 and *S*7 are turned on. The voltage applied to the load terminals is zero.

Table-I Switching Sequences for generating seven level in the output voltage

	Switching Sequences							
Output Voltages V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	On	off	off	off	on	off	off	On
$2/3V_{dc}$	On	off	off	on	on	off	off	On
V_{dc}	On	on	off	off	on	off	off	On
$-1/3V_{dc}$	off	on	on	off	off	on	on	Off
$-2/3V_{dc}$	off	on	on	off	off	on	on	Off
$-V_{dc}$	On	on	off	off	off	on	on	Off
0	off	off	off	off	on	off	on	Off

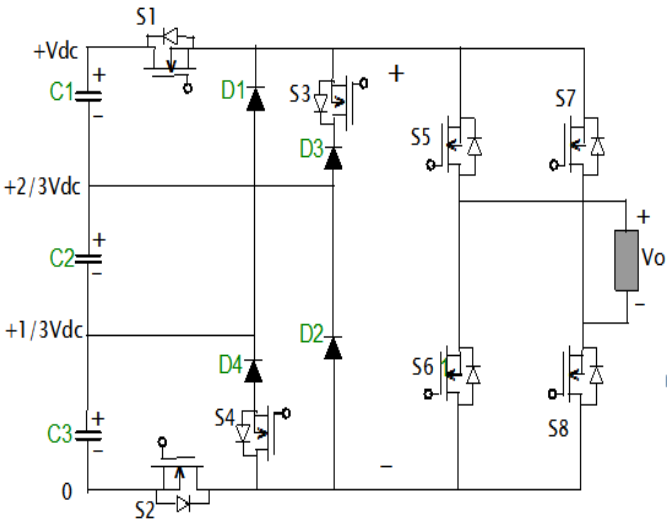
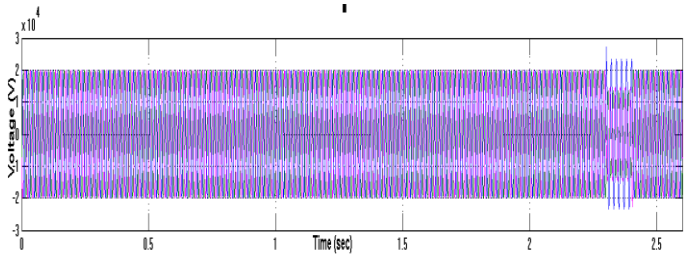


Figure 4. Proposed seven-level inverter topology

SIMULATION RESULT ANALYSIS

The test system consists of grid integrated PV system with two power stages. One for maintain constant dc voltage based on maximum power point tracking and other is for ac/dc conversion. Here a new 7 level topology was introduced to enhance the system performance. The performance of proposed system is analyzed by comparing the conventional and proposed system simulation result is as shown in fig.5 & 6.The test system dynamic performance also tested by applying sudden fault. The fault is initiated at 2.3 sec and cleared after 0.1 sec. By comparing the current under fault the proposed system can limit the fault current effectively.



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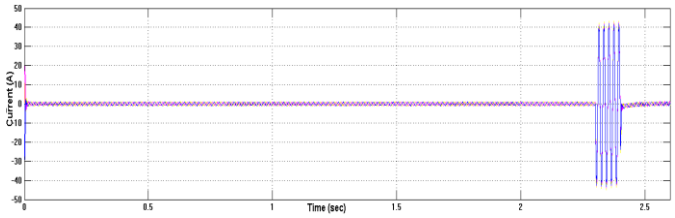

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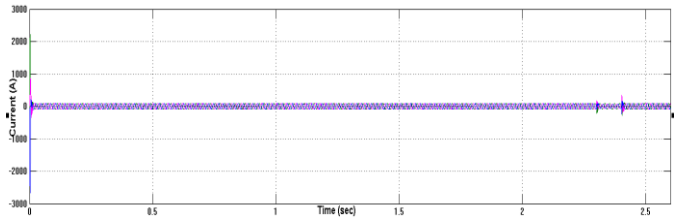

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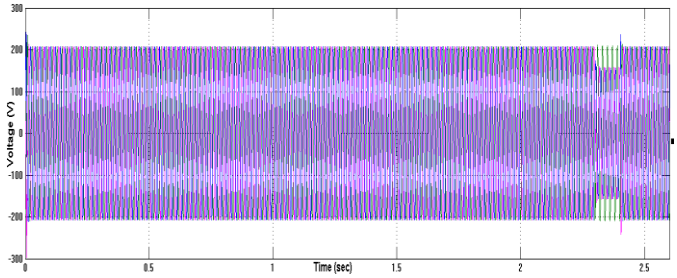

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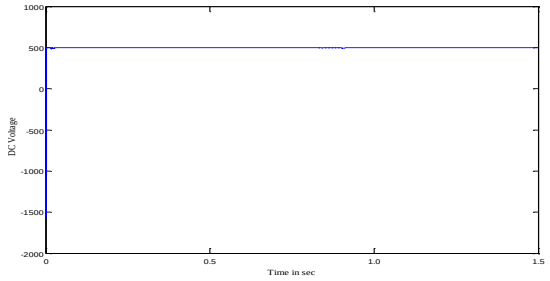
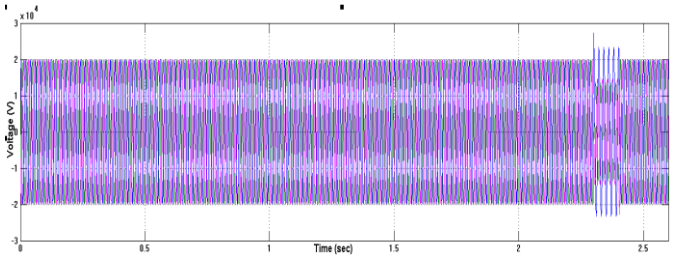
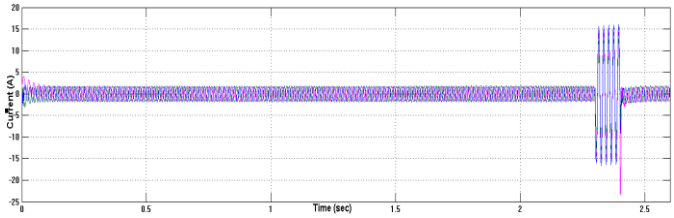


(e)

Figure 5. Traditional inverter with PR controller under fault ***(a)*** voltage at PCC ***(b)*** Current at PCC ***(c)*** & ***(d)*** are the Current and voltage at inverter terminals ***(e)*** Inverter input DC link voltage.



(a)



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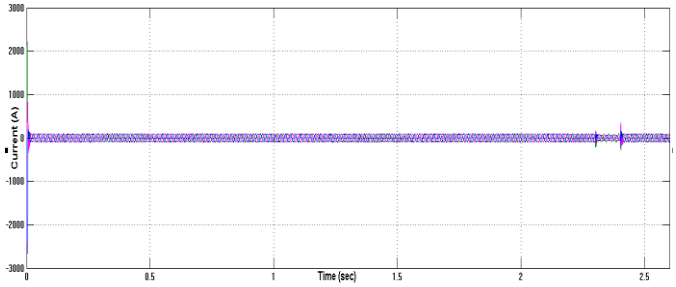

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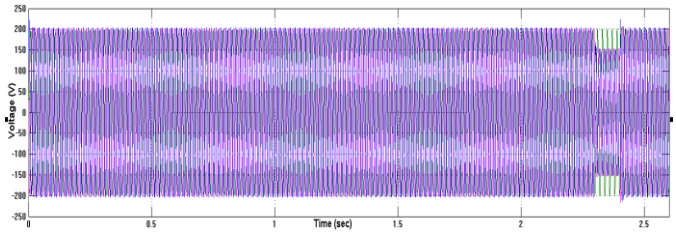

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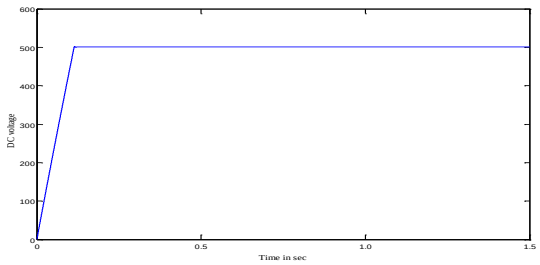


(e)

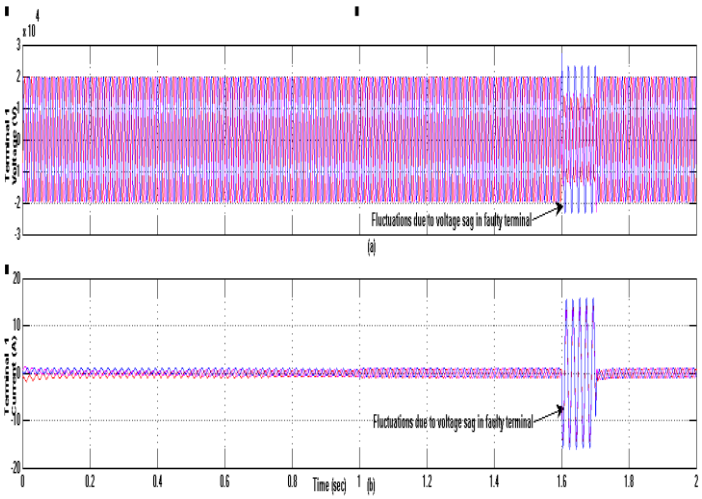
Figure 6. Proposed inverter with fuzzy logic controller under fault ***(a)*** voltage at PCC ***(b)*** Current at PCC ***(c)*** & ***(d)*** are the Current and voltage at inverter terminals ***(e)*** Inverter input DC link voltage.

Conventional two level inverter terminal current has THD is 4.69% and voltage have 13.12%. It was reduced with proposed system.

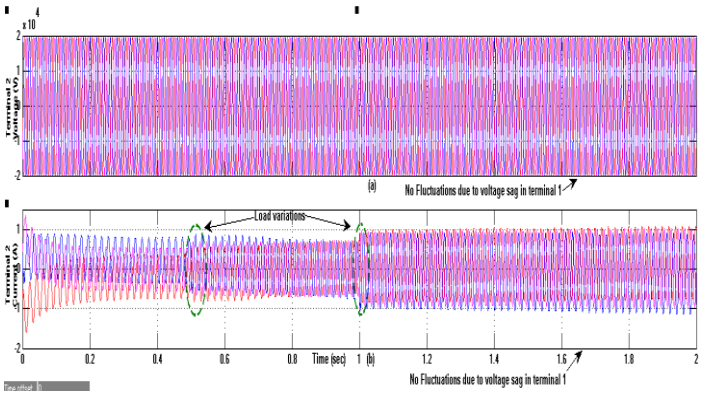
The proposed system terminal current harmonics are reduced to 3.2% (THD) and voltage harmonic percentage is 6.82% (THD). By comparing conventional and proposed fuzzy with

multilevel converter can improves the system performance to a greater extent.

In addition to this a multi-terminal HVDC is developed by connecting another terminal at dc link capacitor. Here the initial terminal is considered as terminal 1 (main or faulty terminal) and another one is as terminal 2 (healthy terminal). The system is implemented by using proposed control topology that is fuzzy logic controller. The active fault current control with fuzzy logic controller during fault ride through operation is developed by using MATLAB/Simulink. The fault occurs in the grid side main terminal shown in Fig.1. during the time interval of 1.6s-1.7s, which is due to the voltage sags. However, it does not effect on the other healthy terminal shown in Fig.7. Here the load variations are considered at the intervals of 0.5s and 1s.



(a)



(b)

Figure 7. Multiterminal HVDC based GCPPP with fuzzy logic controller **(a)**PCC voltage and current of Terminal 1(faulty terminal) (b) PCC voltage and current of Terminal 2(Healthy terminal)

CONCLUSION

The proposed system introduces a novel multi-level converter based grid integrated PV system with fuzzy logic controller. Introduction of multilevel converter can reduces the filtering requirement and increases the power conversion capability of the converter. The proposed converter was a new topology to reduce number of devices required for conversion. The test system is subjected to fault; the faulted system sequence components are distorted. The distorted components are compensated by regulating the injection of multilevel inverter. Here by introducing fuzzy controller in current control will give better response and it will smoothen the system compared with traditional PR controllers. The combination of multi-level converter with fuzzy controller can reduces the %THD from 13.12 to 6.82.

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