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Threshold Voltage Modeling for Nanometer Scale Junction Less Double Gate MOSFET

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Abstract
Most of the existing transistors used in fabrication of integrated chips are with junctions. The device scaling is growing the channel length between junctions in devices are scaling gone down to 10 nm. For smooth functioning of the device extremely high doping concentration gradients become necessary. These junction are becoming increasingly difficult to fabricate. The newer devices have been proposed and demonstrated in which there are no junctions and no gradients of doping. One such device is the Double Gate Metal Oxide Semiconductor Field Effect Transistor (DG-MOSFET) without junction which shows remarkable performance against short channel effects such as Drain Induced Barrier Lowering (DIBL), threshold voltage roll-off, etc. In this paper, a two dimensional model of threshold voltage is considered to study the performance of DG-MOSFET. The model used shows how the DG-MOSFET parameters such as the silicon thickness, oxide thickness, drain bias, and channel length, affect the threshold voltage degradation.

Keywords: Junction less (JL) Double Gate MOSFET, Junction Based (JB) Inversion Mode MOSFET, DIBL, SCEs

INTRODUCTION

The MOSFETs with no junctions built on silicon-on-insulator (SOI) have been demonstrated in [1]-[2]. The junction less (JL) MOSFETs have high impurity concentrations in channel, source and drain regions [3].The basic concept of junction less MOSFET is to use the bulk conduction mode with simplified source and drain engineering without junctions and also sizing the thickness of silicon with large doping concentrations to allow switching the devices with gate. The fabricated device shows improved on/off capabilities [1], [2]. There are several advantages of the junction less MOSFET over classical inversion mode MOSFET devices such as improvements in subthreshold swing slope, large on-current and DIBL [4]. The authors in Refs. [5]-[6] suggest better analog performance of junctionless devices.

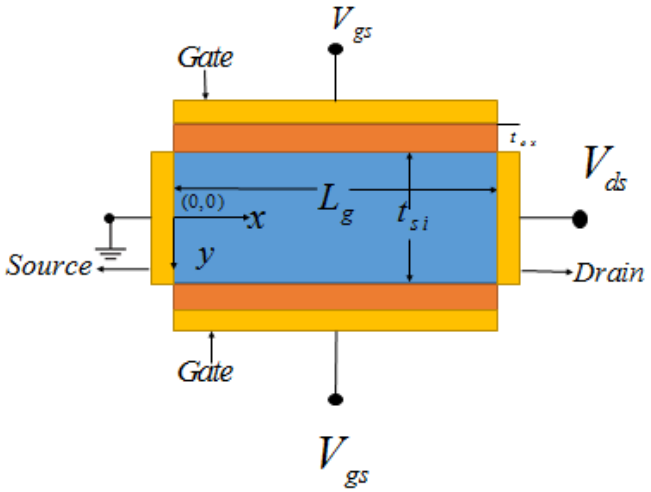

Figure 1. 2-D Schematic Diagram of JL double-gate MOSFET. The drain and gate biases are denoted by *V*ds and *V*gs, respectively. The source and drain regions are assumed to have zero thickness and are located along the left and right side of highly doped silicon-film.

With the growing demand of the JL MOSFETs in circuits, it is important to devise the physical device models. In the literature, several references on the analytical modeling for junction less double-gate MOSFETs [7]–[10] and surrounding gate MOSFETs [11]–[13] have been reported, which focus primarily on analyzing the long-channel behavior and characteristics. The short channel behavior of the devices in the deep submicrometer regime cannot be predicted. The variation in threshold voltage of short channel MOSFETs plays a significant role in circuit applications and is significantly effected by changes in device parameters such as channel length, drain bias, silicon thickness, and gate oxide thickness. An analytical short-channel threshold voltage model for JL double-gate MOSFETs is investigated which is based on the bulk conduction mode of the 2-D Poisson equation [14]. The analytical model of short channel effects in JL MOSFETs, such as the threshold voltage roll-off with the gate length, and DIBL, is established. The work gives insights to the device physics and also provides easier understanding of threshold voltage behavior with a simple formula.
The organization of the paper is as follows. Section-II describes the threshold voltage model. Simulation results are discussed in section III. Finally the conclusion is drawn in section IV.

THRESHOLD VOLATGE MODEL

The cross-sectional view of the JL DG MOSFET is shown in Fig. 1, the symbols used for the geometrical representation are defined as: L_g is the gate length, t_{Si} is the Si-layer thickness, $V_{gs}$is the gate to source voltage and V_{ds} is the drain to source voltage. The coordinate systems are set as *x*-axis is pointing towards the drain and the *y*-axis is along the Si layer thickness. The Si layer is assumed to have uniform doping donor atoms concentration N_D.

The operating principle of JL DG MOSFET is quite the opposite of junction based MOSFETs. In inversion mode devices the minority carriers are induced at *Si-SiO₂* interface, whereas in JL devices bias at the gate helps in accumulating and depleting the majority carriers from highly doped silicon body. The JL based devices can be made both normally off and normally on. The normally off JL DG MOSFET will conduct current through the silicon body if positive bias is applied to the gate, which is the otherwise pinched off due the contact potential between gate and silicon layer. The JL MOSFET is essentially a volume conduction device in which the majority carriers flow in the volume of the silicon body, whereas in junction based (JB) MOSFET the induced minority carries flow at the surface between the gate oxide and silicon body. In the subthreshold region, the channel can be assumed fully depleted, and the 2-D Poisson equation for the N-Channel JL DG MOSFET can be written as

$$\frac{\partial^2 \psi(x,y)}{\partial y^2} + \frac{\partial^2 \psi(x,y)}{\partial x^2} = \frac{-q N_D}{\varepsilon_{Si}} \quad (1)$$

where$\psi(x,y)$ is the 2D channel potential and N_D is the uniform channel doping density. The 2D boundary conditions are described by

$$\psi(0,y) = 0 \quad (2)$$

$$\psi(y, L_g) = V_{ds}\psi(y, L_g) = V_{ds} \quad (3)$$

$$\psi\left(\frac{t_{si}}{2}, x\right) = \psi\left(-\frac{t_{si}}{2}, x\right) \quad (4)$$

and

$$\left[C_{ox}V_{gs} - C_{ox}\emptyset_{ms} - C_{ox}\psi\left(\frac{t_{si}}{2}, x\right)\right] = \pm\varepsilon_{si}\left[\frac{\partial\psi}{\partial y}\right]_{y=\pm t_{si}/2} \quad (5)$$

The 2D Poisson equation in (1) can be further reduced to the quasi 2D equation with the bulk conduction mode [14]. We assume here

(i) The continuous electrical flux between the silicon body and gate oxide.
(ii) The electrical field at $y = 0$ is zero due to the channel potential symmetry along the *y*-direction. It gives

$$\frac{\partial^2\psi(x,y=0)}{\partial x^2} - \frac{1}{S^2}(\psi(x,y=0) - \psi_c) = 0 \quad (6)$$

where ψ (*x*, *y* = 0) is the central potential, $\psi_c$is the long channel central potential, and *S* is the scaling length. They are given as

$$S = \sqrt{\frac{4t_{si}\varepsilon_{si} + C_O t_{si}^2}{8C_O}} \quad (7)$$

$$\varphi_c = Vgs - \theta \quad (8)$$

$$\theta = \left[\emptyset_{ms} + \frac{qN_D t_{si}}{2C_o} + \frac{qN_D t_{si}^2}{8\varepsilon_{si}}\right] \quad (9)$$

where $\emptyset_{ms}$ is the work function difference between the silicon film to gate dielectric interface and $C_o$is the oxide capacitance per unit area. The general solution of the ordinary differential equation in (2) can be obtained as

$$\psi(x, y = 0) = \Psi_c(x) = ae^{\frac{1}{S}x} + be^{-\frac{1}{S}x} + \psi_c \quad (10)$$

With boundary conditions $\psi(x = 0, y = 0) = 0$ and $\psi(x = L_g, y = 0) = V_{ds}$, the parameters a and b in (10) can be obtained as

$$a = \alpha V_{gs} + \beta \quad (11)$$

$$b = \gamma V_{gs} + k \quad (12)$$

With

$$\alpha = \frac{e^{-V} - 1}{2\sinh(V)} \quad (13)$$

$$\beta = \frac{V_{ds} - \theta(e^{-V} - 1)}{2\sinh(V)} \quad (14)$$

$$\gamma = \frac{1 - e^{V}}{2\sinh(V)} \quad (15)$$

$$k = \frac{-V_{ds} + \theta(e^{V} - 1)}{2\sinh(V)} \quad (16)$$

where

$$V = \frac{L_g}{S} \quad (17)$$

By setting $\psi_{c,min} = 0$ and solving for the gate bias V_{gs}, the short-channel threshold voltage for JL double-gate MOSFETs can be obtained as

$$Vth = \frac{2(\beta\gamma + k\alpha) + \theta + \sqrt{(2(\beta\gamma + k\alpha) + \theta)^2 - (1 - 4\alpha\gamma)(\omega^2 - 4\beta k)}}{1 - 4\alpha\gamma} \quad (18)$$

RESULTS AND DISCUSSION

The model studied in this paper can also be used for modeling the inversion mode (IM) for the JB double-gate MOSFET. In this paper, JB-IM denotes the IV operation mode for the JB double-gate device, and the normally off operation for the JL double-gate MOSFET is denoted by JL-DM. Fig. 2 plots the variation of threshold voltage roll-off with the effective channel length for different silicon-film thicknesses. The simulation results of the JL-DM MOSFET and JB-IM MOSFET are compared. It is observed that the threshold voltage roll-off increases by reducing the effective channel length. The comparison is done with for different silicon layer thickness (t_{si}) of 15nm, 10nm, and 5nm. The results show that the 5nm silicon layer provides better threshold voltage roll-off compared with 15nm silicon thickness. The JB-IM device show more degradation than the JL-AM device because of short channel effects. The performance of JL-DM is better with the thin silicon film but that can seriously affect current carrying capacity. The tradeoff between threshold voltage

degradation and current driving capability must be taken into consideration.

Fig. 3 plots the variation of threshold voltage roll-off with the effective channel length at different gate oxide thicknesses (t_{ox}). The simulation of the JL-DM MOSFET and JB-IM MOSFET are obtained. The comparison based on simulation result are made. The smallest threshold voltage roll-off is demonstrated by the thinnest gate oxide of t_{ox}= 1 nm. As there is no source/drain depletion region in the channel of the JL-DM device, it enhances the channel potential barrier and suppresses more short channel effects than the JB-IM device [15].

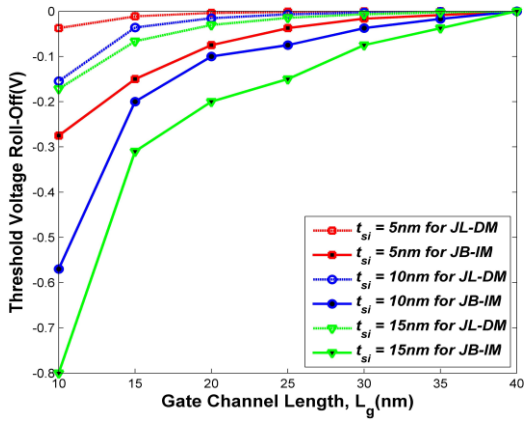

Figure 2. Variation of the threshold voltage roll-off with the effective channel length for different silicon-film thicknesses. The simulation of the JL-DM MOSFET and JB-IM MOSFET are obtained. The comparison based on simulation result are made. The highly doped N-type silicon with doping densities of $N_{d,JL}$= 1 × 10^{20} cm^{-3} and $N_{d,JB}$= 1 × 10^{20} cm^{-3} are used for the silicon film of the JL-DM device and the source/drain region of the JB-IM device, respectively. The effective channel length for the JL device is L_g, and the effective channel length for the JB device is defined by $L_g - L_s - L_d + 2L_D$ [16].

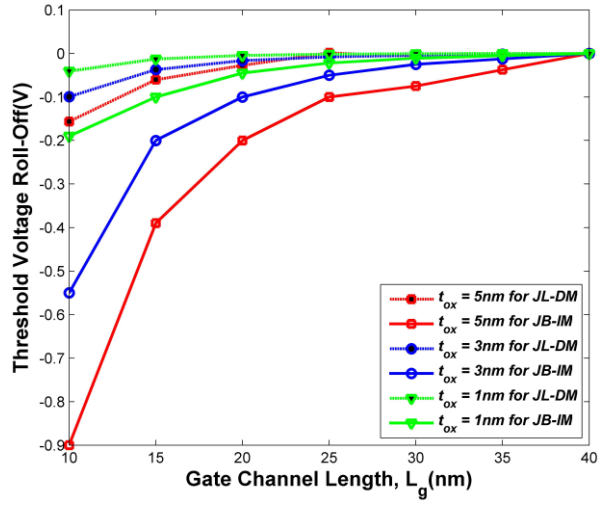

Figure 3. Variation of the threshold voltage roll-off with the effective channel length for different oxide thicknesses. The simulation of the JL-DM MOSFET and JB-IM MOSFET are done. The comparison based on simulation result are made.

The variation in DIBL with the effective channel length for different drain biases is shown in Fig. 4. The JL-DM MOSFET simulation results are compared with JBIM MOSFETs. The DIBL is defined by the difference between the threshold voltage of the low drain bias of V_{ds1}= 0.1 V and that of the high drain bias of V_{ds2}= 0.5, 1.0, and 1.5 V. DIBL gives insights that how high drain voltages affect the operation of short channel devices in nanometer regime. To effectively reduce the effect of DIBL, a low drain bias is required. The JB-IM device with source/drain encroachment on the channel region results in more DIBL than that of JL-DM device. Although quantum mechanics effects (QMEs) are not accounted in this work, it has been shown in [17] that QMEs will enhance the channel potential barrier and increase the threshold voltage in comparison to the electrostatic effects Hence, it is reasonable to conclude that the threshold voltage in Figs. 2–3 will be increase upwards with the inclusion of QMEs.

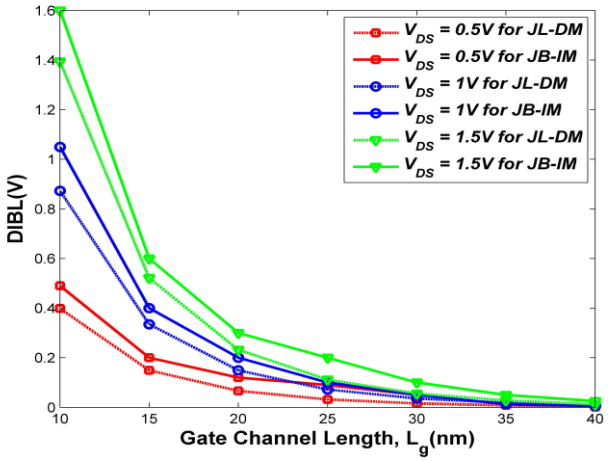

Figure 4. DIBL variation with the effective channel length for different drain biases. The simulation of the JL-DM MOSFET and JB-IM MOSFET are done. The comparison based on simulation result are made.

CONCLUSION

With the 2-D scaling equation in bulk conduction mode, a short-channel threshold voltage for JL DG MOSFETs has been obtained. The JL device has proved to give better performance than the JB device in terms of reducing threshold roll-off, decreasing DIBL, and increasing design space. The thin silicon film and thin gate oxide are required to suppress short channel effects which affect the traditional MOSFSTs in great deal. The formula gives easy insights to device operation and can be used for device simulation for future devices.

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