

Simulation Study on Scalability Improvement of Logic Transistors with MoS₂ Channel and N⁺/P⁺ Si Tunnel Junction

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Abstract

This paper presents the proposal of hybrid device structure using MoS₂ layer and Tunnel FET (TFET) on SOI substrate to improve the scalability of logic transistors for sub-0.5V application based on simulation works. The proposed hybrid device has a MoS₂ layer as the channel and N⁺/P⁺ Si junction at the source edge to provide the heterogeneous structure of two-dimensional (2D) FET and TFET devices. It has been observed that the proposed device shows the reasonable DIBL (Drain-Induced Barrier Lowering) of 50mV even for 10nm gate length. In particular, the proposed devices have the subthreshold slope of 32mV/dec @10nm gate length) by applying N⁺/P⁺ Si tunnel junction at the source side. Also, the proposed hybrid FET with gate length of 4nm is demonstrated to threshold voltage of 0.1V and reasonable I_{off} of 300nA/um @V_{ds} of 0.5V by applying extremely thin MoS₂ channel of 1nm.

Keywords: MoS₂ FET, Band-to-band tunneling (BTBT), Low voltage operation, Field-effect transistor (FET), Tunnel FET (TFET), Silicon-on-insulator (SOI), Subthreshold slop, 2D channel FET, Heterogeneous structure.

INTRODUCTION

In recent technology nodes, much effort has been made to scale down gate length without remarkable short channel effect (SCE) for enjoying density and performance benefits. Bulk structure is replaced by FinFET structure to suppress the off-state leakage current [1], [2]. As gate pitch is decreased to 45nm and smaller, since gate length should be scaled down even to 10nm or less to guarantee the reasonable contact-hole dimension, another device structures such as nanowire and 2D channel FET attract much attention [3].

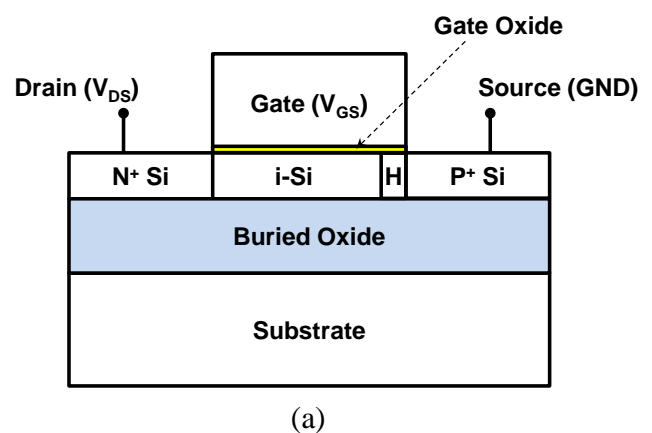
Since standard MOSFET (Metal-Oxide-Semiconductor Field-Effect-Transistor) devices are basically governed by Boltzmann Dirac distribution, they have the lower limit of 60mV/decade for subthreshold slope (SS), leading to a negative candidate for low voltage operation less than 0.5V [4]. Due to very steep SS behavior, several devices such as tunnel FETs (TFET), impact-ionization MOSFETs and NEMFET, etc. have been under intensive study to achieve extremely low standby leakage and low threshold voltage (V_{th}) for sub-0.5V supply

voltage applications [4]. However, it is reported that TFETs suffer from the increase of off-state leakage current (I_{off}) due to the increased intra-band tunneling from the source to the drain as with gate length scaled down to 10nm [5].

In this paper, the hybrid device structure is proposed to improve the scalability of gate length for sub-0.5V voltage operation. The proposed device is a hybrid FET having a heterogeneous structure, where the channel layer is 2D material such as MoS₂ to increase gate controllability and N⁺/P⁺ tunneling junction is formed at the source edge to address the steep subthreshold slope required for low voltage operation. Simulation results on this hybrid device will be given focusing on the scalability improvement and the background physics.

SIMULATIONS

Figure 1 (a) and (b) show the structures of the n-channel TFET (NTFET) for reference and the proposed hybrid FET used in this study, respectively. Both NTFET and proposed hybrid FET have basically a single-gated p-i-n structure and dopant pocket region near the source region on SOI substrate to improve gate contribution on tunneling efficiency [5]. However, the difference between two devices is the channel material, where the material is intrinsic silicon (i-Si) for NTFET and MoS₂ for proposed hybrid FET.



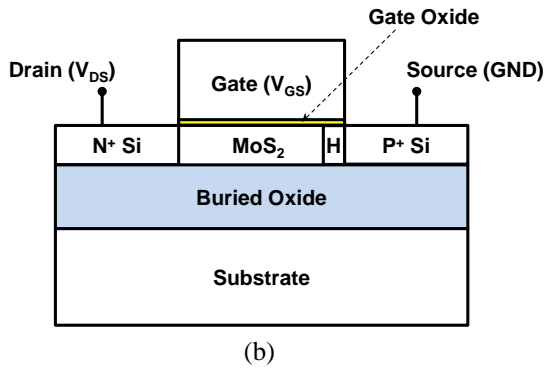


Figure 1. The structures of (a) n-channel TFET (NTFET) for reference and (b) the proposed hybrid FET used in this study. Both NTFET and proposed hybrid FET have basically a single-gated p-i-n structure and dopant pocket region near the source region on SOI substrate to improve gate contribution on tunneling efficiency. The proposed hybrid FET has MoS₂ layer as the intrinsic channel.

The simulation tool to investigate the drivability improvement of NTFET in this paper is SILVACO TCAD ATLAS [6]. BTBT (Band-to-Band Tunneling) mechanism has been modeled using the dynamic nonlocal path tunneling approach, taking into account the nonlocal generation of electrons and holes caused by direct and phono-assisted processes. The device parameters throughout this work (if not differently specified) are the following: doping concentration of source and drain region $N_D = N_A = 1 \times 10^{21} \text{ cm}^{-3}$; intrinsic channel (I-channel) doping concentration $N_D = 1 \times 10^{15} \text{ cm}^{-3}$ for NTFET and $1 \times 10^{13} \text{ cm}^{-3}$ for hybrid FET Halo width 2nm; lifetime in the channel $t = 1 \times 10^{-6} \text{ sec}$ for NTFET; gate work function $F_G = 4.25 \text{ eV}$; supply voltage $V_{GS} = V_{DS} = 0.5 \text{ V}$. Other structural parameters of two devices for simulation are summarized in Table I.

Table I. Typical structural and material parameters of NTFET and the proposed hybrid FET used for simulation works.

		NTFET	Proposed Hybrid FET
Substrate		SOI (Silicon-On-Insulator)	
EOT		0.8nm	
Channel	Material	Si	MoS ₂
	Bandgap @300K	1.12 eV	1.4 eV
	Permittivity	11.9	4.0
	Low-field mobility	1480 cm ² /V.s	60 cm ² /V.s
	Thickness	8nm	
Pocket Region		N+ doped Si (2nm)	
Drain Region		N+ doped Si	
Source Region		P+ doped Si	
Overlap of Gate and Si Tunnel Junction		2 nm	

RESULTS and DISCUSSION

Figure 2 shows the energy band structure of the proposed hybrid FET with gate length of 10nm, where the source & drain regions are P+ & N+-doped Si, respectively, and the channel region is composed of MoS₂ (8nm) and N+-doped Si (2nm). It can be seen that there is band offsets at both the drain edge and the pocket edge due to the insertion of higher bandgap material (i.e., MoS₂) into the channel region. In particular, the band offset between the MoS₂ and pocket regions may have an effect on carrier flow from the source to the drain.

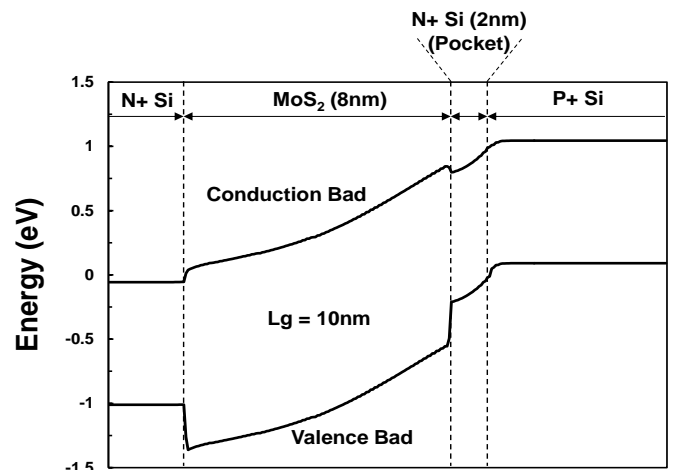


Figure 2. The energy band structure of the proposed hybrid FET with gate length of 10nm, where the source & drain regions are P+ & N+-doped Si, respectively, and the channel region is composed of MoS₂ (8nm) and N+-doped Si (2nm).

Figure 3 (a) and (b) shows the simulated $I_{DS}-V_{GS}$ curves of NTFET and proposed hybrid FET for gate lengths of 10nm and 20nm, respectively. It can be seen that two devices shows quite different subthreshold behaviors with the decrease of gate length from 20nm to 10nm. As shown in Fig. 3(a), for the gate length of 20nm, the proposed hybrid FET has relatively similar electrical behaviors compared with NTFET; higher threshold voltage (V_{th}) of 0.228V vs 0.207V, comparable subthreshold slope of 15mV/dec vs 14mV/dce, and smaller DIBL (drain-induced barrier lowering) of 28mV vs 50mV. In particular, it is worthy noticing that the proposed hybrid FET shows very step subthreshold slope of 15mV/dec thanks to the insertion of N+/P+ tunnel junction at the source edge, although it has 2D channel of MoS₂ having subthreshold slope higher than 60mV/dec. Furthermore, this desirable behavior of the proposed hybrid FET becomes much significant with much scaled-down gate length, as shown in Fig. 3(b).

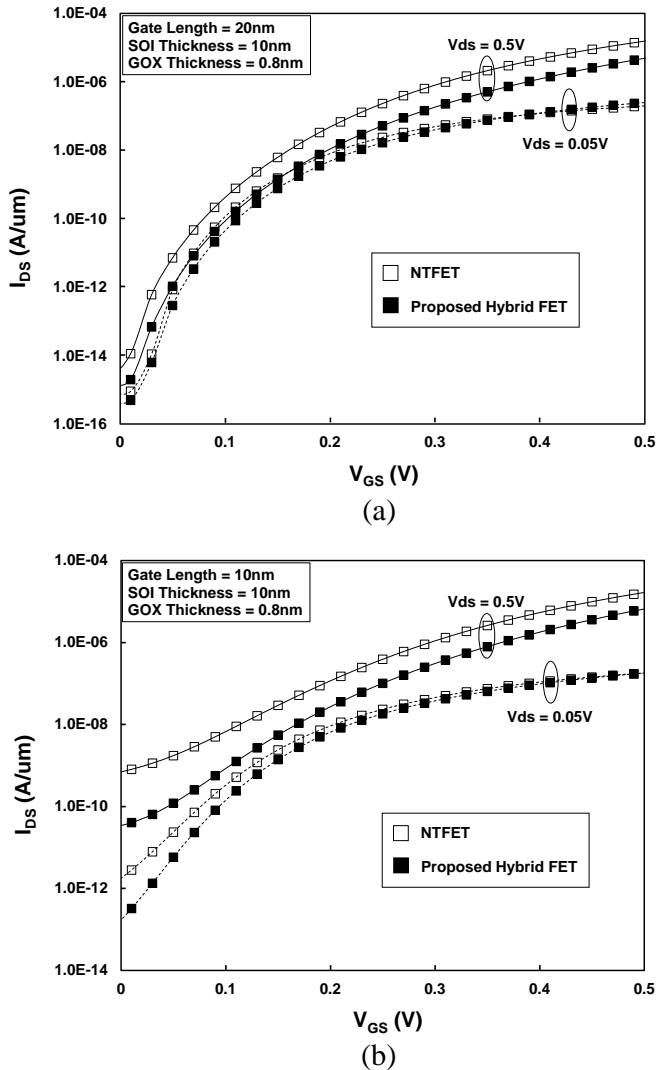


Figure 3. The simulated I_{DS} - V_{GS} curves of NTFET and proposed hybrid FET for gate lengths of 20nm (a) and 10nm (b), respectively.

With gate length decreased to 10nm, NTFET shows much degraded subthreshold behavior such as highly increased subthreshold slope of 42mV/dec (vs 14mV/dce @20nm gate length), higher DIBL of 95mV (vs 50mV @20nm gate length), and much increased off-state leakage current by three orders of magnitude. This is believed to be due to the increased intra-band tunneling. On the other hand, the proposed hybrid FET shows still reasonable subthreshold behavior even for gate length of 10nm, as shown Fig. 3(b). Even though degraded compared with 20nm gate length case, the proposed hybrid FET with 10nm gate length has DIBL of 50mV/dce, steep subthreshold slope of 32mV/dec, and off-state leakage current of a few tens of pA/um range. Thus, the steep subthreshold slope even with 10nm gate length is most remarkable merit of the proposed hybrid FET.

In order to understand the origin of remarkable behavior of the proposed hybrid FET, the vertical and lateral electric field in the channel has been investigated both for NTFET and the proposed hybrid FET. Fig. 4 shows simulated electric field of

two kind of devices with gate length of 10nm, where 0.5V voltage is applied both to the gate and drain. It can be seen that the vertical electric field is higher for the proposed hybrid FET than for NTFET all through the channel. However, the lateral electric field shows different behaviors with the location in the channel. In the pocket region, NTFET has higher lateral electric field than the proposed hybrid FET, leading to the carrier tunneling from the source to the channel. In the intrinsic channel region, the proposed hybrid FET has higher electric field than NTFET. Considering the vertical and lateral electric field in the intrinsic channel region, the effective electric field is comparable both for NTFET and the hybrid FET. In conclusion, it is believed that much improved subthreshold behavior of the proposed hybrid FET with gate length aggressively scaled down to 10nm is due to the decreased electric field in the pocket region resulted from the existence of band offset between MoS₂ and doped Si regions. Since this band offset in the channel region is like to cause the increase of V_{th} and the decrease of on-state current, the proposed hybrid FET needs to be optimized in terms of device parameters such as channel material, device structure, and doping concentration.

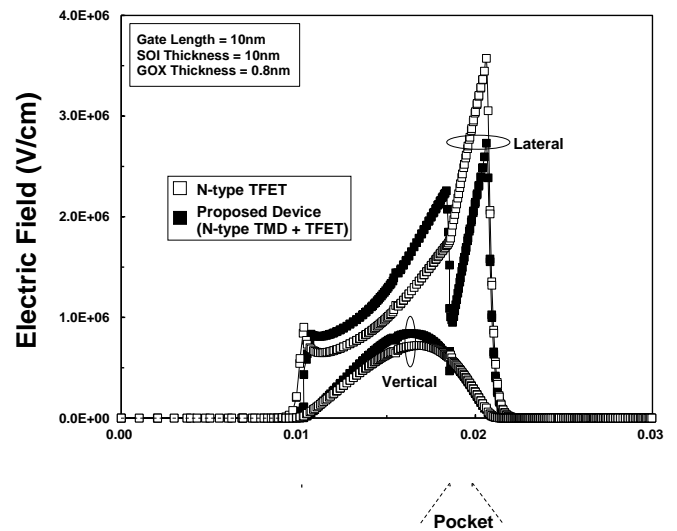


Figure 4. The simulated electric field in the channel region for two kind of devices with gate length of 10nm, where 0.5V voltage is applied both to the gate and drain. Inset shows the energy band structure of the proposed hybrid FET with gate length of 10nm, where the source & drain regions are P+ & N+-doped Si, respectively, and the channel region is composed of MoS₂ (8nm) and N+-doped Si (2nm).

The scalability of the proposed hybrid FET has been investigated as a function of channel (MoS₂) thickness. Fig. 5 shows threshold voltage (V_{th}) and off-state leakage current (I_{off}) behaviors of the proposed hybrid FET with gate length scaling for different MoS₂ thickness, where all simulated devices have gate oxide thickness of 0.8nm, halo width of 2nm, and gate-to-source overlap of 0nm. It can be seen that the proposed hybrid FET shows V_{th} roll-off behavior with both gate length and MoS₂ thickness, and that its I_{off} increase with scaling down the gate length is retarded with decreasing MoS₂

thickness. More to the point, with scaling down the gate length to 6nm or below, the 1nm-thick MoS₂ channel case shows normal transistor's I-V behavior, but thicker (3nm to 7nm) cases suffer from the source-to-drain punch through resulted from the direct tunneling.

field in the channel resulted from the application of 2D material in the intrinsic channel.

The proposed hybrid FET needs to address the increased V_{th} and decreased on-state current drivability due to the band offset in the channel near the source edge. However, although the structural optimization and process design is needed for performance improvement, this kind of hybrid FET will help improving the scalability of logic transistors as well as preparing the device platform for sub-0.5V applications.

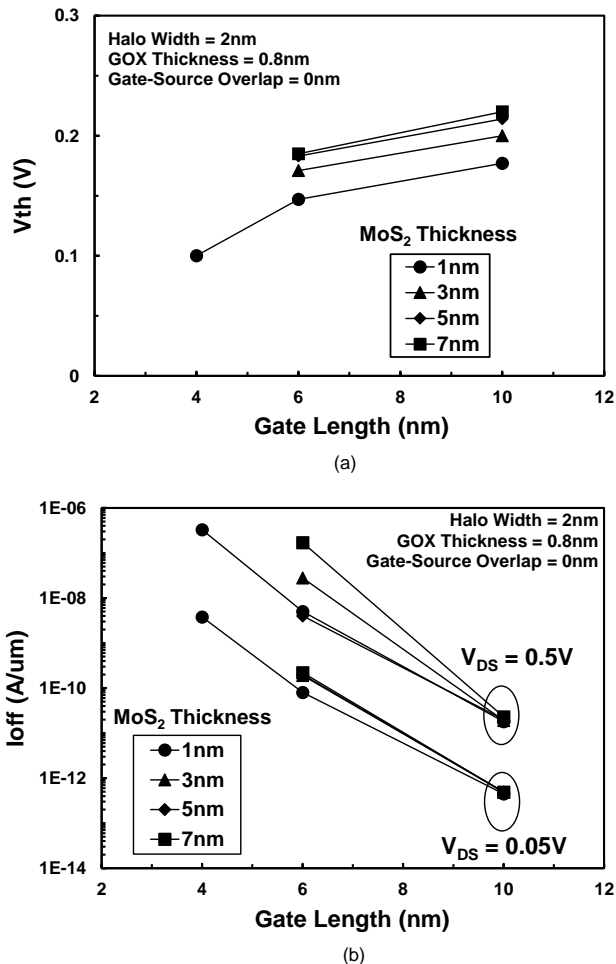


Figure 5. Threshold voltage and off-state leakage current behaviors of the proposed hybrid FET with gate length scaling for different MoS₂ thickness, where all simulated devices have gate oxide thickness of 0.8nm, halo width of 2nm, and gate-to-source overlap of 0nm.

CONCLUSIONS

In this paper, the hybrid FET is proposed to extend the scalability of logic transistors for sub-0.5V application based on simulation works. The proposed hybrid FET is TFET with the intrinsic region of 2D channel material such as MoS₂, where the channel region under the gate is composed of the intrinsic channel and the tunneling junction (i.e., N⁺/P⁺ Si). The proposed hybrid FET shows remarkable subthreshold behavior such as DIBL of 50mV/dec and steep subthreshold slope of 32mV/dec even with gate length decreased to 10nm. This is believed to be due to carrier injection by band-to-band tunneling at the N⁺/P⁺ doped junction and suppressed electric

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BIOGRAPHY

Jong-Wook Lee received the B.S. degree in electronics from the University of Ajou, Suwon, Korea, in 1989, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Taejon, in 1992 and 1996, respectively.

During semiconductor industry experiences, he worked for major chip makers such as Hynix, NEC (Japan), and Samsung Electronics. He had involved in the development of SOI DRAM (Hynix), FDSOI device and process (NEC), and 14nm logic process technology (Samsung Electronics). Also, he is co-inventor of vertical NAND structure (i.e., TCAT) of Samsung Electronics. He joined the department of Electrical and Computing Engineering, Ajou University in Sep., 2014. His research themes include device structure and materials for sub-0.5V voltage operation, scaling-down enabling technology, low-power, high-speed devices and circuits, system-on-chip using 3-D devices and technology, development of multi-chamber, and multi-purpose processing system.

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