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# Design and Implementation of Enhanced Leakage Power Reduction Technique in CMOS VLSI Circuits

**Ayesha Firdous [1], M.Anand [2] and B.Rajan [3]**

[1,2] *Department of ECE, Dr.M.G.R. Educational and Research Institute University, Chennai, India.*

[3] *Department of ECE, Jawahar Engineering College, Chennai, India.*

**Abstract**

The rapid increase of semiconductor technology and growing demand for portable devices powered up through battery has led the constructors to scale down the feature size; resultant reduced threshold voltage as well as thereby enabling integration of incredibly complex functionality on a single chip. In both technological and implementation aspects Chip's maximum power approach is adopted. To increase the concert of devices, the three key factors are essential such as speed of the system, small area, and low power consumption. Specifically, in the integrated devices total power consumption is influenced by the leakage current dissipation. For high performance applications with minimal voltage and power reduction of leakage power is of major concern. Power leakage minimization demand may be due to fast development of power electronic devices operated in batteries like cell phones, laptops, and other handheld devices. In the near past, many of them have focused towards tackling the issues and still in progress. In this research will study and analyze the leakage components. Furthermore, proposed a new enhanced leakage power reduction technique by the combination of Sleepy stacked with LECTOR technique. This includes two leakage control transistors added between the pull up and pull down circuit .The stack effect willbe introduced throughsubstituting each existing transistor with two half sized transistors. It delivers the limitation of the area because of usage of extra transistors towards preserving the circuit state during sleep mode. Also, inserting high resistance between the supply and ground by means of CMOS switch. This technique will provide excellent leakage current reduction without any delay penalty.

**Keywords:** Power Consumption, CMOS, LECTOR, Current Reduction

## INTRODUCTION

In this modern world, due to advancement of battery-based devices with limited power capabilities needs major requirement of power efficiency and power-delay product. This two factors are of great challenge to the electronic designers[1]. Similarly, in VLSI circuit design power consumption of circuit is of major concern. The demand for low power device is not because of development of mobile application alone [3]. The problem of power consumption is major issue before the evolution of mobile era. To resolve power dissipation issue numerous techniques and methods has been proposed by researchers in terms of architetural,device level and even some higher levels. Till today there is not standard approach is evolved for factors to overcome problem of area consumption, delay and power utilization of the designed circuit. Based on the product and application requirement user need to select most appropriate technique.

In case of high performance portable devices power dissipation is the major concern. Three components plays vital role for power consumption which are all leakage current, short circuit and dissipation of power from dynamic switching [4]. In CMOS circuit total power dissipation becomes an dominant components because of continuous scaling of threshold voltage [5]. Through the recycling of stored energy in the nodes dynamic dissipation get reduced in Adiabatic computing. Even in adiabatic process dissipation of energy occurred for constant input values. However, energy dissipation occurs even for constant input signals of the adiabatic circuits where power-clocks is used for charging and discharging of output nodes [6]. Due to continuous scaling in CMOS technology in adiabatic process dissipation due to leakage in the circuit design will perform as dominant component for overall dissipation of power same as traditional logic function of the CMOS devices. In adiabatic circuit power gating approach is adopted for minimizing leakage and dynamic power of the system. In this technique at idle state power gating system shut down the units. The adiabatic circuit is significantly differing from CMOS circuit due to signal waveforms and clocking schemes in conventional approaches. In this scheme it is necessary that their need to be enough distinguish between switch with Power-gating and power clock utilized for turning-off. In adiabatic schemes various power gating are applied [6], [7]. Among the numerous gating approaches voltage scaling approach outperforms in case of adiabatic based CMOS logic circuits. In the mid performance ranges from (5MHz to 100MHz) supply voltage scaling in medium-voltage region performs effectively [8]. Based on this numerous adiabatic –circuit with near-threshold has been proposed without the use of gating power. Dueswitching power dissipation is minimized to quadratic in this scenario minimization of power consumption by the use of supply voltage technique. This techniques has the serious issues of performance degradation.Subsequently, the high performance requirements were fulfilled by scaled value of threshold voltage.But this technique has the serious drawback of increased leakage current which put forth the major concern for high performance circuit with low power utilization [9].

In this paper, proposed a new approach, thus providing a new choice to low leakage power VLSI designers. Furthermore, summarized the existing approach as well as identified the issues towards power reduction.

## RELATED WORK

In existing, most of them have suggested a different method towards control leakage power consumption. These are discussed as follows: Few of them has focused on sleep transistor approach [10]–[13]. In the sleep mode through the power cutting off sleep transistors will be turned off. Though this approach the leakage power reduced in the power source by cutting off in the circuit design. However, this results in the destruction of state plus a floating output voltage in sleep mode. Additionally, this approach reduces delay through the sleep mode sleep minimization by increasing the wake up time to maximum. In existing literatures [12], [14] sleepy stack approach is developed. Through the stack effect transistors in sleepy stats are divided in to two separate half-length transistors for the designed sleepy state design. These classified transistors are parallel connected to the one of the transistor which act as a dividend. In sleep mode/ saving state, leakage current are suppressed by stacked transistor through turning off the sleep transistor. In this technique product penalty of power delay plays significant role since where every transistor is replaced with three transistors. Sleepy stack approach is formed with the combining of transistor stacking with sleep approach for mitigating of subthreshold leakage current reduction[15], [16]. During stacking transistor is divided into two half of pull up and pull down the network which increases the resistance of circuit and sleep transistor connected paralleled which exponentially reduces the $I_{SUB}$ , main advantage of this circuit is that it maintain the proper logic of the circuit without rail out from $V_{dd}$ and main disadvantage of approach is that we cannot use high $V_{th}$ transistor for further reduction of leakage power [17].Dual sleep technique [18]uses either ON or OFF mode in the sleep mode by incorporation of two pull-ups and pull-down individually. Through which dual sleep portion can be made common for the entire circuit design where some logic circuit requires transistors in minimal count[19], In comparison with existing researches it needs increased power delay ehich may impact on increase in delay of the circuit.

## DESIGN PROCEDURE

Nowadays, the design of low power circuit has developed as the main topic in the electronics industry. subsequently, the requirement of this low power has created a noteworthy outlook change, whereas the dissipation of power is a significant factor for deliberation of area and performance. This this section presented anew leakage power reduction techniques and corresponding simulation were presented. These are discussed as follows.

### *A. Proposed method*

In this study, proposed a novel technique that reduces the power leakage of the VLSI circuit design with CMOS circuit. The new approach is sleepy stacked with LECTOR transmission approach. The circuit diagram is shown in figure.2.The proposed scheme uses aspect ratio of W/L=2 in case of PMOS circuit transistor. In other case of NMOS transistor the aspect ratio is of W/L = 1. Through the minimal aspect ratio of the circuit sub-threshold value get minimized.

In this technique, the sleep transistors are used for differentiation of ground and power supply. Other than those remaining transistor are connected to gate. It depends on input vector and controls the switching of sleep transistors, consuming power in both active and idle states. Furthermore, the two transistors are added in logic circuit based on the Pull-up and pull-down design network circuit. To cope with input combination are connected in transistor by placing any one of the transistor near the cut-off voltage. This transistor design will provides the path resistance for ground to supply connection. This resistance will provides minimized leakage current in the circuit. The designed circuit will performs effectively for the both active and standby mode of the circuit design. Furthermore, increase the resistance in the path from source to ground.

The system array is designed using transistors $V_{CC}$ and GND terminals. Such an arrangement is called as self-controlled voltage technique. It is implemented such that it reduces the amount of power consumption by allowing the transistors to swing between safe voltage values to prevent excess power consumption. As the leakage current reduces, the power dissipation across the transistors is also reduced significantly.

### *B. Layout Design*

The layout design of transistors shows the implementation of NMOS by n+ gate and diffusion layer through the incorporation of poly-silicon. Further the designed circuit interconnected with metal-1 and metal-2 for implementation. In this designed circuit read and write operation will be performed for the active word line in the circuit. The designed circuits act as open circuit when word line is not on active state..

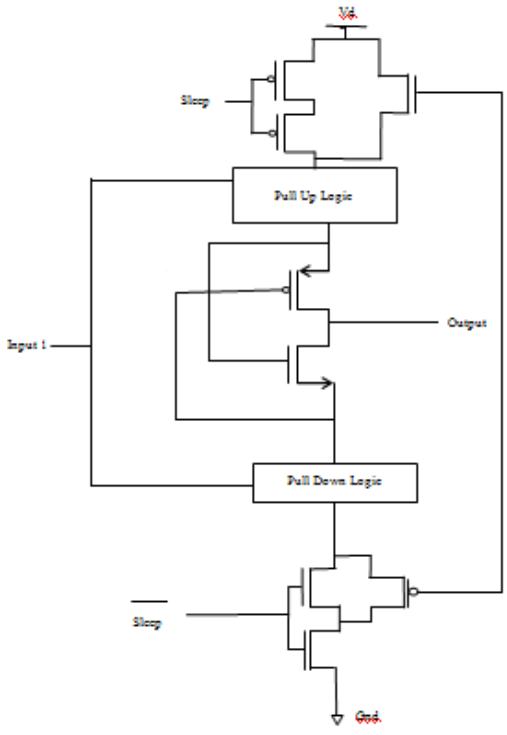


**Figure 1.** Block Diagram of proposed method

The above figure 1 illustrates proposed architecture design which contains LECTOR stack for power consumption. This

proposed approach uses a combination of Pull Up and Pull down logic design for power consumption minimization. The sleepy signal is fed in to Vcc with parallel connection with Pull Up and Pull down logic circuit were in both the transistor is provided with the sleepy signal waveform. Implementation of the proposed approach is adopted in VLSI circuit design, and corresponding performance is analyzed.

## OPERATION PRINCIPLE

The sleep signal incorporated in the design turns off the certain parts of the circuit which are not used and turned off in the simple and fast way. When the design part activated or start connecting leakage current will be minimized in huge amount which means there will not be huge leakage current. In sleep mode signal provides the critical part to identify the sleep mode signal need to be transferred without altering the other part of the design by minimizing threshold currents. In the case of active mode of the device sub-threshold, current need not be concerned since the current in the circuit design is dynamic. The proposed design is based on the considering this factors for minimizing leakage current reduction. In proposed design circuit the main concept is charge sharing and recovering of stored charges between output capacitor and capacitance nodes. In precharge phase of the proposed circuit design the charging and discharging of the node is performed by setting it at VDD/2. Further the charging and discharging is performed for the voltage ranges from VDD/2 to VDD or in the range of VDD/2 to 0 respectively for the designed circuit. The voltage power at the rate which is half the power of VDD ideally minimizes consumption of active power up to 50%. By the incorporation of scaling in the designed technology the impacts are channel length reduction, leakage current, threshold voltage, and leakage power are the dominant portion of the power in wider gates increased dramatically. Through the evaluation of designed circuit, it is clearly observed that to eliminate the sub-threshold current voltages in the source and drain need to be equal. The proposed design is developed to operate in two modes of operation like active and sleep mode.

### *A. Active mode*

For the design circuit input and output signal of the system are in the range of VDD/2 to 0 and VDD/2 to VDD respectively. In the evaluation phase of the circuit design, all nodes in the circuit design are in the range of VDD/2 for pre-charge phase, and output of the design circuit is ranges from VDD/2 to 0.In the designed network topology it provides faster NAND gate operation without considering any skew of the signal, through the utilization of domino logic function in the connected transistor in the designed pull-down network. In the proposed topology evaluation phase varies from VDD/2 to for the output voltage in the pulled down circuit from VDD/2 to 0. The output node voltage V0 in the pulled down transistor remains the voltage value of VDD/2 and vice versa.

### *B. Sleep mode*

In sleep mode, evaluation phase is disabled after the pre-charge phase of the proposed design. Every nodes proposed design all nodes have the power values are at the rate of VDD/2 in the evaluation phase. When high-level latches are located in the evaluation phase sub-threshold current may decrease drastically which is considerably small in the case of drain-source voltages.

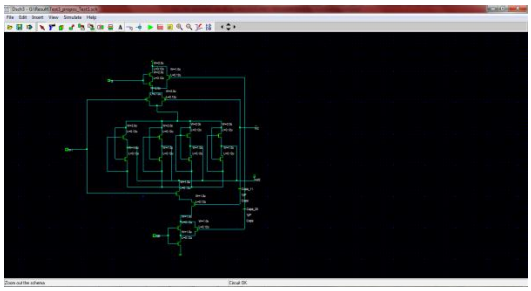

**Figure 2.** Logic diagram of proposed method

The proposed design is simulated using microwind software with various technology, and the results are depicted. This layout design contains cascade connection of proposed Sleepy stacked with LECTOR approach were implemented. In this layout design, transistor logic circuits are provided with constant input voltage supply for the both pull-up and pull-down transistors. In designed layout individual pull-up transistors are provided with 0.12V and 2.0V supply with a capacitance value of 1pF.

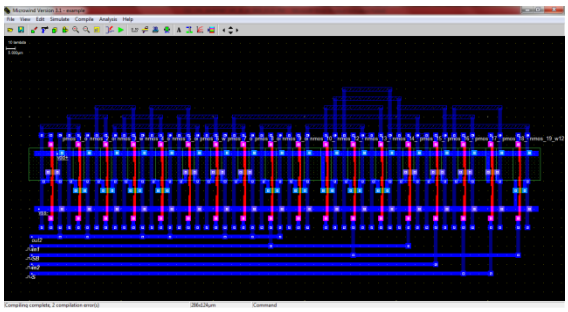

**Figure 3.** Layout design of proposed method

Layout design for proposed approach is shown in figure 3. This contains 10series connection of NMOS devices for same input power level .Further, this layout design contains 8 PMOS transistor for transmission of a signal in cascade. In layout design PMOS_15 and NMOS_9 is designed as In1 circuit for processing electrical signal and PMOS_ 16 and NMOS_10is selected as Input 2 for the developed architecture design circuit. From the output signal waveform is obtained for the feed input power supply, and the sleepy waveform is applied to the transistor.

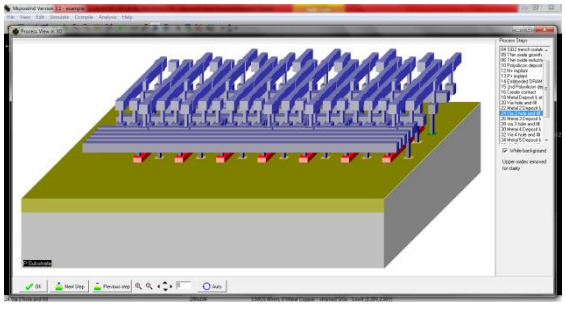

**Figure 4.** 3D view of proposed method

The design was tested with varying voltage and current levels at the inputs. To test the effect of time delay, tested the circuit at different time intervals and observed the readings. The proposed approach provides the advantage of minimized number of pins through the generation of memory in subsequent amount.

## SIMULATION RESULTS AND DISCUSSION

This section provides the description of simulations of the proposed methods are elaborated and shown in tabular form. First, make a schematic diagram (Figure.2) and create a layout diagram (Figure.3)by using the tools. Secondly, obtain the results regarding power dissipation, current, and voltage. Subsequently, two type of window is involved in this tool such as DSCH and MICROWIND where layouts are designed and the parameters are power dissipation, current and voltage at different technology. For the designed circuit Verilog file is created and schematic is created. In next stage created Verilog file is compiled in MICROWIND software for evaluating performance of the designed circuit. In other words the created schematic in the Verilog is converted and generated in MICROWIND for evaluating the simulation performance of the system in Verilog files of the designed system. The simulation is carried out for the technology of 32nm, 45nm, 65nm and 90nm. The designed circuit is incorporated with the input voltage of 1.2Vwith the designed temperature of 27˚C. For the designed input voltage and temperature the transient analysis uses 10µs. Figure 5 shows the output of proposed circuit.

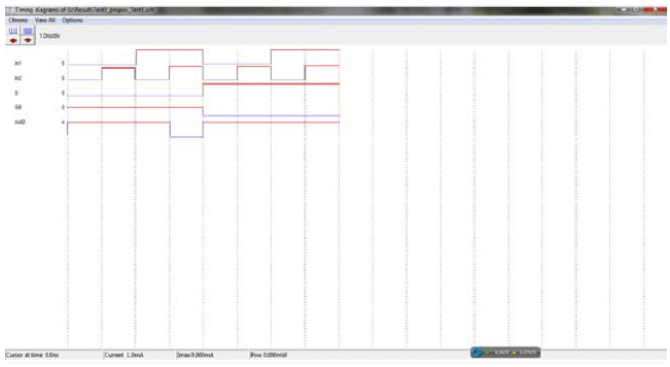

**Figure 5.** DSCH output result

**Table 1.** Simulation Data of single stage power reduction approach for NAND Gate

| Techniques | 90 nm | 65 nm | 45 nm | 32 nm |
|---|---|---|---|---|
| **Voltage** | 1.2V | 0.7V | 0.4V | 0.35V |
| **Current** | 0.012mA | 0.08mA | 0.002mA | 0.003mA |
| **Power** | 0.375µW | 0.037 µW | 0.112 µW | 0.070 µW |
| **Performance** | Good | Good | Good | Good |

**Table 2.** Simulation Data of two stage power reduction approach for NAND Gate

| Techniques | 90 nm | 65 nm | 45 nm | 32 nm |
|---|---|---|---|---|
| **Voltage** | 1.2V | 0.7V | 0.4V | 0.35V |
| **Current** | 0.3125mA | 0.94 | 0.35 | 0.257 |
| **Power** | 3.324µW | 0.661µW | 0.140 µW | 0.090 µW |
| **Performance** | Good | Good | Good | Good |

**Table 3.**Simulation Data of three stage power reduction approach for NAND Gate

| Techniques | 90 nm | 65 nm | 45 nm | 32 nm |
|---|---|---|---|---|
| **Voltage** | 1.2V | 0.7V | 0.4V | 0.35V |
| **Current** | 0.346mA | 0.2020mA | 0.1154Ma | 0.3314 |
| **Power** | 4.156µW | 0.857µW | 0.187µW | 0.116µW |
| **Performance** | Good | Good | Good | Good |

Simulation results of the single stage power reduction approach are discussed in Table 1. The comparative analysis of the simulated values provides significant performance and measured in terms of delay, maximum current and delay of the system. The designed circuit performance is implemented in Micro wind 3.1 tools in 90nm, 65nm, 45nm and 32nm technology at room temperature. Similarly, results of the two, three stage power reduction approach are discussed in Table 2 and table 3 with various technologies. In the designed single stage transistor for 90nm technology voltage level is 1.2V with power 0.375 µW and current range of 0.012mA with effective performance. In case of 32nm and technology voltage level is about 0.35V with current range 0.003mA with power value 0.070 µW with significant power characteristics performance. For the 45nm technology the voltage value of 0.4V current and power level of 0.112 µW with current 0.002mA. Similarly for 65nm technology the electrical performance of the system effective with the voltage level of 0.7V current value of 0.08mA and power is of 0.037 µW.

**Table 4.** Simulation Data of novel proposed technique for NAND Gate

| Techniques | 90 nm | 65 nm | 45 nm | 32 nm |
|---|---|---|---|---|
| **Voltage** | 1.2V | 0.7V | 0.4V | 0.35V |
| **Current** | 0.215A | 00.1254A | 0.0716A | 0.0627A |
| **Power** | 0.258µW | 0.058 µW | 0.013 µW | 0.008 µW |
| **Performance** | Good | Good | Good | Good |

Simulation results of the proposed methods are discussed in Table 4 and with various technologies. Through the comparison table it is observed that, power reduction is in considerable amount compared with conventional techniques. The advantage and disadvantages of the previous study discussed in table5. While, compared to single stage power reduction approach, the proposed power reduction approach provides improved result. Based on the above analysis, the

novel approach has offer better performance when compared to single, two and three stage power reduction approach for NAND gate.

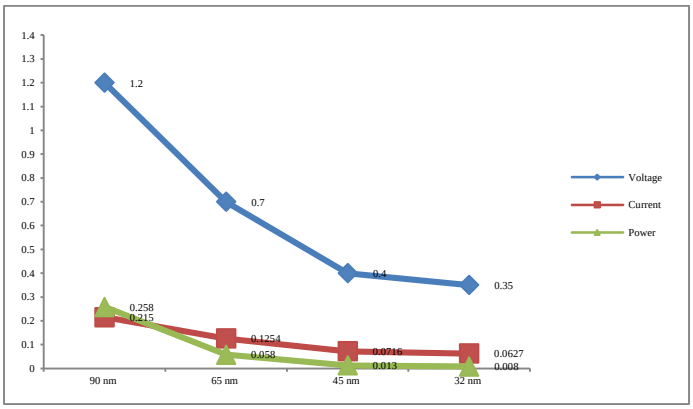


**Figure 6**. Simulated data Vs. Technology

In figure 6 comparative analyses are described for various nanometer technology in terms of voltage, current and power levels

**Table 5.**Advantages and disadvantages of previous studies

| Technique | Advantages | Disadvantages |
|---|---|---|
| Stack approach[20] | Leakage saving | transistors increase thedelay |
| sleepy stack technique(Park, Mooney & Pfeiffenberger, 2004; Park, 2005 | Less delay compared to forced stacking | Sleep transistors need control circuit, |
| Dual Threshold Transistor Stacking[21] | reduce the sub-threshold leakage while maintaining the dual $V_{th}$ | Increases propagation delay and area. |
| dual stack technique[22] | NMOS reduces the high logic level while PMOS destroys the low logic level | Power delay increases. |
| Forced stacking[3] | Easy to implement, Leakage savings. | Propagation delay increases. |
| Stacking transistors | maintain the proper logic of the circuit without rail out from $V_{dd}$ | Can't able to use high $V_{th}$ transistor for further reduction of leakage power |
| sleep, zigzag, leakage feedback approaches, sleepy keeper approach[2] | Greater Leakage power reduction | lowers performance, high $v_{th}$ applied |

In table 5 advantages and disadvantages of various power minimization techniques are described. The observation of various power minimization techniques provided in this research are stack, sleepy stack, dual threshold , stacking transistor and so on, In order to overcome the existing drawbacks in this research utilizes LECTOR based stack approach for power consumption minimization is developed.

## CONCLUSION

This research article presented a technique for effective leakage power reduction in VLSI. We have applied LECTOR stack state retention with sleepy transmission approach to the NAND gate circuit. The designed circuit is comparatively analyzed in terms of static and dynamic power performance. Further the analysis is carried out by power-delay and propagation delay of the system with existing literatures. This approach shows effective performance for both static and dynamic power conditions. This technique provides alternative options for CMOS designer for design of circuit for significant performance. As compare to 90nm technology the circuits designed in 45nm technology produce improved results in terms of minimized power consumption rate, consumption of area and delay which make it simple and efficient for VLSI hardware implementation.

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