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Design of Power Efficient Reversible Carry Skip Adder

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Abstract

Reversible computing is emerging as a promising area of technology having wide number of applications in areas of advance computing such as low power CMOS VLSI design, quantum computing, optical computing, DNA computing nanotechnology and cryptography. Reversible logic is one of the optimization methods to reduce the power dissipation which occurs due to increasing complexity of the chip when more and more devices are integrated on a single chip. With reversible logic, we are always able to reconstruct any previous computation given a description of the current state. This paper presents various designs of reversible logic gates used for reversible operations and one of the applications as carry skip adder block. This paper also proposes improved and power efficient new reversible 4*4 carry skip adder and it is demonstrated with the help of simulation results that the performance of the adder architecture designed is better not only in terms of number of transistors and garbage outputs but also power dissipation when compared to existing counterparts in literature. Simulation results reveal that the proposed carry skip adder achieves average power dissipation of 44µW which is less as compared to the existing designs.

Keywords: Low Power VLSI, Reversible logic, Carry Skip Adder, quantum ALU.

INTRODUCTION

In modern VLSI systems, power dissipation is very high due to rapid switching of internal signals and also in conventional computers, the operation carried out is irreversible i.e. once the output is generated, the input bits are lost. Thus if technology scaling continues to follow Moore's Law, the energy dissipation due to bit loss will be a major issue in future. Landauer has shown that for every bit of information lost in logic computations that are not reversible, minimum kTln2 joules of energy(heat) is dissipated, where $K=1.38060\times10^{23}$ $m^2kg^{-2}K^{-1}$(joules Kelvin[1]) is the Boltzmann's constant and T is the absolute temperature at which operation is performed[1]. In fact if a circuit is composed of only reversible gates, zero power dissipation is possible [2]. The erasure of bit done is not significant and hence a lot of power dissipation takes place which is one of the major concerns in modern CMOS technology. C.H. Bennett proposed a theoretical background about the reversible logic which proves that there is a direct relationship between the amount of heat dissipated and the number of bits erased.

Also the reversible computation is performed only when the system comprises of reversible logic gates [3].

With logical reversibility there is always a possibility to retrace each and every step and reconstruct the data which was used in previous computations. Thus with minimum energy dissipation, reversible logic circuits offers better alternative solution [4].

The most prominent application of reversible logic lies in the field of quantum computing. A quantum computer is viewed as a quantum network composed of quantum logic gates; each gate performs an elementary unitary operation such as addition, multiplication and exponentiation on one or more qubits, an elementary unit of information corresponding to the classical bit values 0 and 1[5]. This unitary operation is reversible and hence Quantum Arithmetic comprises of reversible logic components.

In this paper, the focus is on transistor realization of reversible four bit carry skip adder circuit using basic reversible gates i.e. Peres gate, Toffoli gate and Fredkin gate. The transistor realization of various basic reversible gates is also demonstrated with the help of simulation waveforms. In order to have reduced number of transistors, Toffoli gates are used for performing AND operation in the proposed reversible carry skip adder. The transistor implementation of various carry skip adder existing in literature is also demonstrated in this paper. The rest of the paper is organized as follows: Section 2 provides background on reversible logic, some qualitative parameters of basic reversible gates and their forward and backward computation. Section 3 describes the transistor realization of basic reversible gates. Section 4 illustrates about the implementation of reversible carry skip adder block using various reversible logic gates existing in literature. Section 5 describes the proposed four bit reversible carry skip adder block and it's comparisons with the existing works. Finally this paper is concluded with the section 6.

BACKGROUND ON REVERSIBLE LOGIC

A reversible function has following properties:

- The number of inputs is equal to the number of outputs.

- Unique mapping between its input and output vectors that is, for every output pattern there is an unique input pattern and input states can be easily reconstructed from the output vector states.
- Fanout is strictly prohibited in reversible logic as fanout disrupts the unique mapping between its input and output vectors.
- Feedbacks are also not allowed in order to keep the mapping intact.

Qualitative Parameters (Cost metrics)

The performance of reversible circuits is measured by a number of qualitative parameters that are defined below.

Quantum cost (QC):

This gives the number of primitive gates(1×1 or 2×2) used in the quantum logic synthesis of reversible gates. The quantum cost of 1×1 i.e. NOT gate and 2×2 gate is taken as unity [6].

Garbage Outputs (GO):

This refers to those outputs which are not primary outputs and are unused in any further computations. In other words these garbage outputs are required to restore reversibility in the circuit .Since they remain unused, they must be as low as possible [7].

Constant Inputs(CI):

These are also known as ancilla bits i.e. 0 or 1 which are used in reversible circuits for strong intermediate values during computation. Like garbage outputs, it should be minimized as far as possible, else it would be difficult to realize quantum circuits [8].

Delay:

The total time required to perform a function from any input line to any output line, the maximum number of gates in this path is considered as delay of the path [9].

FORWARD AND BACKWARD COMPUTATION OF REVERSIBLE GATES

There are several reversible gates that have been designed. Some basic reversible gates and their quantum equivalent is shown as under.

Figure 1 shows a Feynman gate[10].Feynman gate is also called as fanout gate or Copying gate since this gate is required for output duplication when the second input is '0'.The gate has a quantum cost of 1.

Forward Computation:

P=A;

If A=0 then Q=B,

Else Q=B'

Backward Computation:

A=P;

If P=0 then B=Q,

Else B=Q'

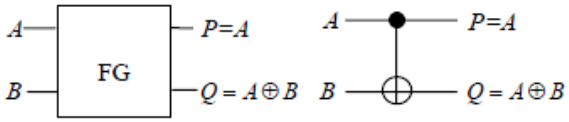

Figure 1: 2×2 Feynman Gate

Figure 2 shows a 3×3 Toffoli gate[11].It has the quantum cost of 5.From the truth table of Toffoli gate, it is clear that the output third bit is reversed as of third input bit C whenever the first two input bits (A and B) are set.

Forward Computation:

P=A; Q=B

If A AND B =0 then R=C,

Else R=C'

Backward Computation:

A=P; B=Q;

If P AND Q=0 then C=R,

Else C=R'

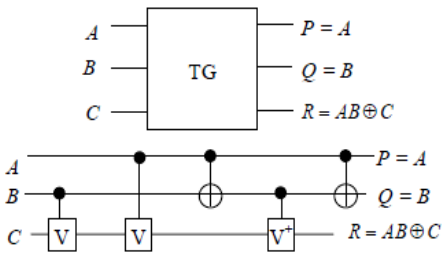

Figure 2: 3×3 Toffoli Gate

Figure 3 shows a Fredkin gate [12]. The gate has quantum cost of 5.It is also known as controlled swap gate i.e. the output bits(Q and R) are swapped as of input bits B and C whenever the first bit A is set.

Forward Computation:

P=A;

If A=0 then Q=B and R=C,

Else Q=C and R=B.

Backward Computation:

A=P;

If P=0 then B=Q and C=R,

Else C=Q and B=R.

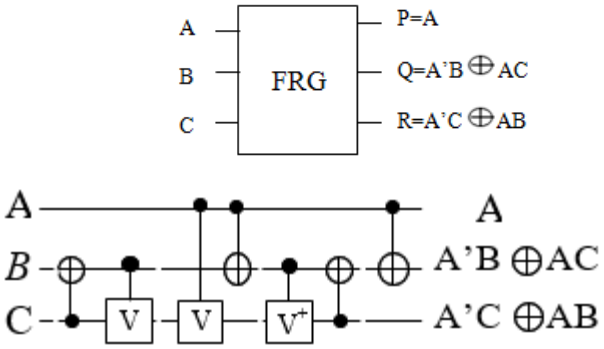

Figure 3: Fredkin Gate

Figure 4 shows a Peres gate (PG) [13] which is also known as new Toffoli gate. It is the combination of both Feynman and Toffoli gate and has the quantum cost of 4.

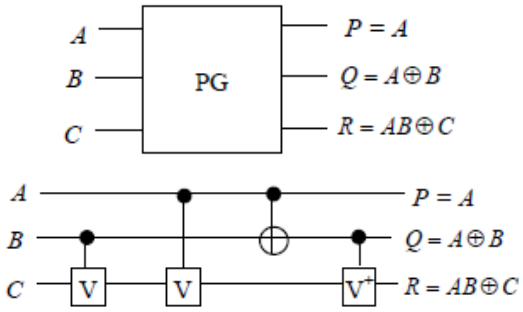

Figure 4: Peres Gate

Figure 5 shows a 4*4 TSG gate [14].This gate has the property that it can singly work as a full adder. The quantum cost of TSG gate is 13.

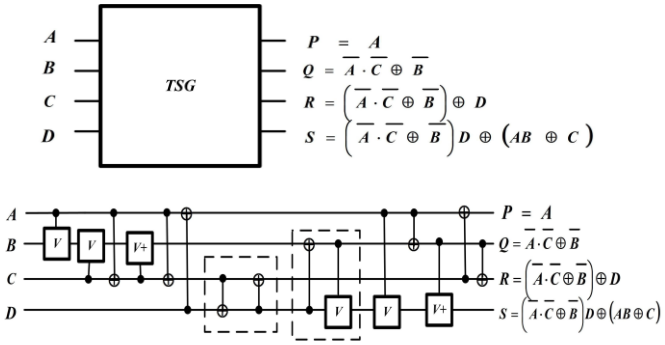

Figure 5: TSG Gate

Figure 6 shows 4*4 modified TSG gate (MTSG)[16]. The gate has the quantum cost 6 which is less than the TSG gate.

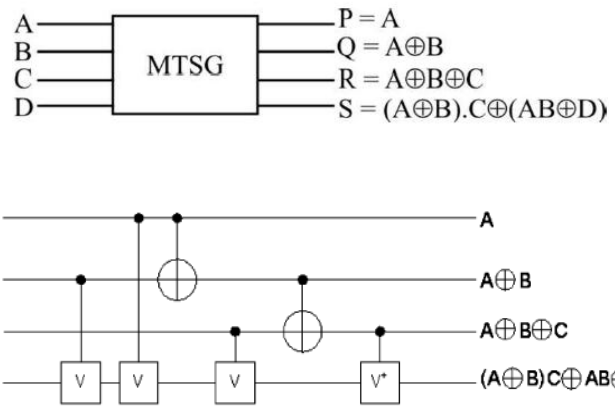

Figure 6: MTSG Gate

TRANSISTOR REALIZATION OF BASIC REVERSIBLE GATES

The transistor implementation of basic reversible gates using pass transistor logic is demonstrated as under designed in Tanner Tool v.13 250nm:

Feynman Gate

The schematic of Feynman gate is shown in figure 7 and the simulation results are shown in figure 8.

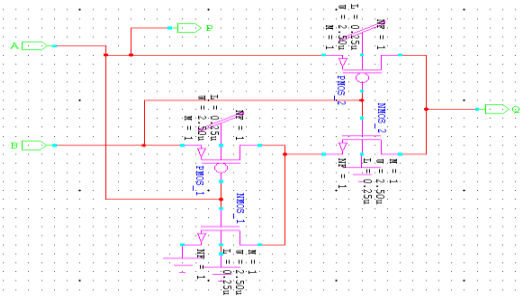

Figure 7: Schematic of Feynman gate

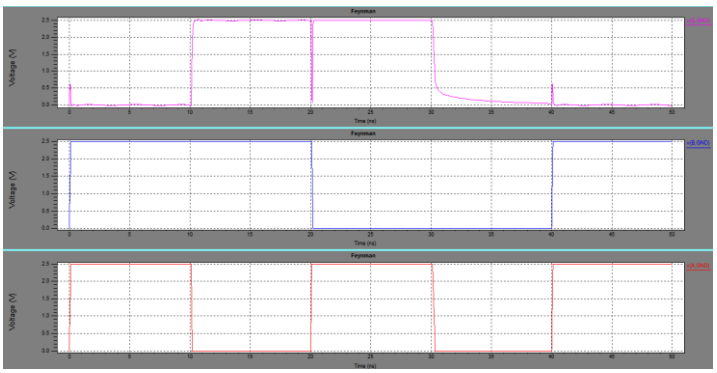

Figure 8: Simulation results of Feynman gate

Toffoli gate

The schematic of Toffoli gate is designed as shown in figure. 9 and simulation results are shown in figure 10.

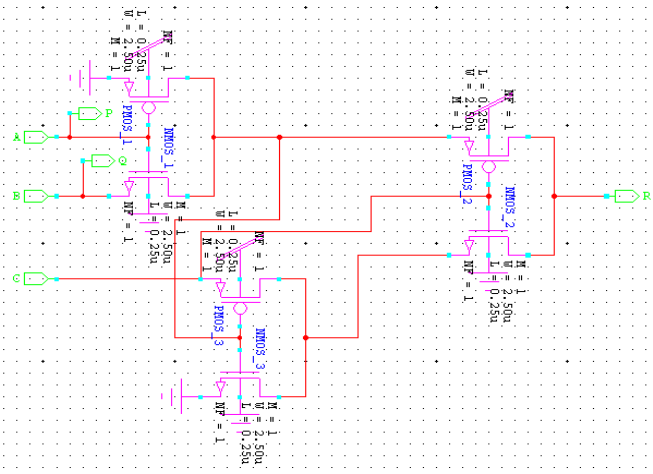

Figure 9: Schematic of Toffoli gate

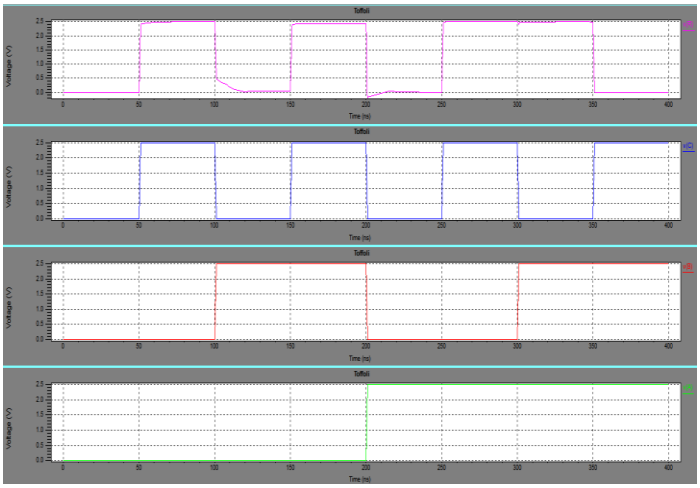

Figure 10: Simulation results of Toffoli gate

Fredkin Gate

The schematic of Fredkin gate is shown in figure 11 and the simulation results are shown in figure 12.

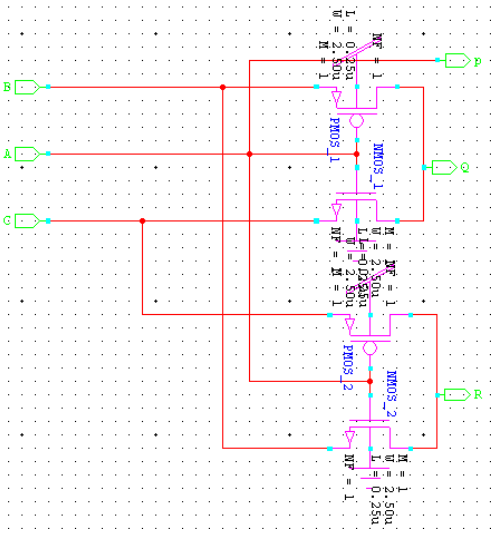

Figure 11: Schematic of Fredkin gate

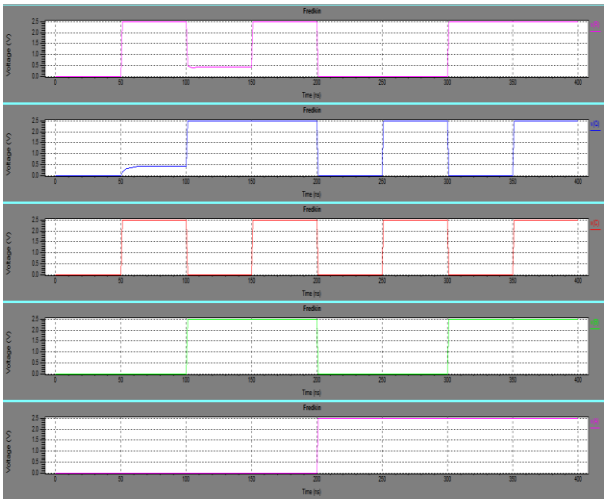

Figure 12: Simulation results of Fredkin gate

Peres Gate

The schematic of Peres gate is designed as shown in figure 13 and simulation results are shown in figure 14.

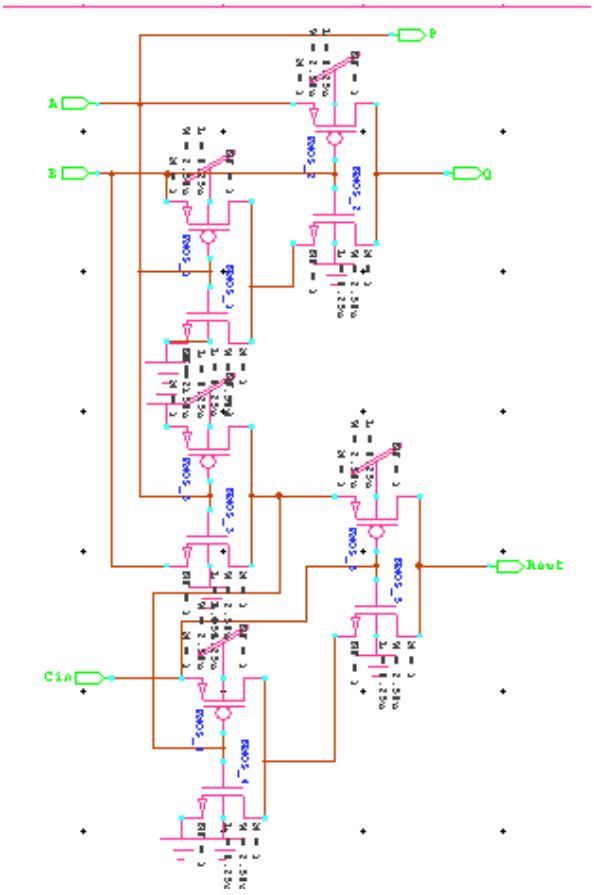

Figure 13: Schematic of Peres gate

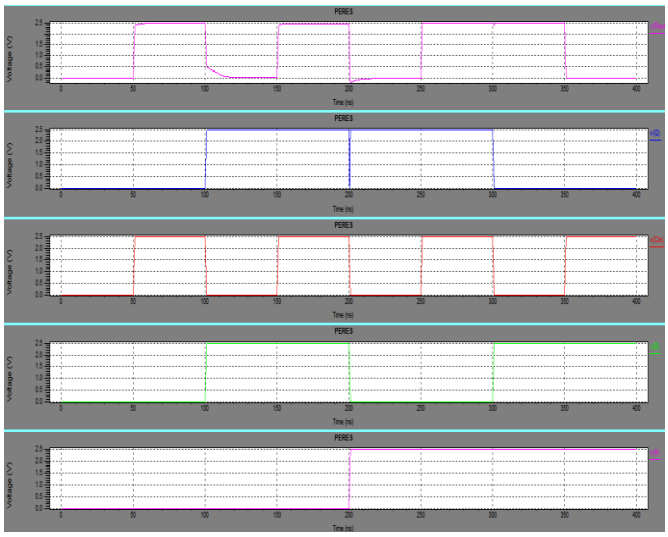

Figure 14: Simulation results of Peres gate

TSG Gate

The schematic of TSG gate is designed as shown in figure 15 and simulation results are shown in figure 16.

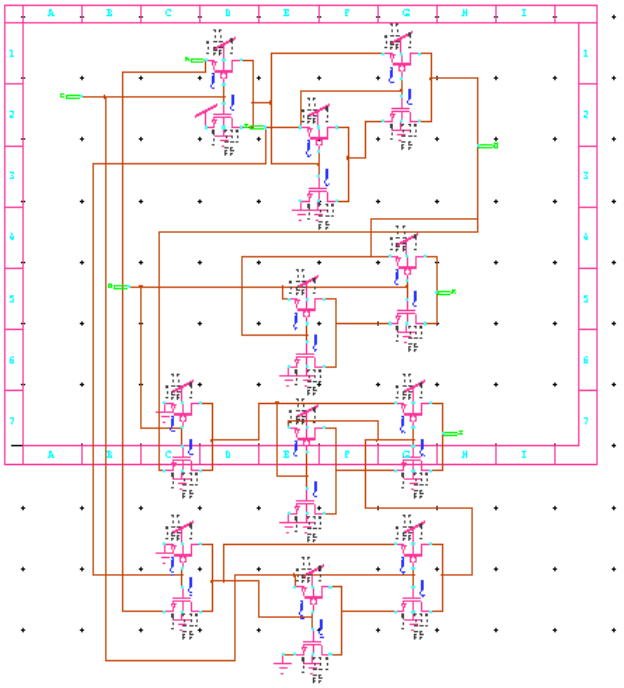

Figure 15: Schematic of TSG gate

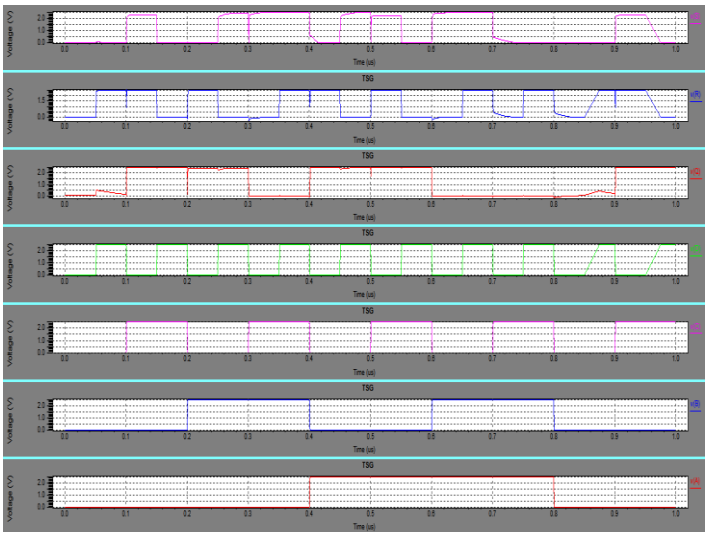

Figure 16: Simulation results of TSG gate

IMPLEMENTATION OF VARIOUS CARRY SKIP ADDER CIRCUITS

There are currently four other 4 bit reversible carry skip adder blocks in the literature and the transistor realization of these circuits are presented along with the simulation results.

Adder 1: Carry skip adder using 4 TSG, 3 Toffoli & 1 Fredkin gates

The carry skip adder block designed using 4 TSG, 3 Toffoli and 1 Fredkin gates is more optimized as three Fredkin gates

required to generate AND4 operation is replaced by Toffoli gates as Toffoli gates requires bare minimum of only three transistors to perform AND function as depicted in figure 17.

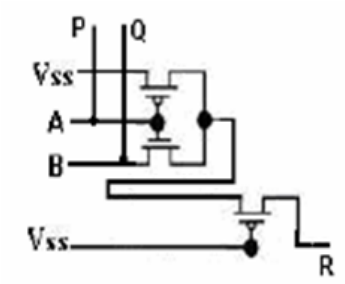

Figure 17: Transistor implementation of Toffoli gate as AND gate

The transistor implementation of the four bit carry skip adder block is shown in figure 18. The input simulation waveforms is kept same for all the designs in order to calculate the average power dissipation for all the designs. Thus input simulation waveforms is shown in figure 19(a).The output simulation results is shown in figure 19(b).

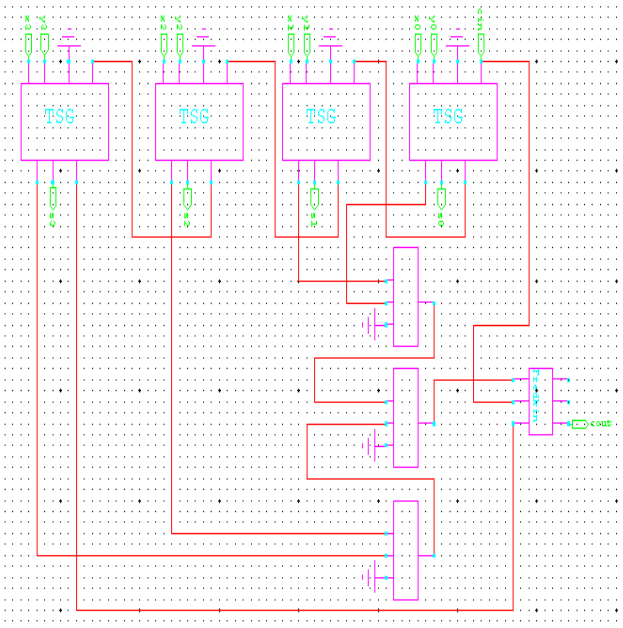

Figure 18: Transistor implementation of CSA using 4 TSG, 3 Toffoli and 1 Fredkin gates

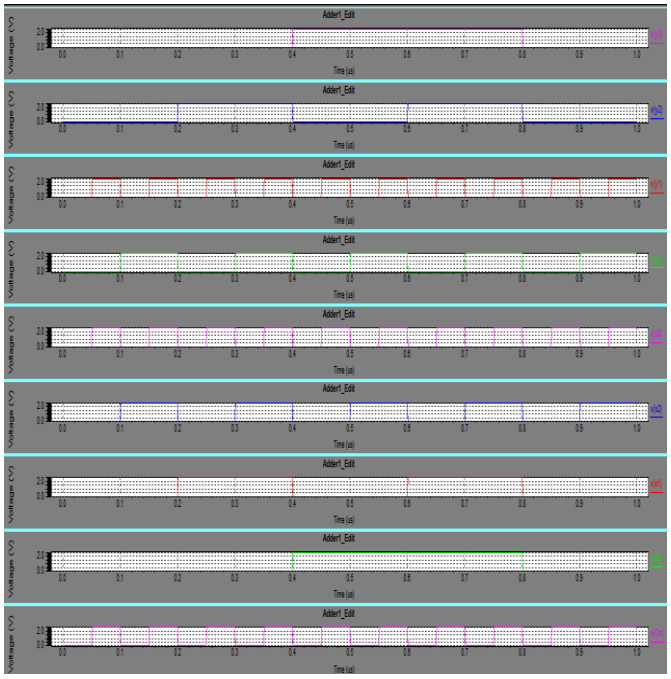

Figure 19(a): Input simulation results of Adder 1

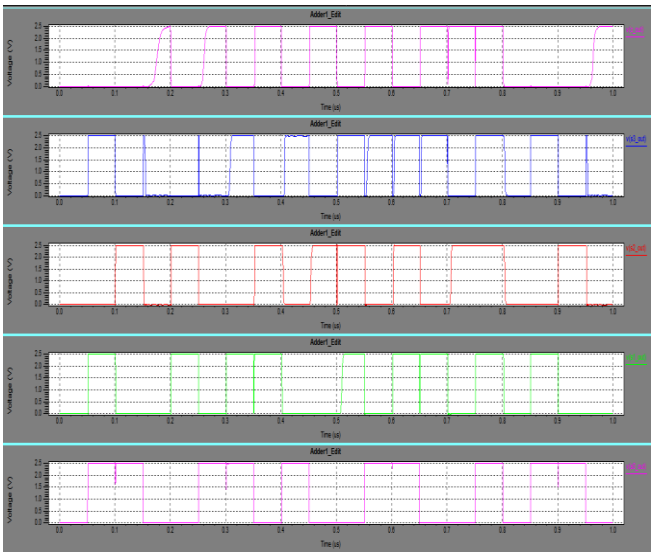

Figure 19(b): Output simulation results of Adder 1

Adder 2:Carry skip adder using 4 TSG & 4 Fredkin gates

The TSG gate, proposed by Thapliyal and Srinivas in [14] is used to design four bit reversible carry skip adder block using 4 TSG and 4 Fredkin gates. The transistor implementation of the adder block is shown in figure 20 and its input simulation results are shown in figure 19(a) and output simulation results are shown in figure 21.

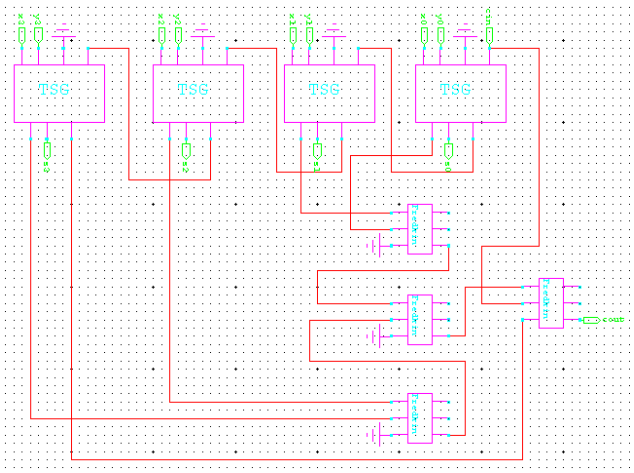

Figure 20: Transistor implementation of CSA using 4 TSG and 4 Fredkin gates

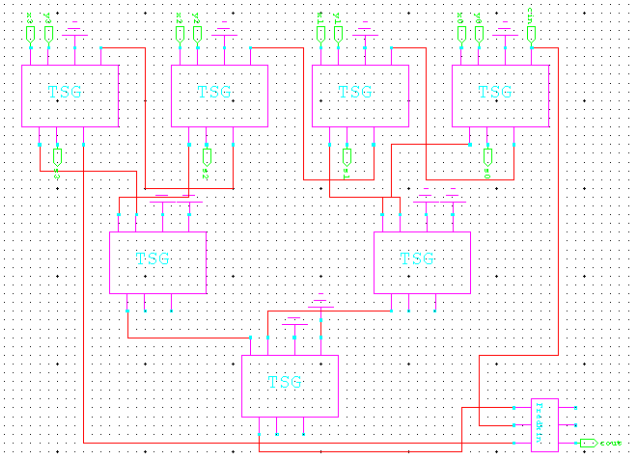

Figure 22: Transistor implementation of CSA using 7 TSG and 1 Fredkin gates

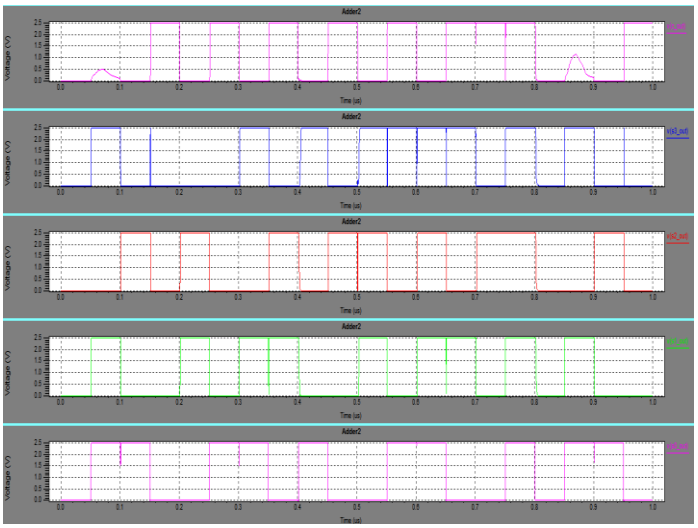

Figure 21: Output simulation results of Adder 2

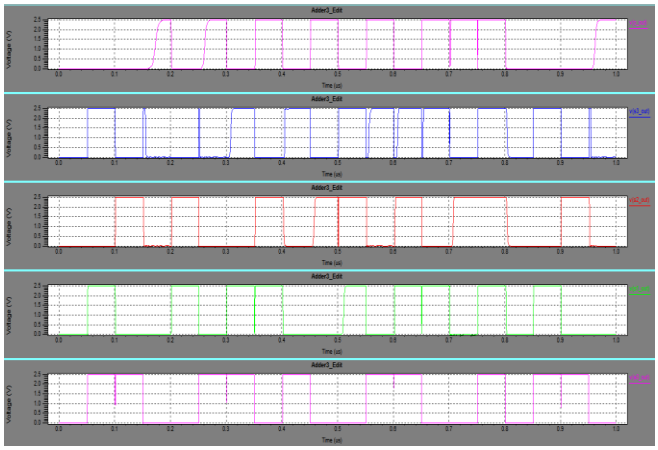

Figure 23: Output simulation results of Adder 3

Adder 3: Carry skip adder using 7 TSG & 1 Fredkin gates

The modified design of carry skip adder consists of 7 TSG and 1 Fredkin gates. The transistor implementation of reversible 4 bit carry skip adder is shown in figure 22 and its input simulation results are shown in figure 19(a) and output simulation results are shown in figure 23.

Adder 4: Carry skip adder using 4 MTSG & 3 Peres & 1 Fredkin gates

The carry skip adder block comprises of 4 MTSG gates, 3 Peres and 1 Fredkin gates. The transistor realization of MTSG gate is shown in figure 24 and its simulation results are shown in figure 25. The schematic of 4 bit reversible carry skip adder block is shown in figure 26 and its input simulation results are shown in Fig 19(a) and output simulation results are shown in figure 27.

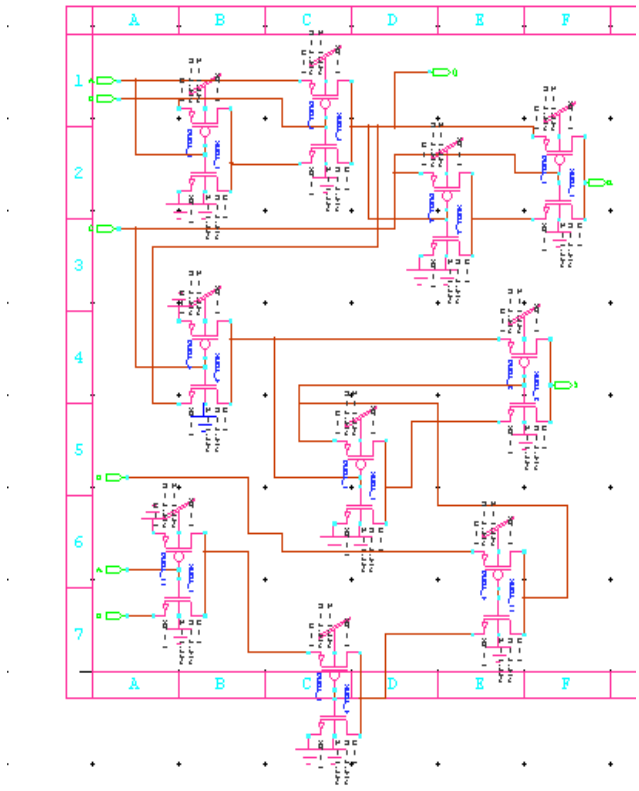

Figure 24: Transistor implementation of MTSG gate

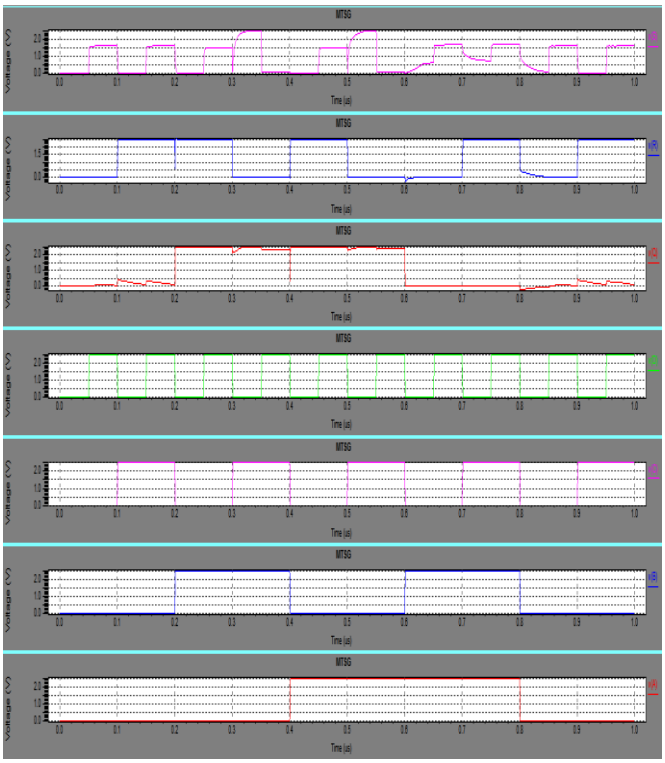

Figure 25: Simulation results of MTSG gate

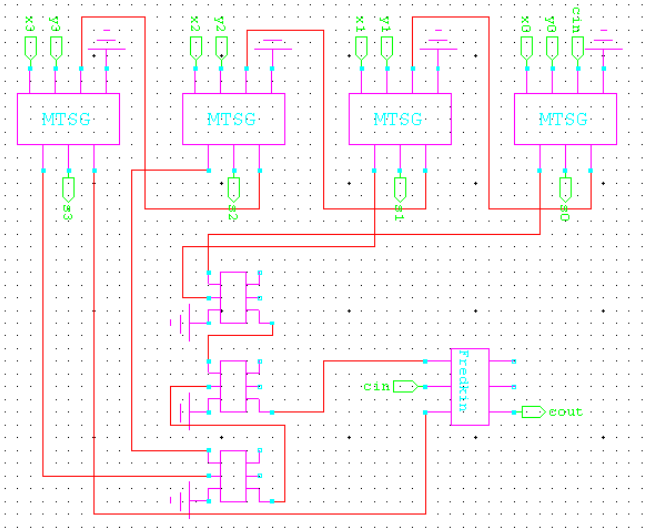

Figure 26: Transistor implementation of CSA using 4 MTSG 3 Peres and 1 Fredkin gates

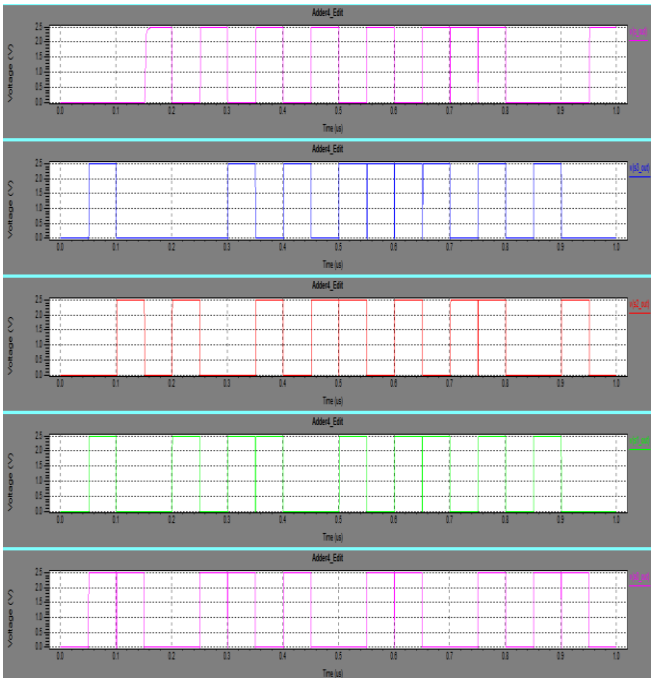

Figure 27: Output simulation results of Adder 4

PROPOSED DESIGN OF FOUR BIT CARRY SKIP ADDER BLOCK

The Peres gate is used to implement the full adder block as shown in figure 28. Peres gate is used basically because the transistor implementation of Peres gate uses 10 transistors and this full adder block consists of 17 transistors.

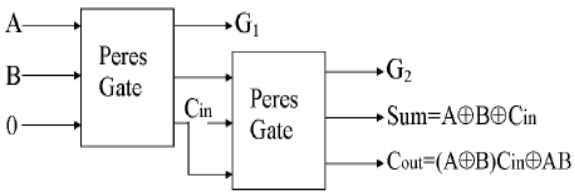

Figure 28: Block diagram of reversible full adder

There are several types of adders used in the computing systems and the most common among them is ripple carry adder in which full adders are connected in series and carry is propagated through all the stages and hence requires more carry propagation time to generate carry output [15].Carry look ahead adders are fastest among all the adders since carry output is generated in parallel computation but requires a large number of gates. The conventional block diagram of carry skip adder is shown in figure 29, is the most promising adder which presents hardware and performance compromise between both the above adders. In the full adder operation, if either of the input is logical one, then the block will propagate the carry input to carry output. Hence the ith full adder carry input C_i, will propagate to its carry output, C_{i+1}, when $P_i=X_i \oplus Y_i$ [17].

In the proposed carry skip adder in figure 30, 4 bit parallel addition is done using two peres full adder block. The block propagate signal P is generated using three toffoli gates, where $P= p_0.p_1.p_2.p_3$ and $p_0= X_0 \oplus Y_0$, $p_1= X_1 \oplus Y_1$, $p_2= X_2 \oplus Y_2$ and $p_3= X_3 \oplus Y_3$ [18].The toffoli gates are used for generating the AND function as this will reduce the computational complexity of the circuit in terms of transistor implementation without affecting the garbage as the ANDing operation using toffoli gates requires only three transistors when it's third input bit is 0 as shown in the figure 17.

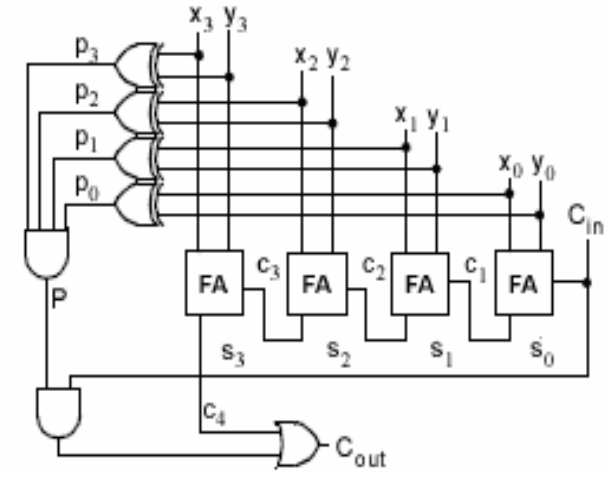

Figure 29: Four bit carry skip adder block [17]

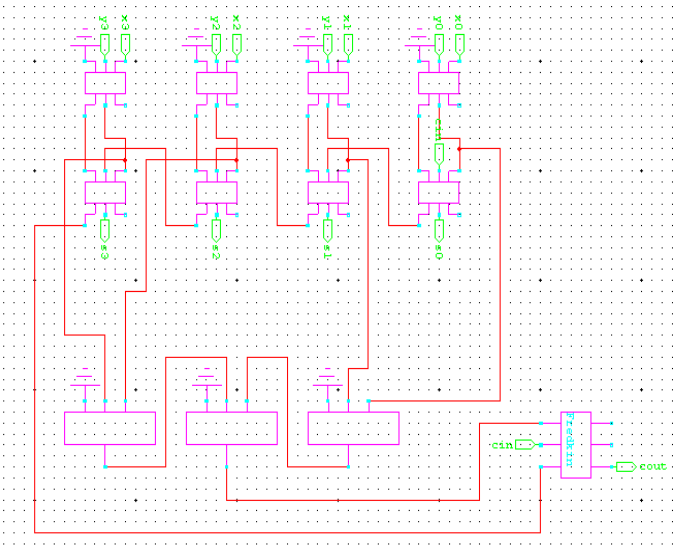

Figure 30: Four bit carry skip adder using Peres gates,Toffoli gates and Fredkin gate

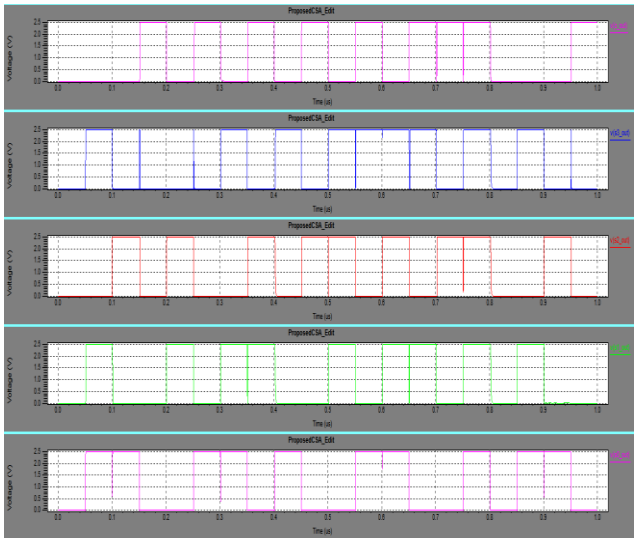

Figure 31: Output Simulation Results of Four bit Carry Skip Adder block using Peres, Toffoli and Fredkin gates

Proposed carry skip adder block constructed with 8 peres gates, 3 Toffoli gates and 1 Fredkin gate. Here the Peres full adder block consists of 2 Peres gates and thus 8 Peres gates are required to generate different propagate signal and three Toffoli gates are used for generating the AND operation,which was required to generate block propagate P signal. Fredkin gate is used to generate an AND and OR operation to generate Cout [18]. The input simulation results are shown in figure 19(a) that is the input bits X_0, X1, X2, X3, Y0, Y1, Y2, Y3 and Cin Output simulation results of four bit Carry Skip Adder block is shown in figure 31. The output bits shown are S_0, S1, S2, and S3 along with the carry output Cout. The table below shows the summary of all four existing designs of four bit carry skip adder compared with the proposed design.

Table 1: Comparative Result of Different Four bit Carry Skip Adder Circuit

Adder designs	Number of gates used	Number of garbage outputs	Number of constant inputs	Number of transistors	Average Power dissipation(μW)
Proposed Circuit	12	12	7	81	44
Ref. [17]	8	12	7	85	54
Ref. [19]	8	12	7	88	119
Ref. [18]	8	15	10	91	104
Ref. [16]	8	12	7	85	81.54

CONCLUSION

The focus of this paper is on transistor implementation of reversible four bit carry skip adder using basic reversible gates Peres gates, Toffoli gates and Fredkin gate. The simulation tool used is Tanner Tool version.13 for 250nm technology. To analyze the performance of proposed design, existing carry skip adder circuits are also implemented using various reversible logic gates. It is proved that the proposed adder architecture is better than existing designs in terms of number of transistors, garbage outputs and average power dissipation. The proposed design find its use in reversible processor, reversible ALU, etc. Also this work plays a significant role in quantum computers where more complex reversible sequential circuits are designed so as to minimize the power consumptions and build more improved applications.

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