A Part Hardware Implementation of Hydraulic Energy Conversion System Chain in Low Power Controlled by DSP F2812

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Abstract

The laboratory hardware prototype implementation part of the hydraulic energy conversion system chain has been operated in low power and controlled by DSP F2812. The part of chain includes an uncontrolled AC-DC three phase rectifier followed by a controlled DC-DC boost converter connected to a resistive load. The control strategy algorithm of this system results in two regulation loops one of them for the DC output capacitor voltage and the other for the dc input inductor current. This strategy was developed on Matlab-Simulink and implemented in eZdsp TMS320F2812 DSP board from Spectrum Digital. The Real Time Workshop platform can link between the control strategy and the realized hardware prototype, which generate the logic pulses to the IGBT switch of the boost converter. The simulation and experimental results confirm the effectiveness and powerful of the hardware and software implementation.

Keywords: DC/DC Boost Converter, DSP F2812, Hardware Prototype Implementation, Matlab-Simulink, Three Phase Uncontrolled Rectifier.

INTRODUCTION

Renewable energies have occurred recently a very important development due to their inexhaustible potential and positive impact on the environment. The study of the renewable energy conversion chain is a basic element to improve the quality of green energy production. Power converters are a fairly important part of the conversion chain [1], [2]. The last can be separated in two parts: the generator side converter and the grid or load side converter. The generator side converter is principally objective study of this work.

The choice of the uncontrolled three phase rectifier AC-DC plus boost converter for the primary side is more interested because it contributes to increase the reliability, the economical conveniences [3] and reduce the higher complexity of the control system. The DC-DC boost converter suitably converts the unregulated DC input voltage coming from the uncontrolled rectifier into a regulated DC output voltage.

It uses solid state devices like transistors and diodes to work as a switch. Energy storage components, containing capacitors and inductors, are used for energy transfer and work at the same time as a low-pass filter [4].

The control algorithm methodology for DC-DC boost converter can be traditionally implemented in an analog way.

However, the change in controller gains or algorithms can only be made by hardware adjustment which produces a fixed, non-flexible and uneconomical realization [5]. Whereas the digital controller is a good solution to these problems, since it can be implemented by digital signal processing (DSP) which has many advantages over analog controller [6], [7], like the programmability in real-time, flexibility and facility to implement complicated control algorithms and so forth. In this study, the aim is to develop a laboratory prototype to validate and prove the performance effectiveness of a hydraulic conversion chain part operated in low power. In order to implement this, we have started in this work with the implementation and experimental test of the three-phase uncontrolled rectifier plus the controlled boost converter. All signal sensors as voltage and current necessary for our strategy command executed by eZdsp DSP board are collected using the realized measurement boards. Our perspective is to test the realized cards with a higher power (1.5KW) where a synchronous generator supplies the system for be adjoin into the other experiment part of inverter/load in order to build a complete conversion chain [8] prototype for the experiment in the laboratory.

HARDWARE IMPLEMENTATION CIRCUIT

The full system of our laboratory test prototype is illustrated in Fig. 1. It consists of two parts: the hardware power part and control part. The first one includes an AC three phase input source feeds an uncontrolled three phase rectifier followed by a controlled boost converter connected to a resistive load. The second one contains a DSP F2812 control board communicated to a computer with necessary software (Matlab-Simulink and Code Composer Studio CCS). The both cited parts need an intermediate interface consists of an IGBT driver module isolated with opto-coupler, sensors circuits with current and voltage transducers for the measuring and adapting signals.
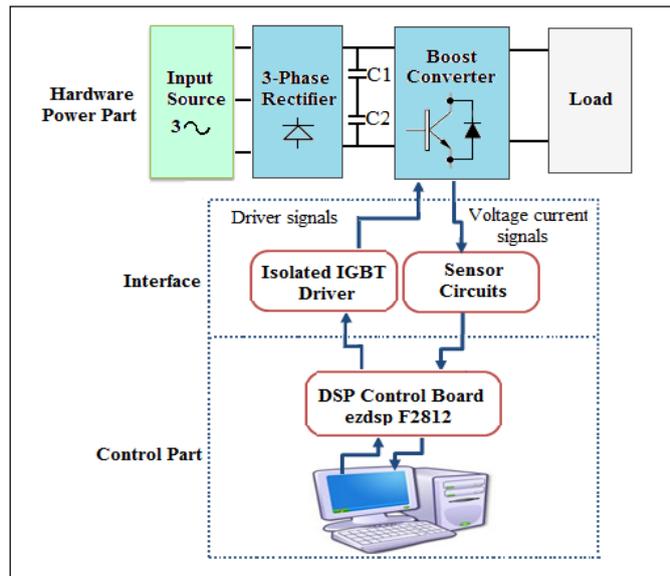
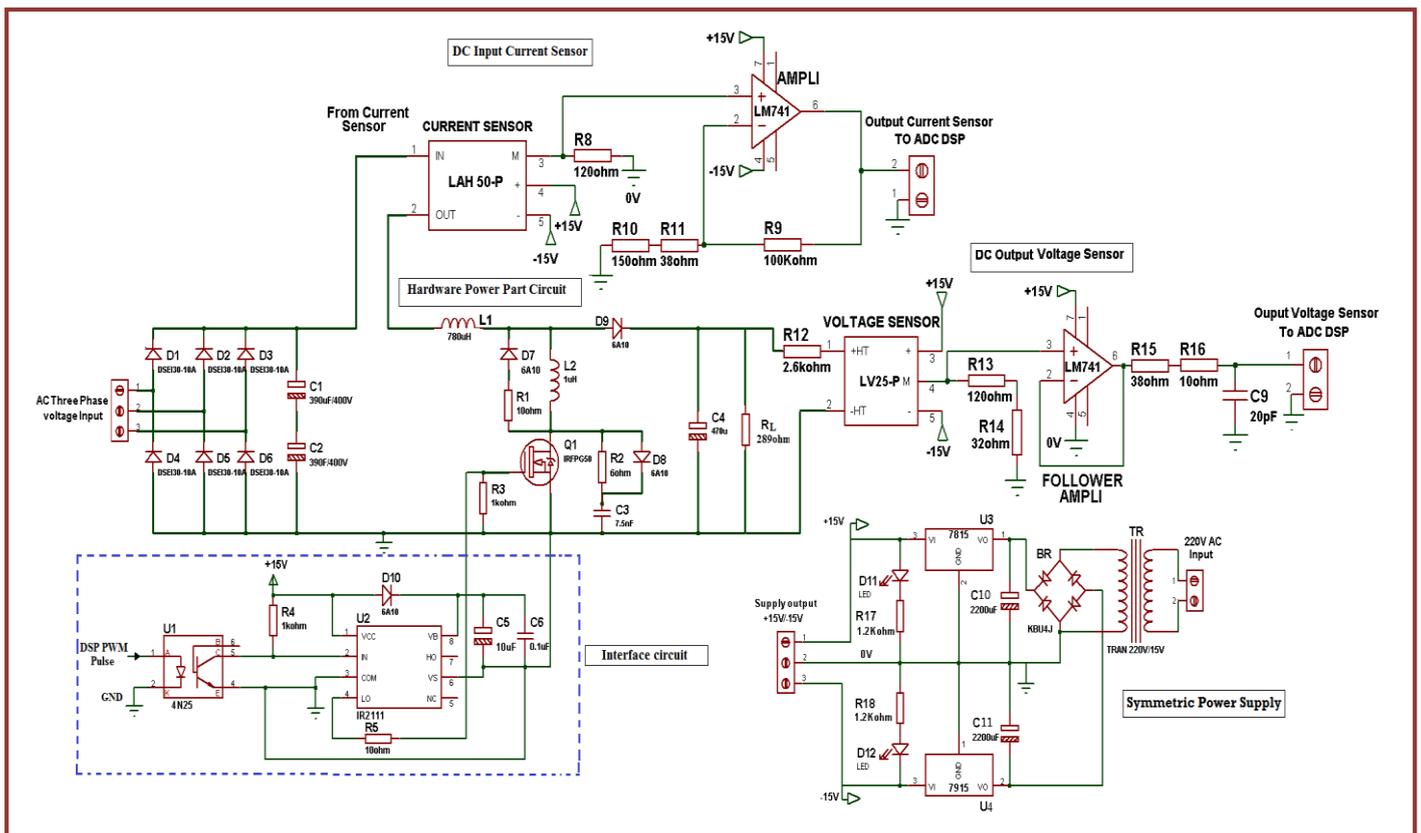**Figure 1:** Hardware System full scheme

Figure 2: Prototype test scheme of the hardware power part with its intermediate interface control

The output of three phase rectifier is an unregulated DC voltage because it fluctuates with the change of potential power in line. The dc load output voltage and dc input inductor current will be regulated by varying the DC/DC converter switch using a generated C language program by Matlab in the CCS which has the rule of executing and loading this program into the DSP.

Along with this system, IGBT driver circuit is used for amplifying the DSP output signals from 3.5 V to the value around 15V triggering levels. The hardware power part and control part are isolated with the help of opto-couplers. The schematic diagram for hardware power part and control part

circuits with their intermediate interface is shown in Fig. 2.

HARDWARE POWER PART CIRCUIT

Uncontrolled Three Phase Rectifier Power Circuit

The uncontrolled rectifier is the simplest, cheap, and rugged topology used in power electronic applications. It converts alternating current (AC) to direct current (DC), which cannot work in bi-directional power flow but in our case it's not needed. It is assumed that the AC power generated from the generator is converted into DC power through diode bridge rectifier circuits [8], [9]. The mean value of DC voltage and current of the three phase diode rectifier (see Fig. 3) are as follow:

$$V_{dc} = \frac{3\sqrt{2}}{\pi} * V_{LL} \; ; \; i_{dc} = \frac{\pi}{\sqrt{6}} * i_g \qquad (1)$$

Where: $\quad i_g = i_{nom} = \frac{S_{nom}}{\sqrt{3} * V_{nom}}$

With: (V_{dc}, i_{dc}) are the DC outputs voltage and current of rectifier respectively; (V_{LL}) is the RMS value of generator phase-phase voltage; (i_g) is the generator current; (S_{nom}) is apparent power and (V_{nom}, i_{nom}) are the AC nominal voltage and current.

The selected diode for the uncontrolled three phase rectifier power circuit is a DSEI 30-10A from IXYS Fast Recovery Epitaxial Diode (FRED), supporting 1000V at its terminals and a current of 30A [10].
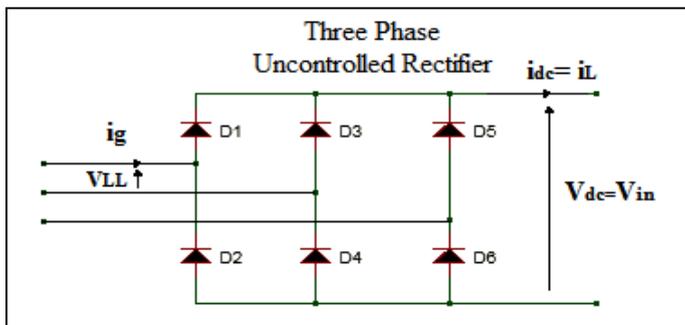

Figure 3: Three-phase uncontrolled rectifier circuit

Boost Converter Power Circuit

Inductance and capacitor design: The boost primary side is connected to the rectifier with an inductance L_1 and its secondary side is connected to the load via a capacitor C_4 as shown in Fig. 2. The both parameters L_1 and C_4 should well designed in order to the output voltage ripples should be too low even if the ripples input current could be high. Therefore, the parameters values of L_1 and C_4 for a desired outputs voltage and current ripples are as follow [8], [11]:

$$L_1 \geq \frac{V_{in}(1-d)}{f_{sw}\Delta I_{in}} \; ; C4 \geq \frac{I_{out}(1-d)}{f_{sw}\Delta V_{out}} \qquad (2)$$

Where: (ΔI_{in}, ΔV_{out}) are voltage and current ripples respectively with: $\frac{\Delta V_{out}}{V_{out}} \leq 5\%$ and $\frac{\Delta I_{in}}{I_{in}} \leq 10\%$; ($V_{out}$, I_{in}) are output voltage and input current respectively; d =duty cycle; f_{sw} = switching frequency of the converter.

Transistor design: The transistor must be able to support a voltage and current (V_K; I_K) equal respectively to: [12]

$$V_K = V_{in} + V_{out} \; ; \; I_K = I_{out} * \sqrt{\frac{(V_{out} + V_{in\_min} + V_D)*(V_{out} + V_D)}{V^2_{in\_min}}} \qquad (3)$$

The transistor choice is an IRGPS60B120KD of the International IOR Rectifier supporting 1200V at its terminals and a current passing capability of 45A [13].

This IGBT transistor is very sensitive to sudden changes in voltage and current those occur during switching. Two switching assistance circuits (CALC or snubber) can be integrated at the closing/opening state.

Closing state: the series CALC circuit imposes that the growth of current occurs after the voltage be in zero state. The inductance L_2 in series with the switch makes this possible because it slow down the growth of the current while the voltage drops. This inductance cannot be introduced alone; this would amount to opening a current source. The energy stored in the opening state must be evacuated by using a resistor R_1 and a Flyback diode (6A10) [14], which impose the direction of the current (Fig. 4). The designing of the series CALC circuit at the closing state introduces two constraints: [15]

- Imposed overvoltage on the switch equal to $\frac{R_1}{I_K}$

-CALC initialization is made before the next closing switch:

$$t_1 = 3\frac{L_2}{R_1} \text{ with } L_2 = \frac{V_K * t_r}{I_K} \qquad (4)$$

Where: t_1 is the initialization or discharge time of the inductor L_2; t_r is rise time of the IGBT switch; (V_K; I_K) are the voltage and current can support the IGBT switch; (R_1; L_2) are the resistance and inductor respectively of CALC at closing state.

Opening state: the parallel CALC circuit slows down the evolution of the voltage at the switch terminals. A capacitor is placed in parallel on the switch, charging through the diode thus limiting the growth of the voltage and deriving a part of the current. The resistance limits the discharge of the capacitor in the switch at the next closing as shown in Fig. 5. The parallel CALC circuit, likes the previous one, introduces two constraints: [15]

- Imposed over current on the switch equal to $\frac{V_K}{R_2}$;

- Switch must remain closed as long as the capacitor

discharges: $t_2 = 3R_2 * C_3$ with $C_3 = \frac{4}{9} * \frac{I_K * t_f}{2 * V_K}$ (5)

Where: t_2 is the discharge time of CALC capacitor C_3; t_f is the fall time of IGBT switch; $(R_2; C_3)$ are the resistance and capacitor respectively of CALC.
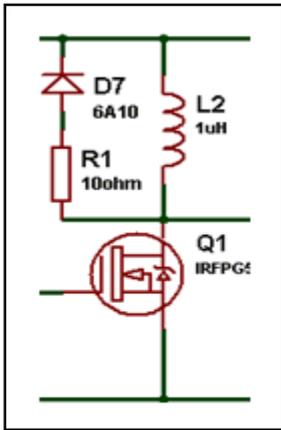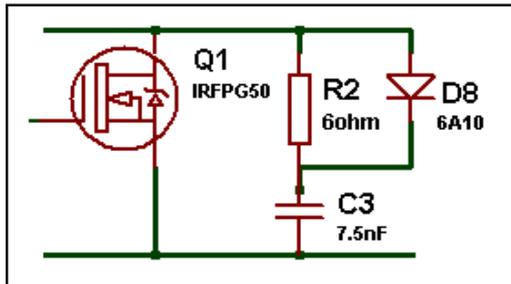

Figure 4: CALC at closing

Figure 5: CALC at opening

INTERMEDIATE INTERFACE CIRCUIT

Isolated IGBT Driver

IGBT is a voltage controlled device from its gate; require a minimum gate threshold voltage of about 15V for generating the collector-emitter conduction. Voltage and current values of the DSP output signals are not enough for operating of IGBT. So, IGBT driver IR2111 is used for amplifying the DSP output signals from 3.5 V to the value around 15V triggering levels [16]. Besides to this, In order to isolate the control part circuit to hardware power part circuit, we used an opto-coupler of 4N25 type [17]. The schematic circuit diagram for the IGBT driver and opto-coupler circuit is shown in Fig. 2.

Measurement Sensor Circuits

The measurement cards consist of hall-effect sensors which are required for voltage and current measurement are describing in below.

Voltage Transducer: The DC output voltage of boost converter is measured by using LEM LV25-P voltage transducer [18]. The card is adjusted to read 24Vrms and convert it into 3Vrms. the transducer delivers a current from the secondary side 2.5 times greater than the primary current flows through it. The rated primary current is 10mA, in the case of LV25-400 the peak value of measured voltage is 400V. To limit the primary current to 10mA where the applied voltage is 24V, a 2.6KΩ resistor is used to reduce the primary current to the desired level. The transducer card used in the study is shown in Fig. 6.

It has five pins, two on the power side ±HT and three others on the voltage drop side which allows the connection of the sensor with a polarized power supply and the measurement recovery. The voltage sensor LV25-P must be connected to a resistor R_{13} in series to the measuring terminal and finally a polarized power supply (±15V) connect to both power supply terminals as shown in Fig. 6.
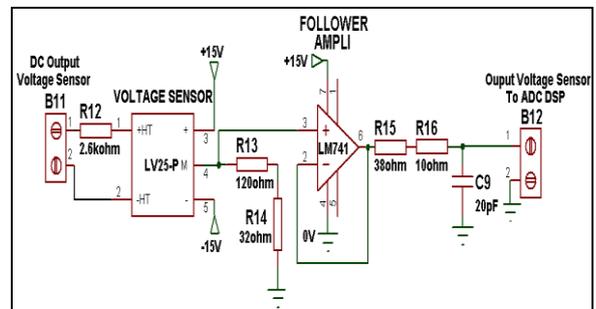

Figure 6: Card implementation of voltage sensor LV25-P

The upper and lower limits of resistor R_{13} were stated on the LV25-P datasheet as 100Ω min. and 190Ω max (for ±15V supply). In order to obtain a voltage output that used a reasonable amount of the 3V output resolution at normal operation, the upper most common value of 120Ω was used. The voltage output of the transducer at 24VDC was therefore:

$$V_{out} = \frac{V_{in}}{R_{in}} * conversion\_ratio * R_{13} = 3V \qquad (6)$$

It is a good practice to use a follower amplifier (op-amp) as driver circuit for signal conditioning of DSP input analog signals as shown in Fig. 6. The follower op-amp isolates the ADC and provides low/stable output impedance. The external resistors (R_{15}, R_{16}) isolate the ADC from the amplifier; however, during sampling, C_9 acts as a reservoir and helps in signal stability. The optimum capacitor value is 20–30pF and the resistor value is selected to meet the speed or bandwidth requirement; but it should not typically exceed 50Ω.

Current Transducer: The current transducer is a sensor which produces a voltage image of the measured current. The current to be measured passes through the sensor and produces a magnetic field which is responsible for the occurrence of the voltage V_h (Hall voltage). This voltage is almost proportional to the magnetic field and therefore it is proportional to the actual current. Similar to the voltage transducer, the

measurement resistor value R_8 for the current transducer was selected to give good use of the output range and be under the 3V limit at normal operation. This was checked using the following formula:

$$V_{out} = I_{pri} * no.of.primary turn conversion ratio * R_8 \qquad (7)$$

The upper limit of measurement resistor R_8 was stated on the LA50-P datasheet as 120Ω max [19]. Therefore, the output of the LAH50-P is loaded with a measuring resistor of 120 Ω. This output voltage proportional to the measured input current is not under the 3V DSP range input. For this purpose a non-inverting operational amplifier LM741 was implemented in the same card of current sensor LAH50-P to meet into DSP range operation as shown in Fig. 7.
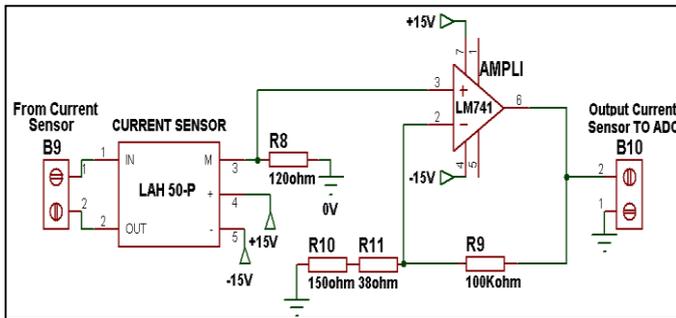

Figure 7: Card implementation of current sensor LAH50-P

CONTROL PART CIRCUIT

In our experiment, we used an eZdsp F2812 stand-alone DSP board as a hardware platform for our DSP controller. The TMS320F2812 is a 32-bit fixed point DSP controller with on-board flash memory [20]. The CPU operates at 150MHz. The C28x DSP generation is efficient in executing C and C++ language code built on Code Composer Studio tools, hence enabling control algorithms to be developed in high level languages. The F2812 supports the peripherals used for embedded control and communication, such as an event manager module for pulse-width-modulation (PWM) and a dual 12-bit, 16-channel analog-to-digital converter (ADC). In below, brief description of the used modules in our control strategy:

Pulse-Width-Modulation (PWM) Module

In this application, the event manager module (EVB) and General Purpose Timer of the DSP were used to generate asymmetric (up) PWM wave [21]. In order to set the timer period to desired frequency 10 kHz, the timer period value must be calculated as follows:

$$Time\_period = int32\left(\frac{sysclkout}{2*TPS*PWM\_freq}\right) \qquad (8)$$

Where:

- *SYSCLKOUT* is the CPU clock frequency (150MHz for the TMS320F2812 DSP);

- *TPS is the time Prescaler.*

Analog-to-Digital Converter Module

The Analog-to-Digital Converter (ADC) module is a dual 12-bit, 16-channel ADC [22]. The 12-bit ADC has a built-in sample-and-hold circuit. The 16 channels provide multiplexed inputs to the ADC, as there is only one converter in the ADC module. Each conversion can be programmed to select any 1 of 16 input channels. The conversion time is 200 ns for a single conversion and 60 ns for pipelined conversions. The analog voltage input is limited from 0 to 3 V. The digital value of the ADC can be calculated by the following equation, where ADCLO is the ground reference value for ADC.

$$Digital\_value = 4095*\left(\frac{Input\_Analog.voltage\_ADCLO}{3}\right) \qquad (9)$$

CONTROL STRATEGY METHOD

The control of the DC-DC boost converter consists of two cascaded inner and outer loops. The outer loop is related at the dc voltage output control where it should measure the dc converter output voltage and regulated at its reference. The loop output provides the dc current reference necessary to the inner control loop. The last is based on the dc inductor current input control where this time it should measure the dc inductor current input of boost converter and compare it with its reference value. The error between them is used to vary the duty cycle of boost converter to regulate the rectifier current output. Therefore, the output voltage of the DC-DC converter switch is regulated to be within a specified range in response to changes in the input voltage and the load current. The Fig. 8 shows the strategy control method scheme of the DC-DC boost converter.
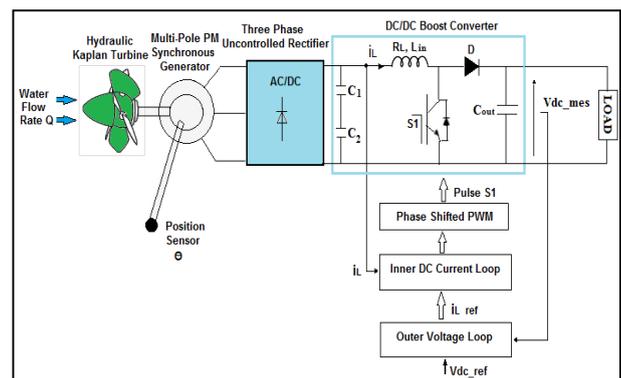

Figure 8: Strategy control method of the DC-DC boost converter

Frequency response method was used in the design of voltage mode controllers for DC-DC converter.

Small signal model of the converter was first obtained by linearizing the power stage of the boost converter around an

operating point [8]. In digital control, the control algorithm is implemented on DSP.

The boost converter small signal input current $\hat{i}_L(s)$ to output voltage $\hat{v}_{out}(s)$ and control $\hat{d}(s)$ to input current $\hat{i}_L(s)$ transfer functions, derived by the standard state-space averaging technique [8], are given respectively as follow.

$$H_C(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{C_{out}V_{out}s + (1-D)I_L}{L_{in}C_{out}s^2 + RC_{out}s + (1-D)^2} \qquad (10)$$

$$H_V(s) = \frac{\hat{V}_{out}(s)}{\hat{i}_L(s)} = \frac{(1-D)}{C_{out}s + \frac{1}{R}} \qquad (11)$$

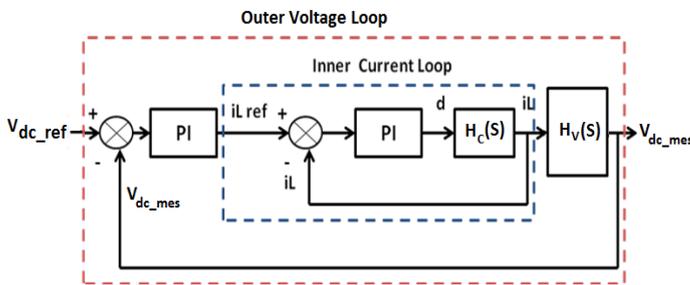The figure below shows the outer voltage and inner current control loops.

Figure 9: Outer voltage and inner current control loops

For stable and continuous operations of the converter, the average input current should be controlled to be dc, which requires that bandwidth of voltage and current loops are separated far apart with a slow voltage loop and a fast current loop. This can make the design of controller easier.

Inner current control loop design

The current loop transfer function $H_c(s)$ obtained above is equivalent in high frequency with parameter values as follow:

$$H_C(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_{out}}{L_{in}s} = \frac{27.6 * 10^3}{s} \qquad (12)$$

The $H_c(s)$ bode plot designates the phase margin PM equals to 90° which is obtained at crossover frequency $\omega c = 2.76*10^4$ rad/s. The PI controller is designed to increase the low frequency gain and reduce the steady state error between the desired and actual inductor currents while maintaining a positive PM at selected crossover frequency. The open loop current transfer function is given by:

$$H_{OL1}(s) = \frac{27.6 * 10^3 * K_p\left(s + \frac{K_i}{K_p}\right)}{s^2} \qquad (13)$$

The phase margin should be 60° at the gain crossover $\omega c = 2{,}76$Krad frequency.

Gain condition: at crossover frequency, the system gain is

unity. $K_p{}^2\left(7.617*10^6 + \left|\frac{K_i}{K_p}\right|^2\right) = 76.176*10^3 \qquad (14)$

Phase condition: at crossover frequency, phase angle of the loop. $\arg(H_{OL1}(j\omega_c)) = PM - 180° = -120° \qquad (15)$

Therefore: $\qquad \frac{K_i}{K_p} = 1.593*10^3 \qquad (16)$

From (14) and (16), we can get the values of parameters K_p and K_i:

$$K_p = 0.0866; \quad K_i = 138 \qquad (17)$$

Outer voltage control loop design

The outer voltage control loop generates the inductor current reference i_{Lref} for the inner current control loop as seen in Fig. 9. The fast current loop can correct for the current errors quickly. For that reason in the voltage loop design, the inner current loop dynamics can be neglected.

Its transfer function is not included in the voltage loop design. The voltage loop transfer function $H_v(s)$ with parameter values is given as follow:

$$H_V(s) = \frac{\hat{V}_{out}(s)}{\hat{i}_L(s)} = \frac{(1-D)}{C_{out}s + \frac{1}{R}} = \frac{36.125}{0{,}068s + 1} \qquad (18)$$

The bode plot of $H_v(s)$ designates the phase margin PM equals to 91.6° obtained at crossover frequency $\omega_c = 531$rad/s. The PI controller is designed to increase the low frequency gain while maintaining minimum PM of 60° at crossover frequency $\omega_c = 53.1$rad/s. The open loop transfer function of dc voltage is given by:

$$H_{OL2}(s) = \frac{36.125 * K_p\left(s + \frac{K_i}{K_p}\right)}{s(1 + 0.068s)} \qquad (19)$$

Gain condition: at crossover frequency, the system gain is unity: $|H_{OL2}(j\omega_c)| = 1$

$$K_p{}^2 * \left(2.819*10^3 + \left|\frac{K_i}{K_p}\right|^2\right) = 30.33 \qquad (20)$$

Phase condition: at crossover frequency, phase angle of the loop: $\arg(H_{OL2}(j\omega_c)) = -120°$

$$\frac{K_i}{K_p} = 53.997 \qquad (21)$$

From (20) and (21), we can get the values of parameters K_p and K_i:

$$K_p = 0.073; \quad K_i = 3.9267 \qquad (22)$$

SIMULATION RESULTS

Before proceeding to the real time part implementation of the hydraulic energy conversion chain, a digital simulation were implemented using matlab/simpower system in order to study the system dynamic performance and efficiency. The sampling time used for the simulation is 0.2μs.

Waveform Signal of Uncontrolled Three Phase Rectifier

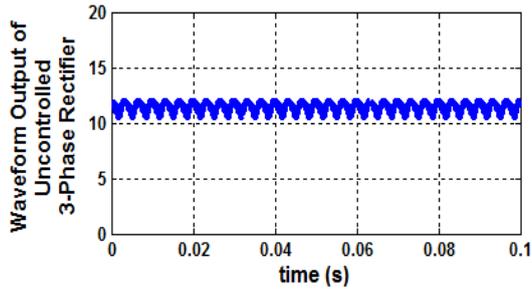The Fig. 10 illustrates the waveform output signal of the three phase uncontrolled rectifier.

Figure 10: Output dc voltage of uncontrolled three phase rectifier

The simulation result of the Fig. 10 shows that the dc output voltage of the uncontrolled three phase rectifier is average equal to 12V and almost filtered by two series output capacitors of 390μF.

Waveform Signal of Controlled Boost Converter

The pulse of boost converter IGBT switch is generated by comparing the triangular carrier waveform to the given duty cycle signal by the control strategy. When the duty cycle signal by the control strategy. When the duty cycle is greater than the carrier, the pulse takes 1 is the high state and if not the pulse takes 0 is the low state.

The following figures display the signals comparison of the triangular carrier with duty cycle, the pulse generated by the PWM Generator block and the dc output voltage of boost converter.
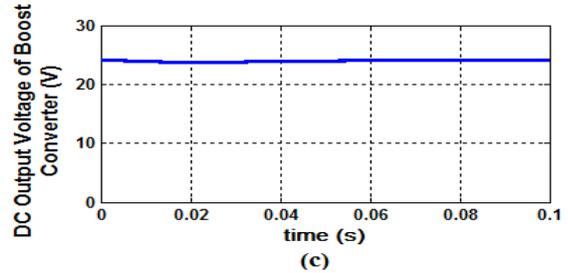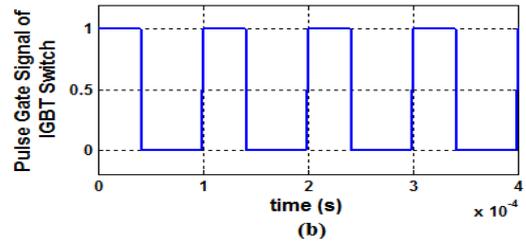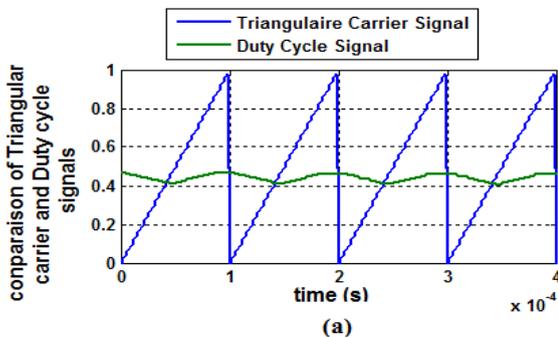

Figure 11: (a) Comparison of triangular carrier and duty cycle signals (b) pulse gate signal of IGBT switch (c) dc output voltage of boost converter

It is seen from the Fig. 11 that the control strategy succeeds to regulate the dc link voltage of boost converter at its set point 24V even if the variation of the load current happened.

EXPERIMENTAL RESULTS

The test bench used for the experiment was developed in our laboratory (Fig. 12 (c)).The control algorithm of the boost converter is based on the gate pulse that generated via the eZdsp F2812 DSP board. The development of this control algorithm is performed with Matlab/Simulink in the first step. The embedded target for the TI TMS320C2000 DSP platform generate the C-code real-time implementation of the Simulink model already done and then the Real-Time Workshop builds a Code Composer Studio (CCS) project from the C code. The generated C code is compiled, linked, downloaded, and executed on an eZdsp DSP board from Spectrum Digital.

The Fig. 12 illustrates the generated C-code real-time implementation of the Simulink model in code composer studio in (a), the pins used on eZdsp F2812 DSP board in (b) and the hardware implementation of the controlled boost converter in (c).
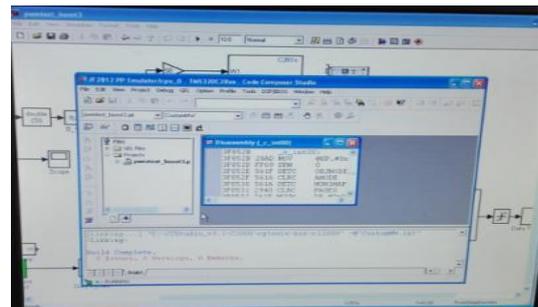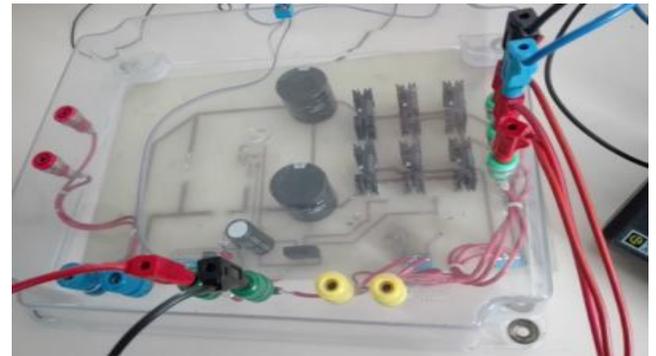

(a)

(b)

(c)

Figure 12: (a) Generated C-code real-time implementation of the Simulink model in code composer studio (b) pins used on eZdsp F2812 DSP board (c) hardware implementation of the controlled boost converter.

Waveform Signal of Uncontrolled Three Phase Rectifier

A three-phase power supply, with line-to-line voltage ranging from 0 to 400V, is used as a source for a three-phase 380V/220V voltage step-down transformer that feeds our uncontrolled three-phase rectifier as represented in Fig. 13 (a),(b),(c). In our case, we have to test and examine our prototype just at low voltage, so we have set the three-phase supply input to have the desired DC voltage output 12V that will subsequently use as a boost converter input.

(a)

(b)

(c)

Figure 13: (a) Hardware implementation full scheme of the uncontrolled three phase rectifier (b) Power circuit of uncontrolled three phase rectifier (c) waveform output of uncontrolled three phase rectifier

The experimental results in the Fig. 13 show that the output voltage of uncontrolled three phase rectifier ac/dc is average equal to 12V and well filtered by the two series capacitors in output of the rectifier. This dc voltage output will be used in the next as the input of boost converter.

### *Waveform Signal of Controlled Boost Converter*

From a dc voltage boost converter input of 12V comes from the three phase uncontrolled rectifier; we wish to obtain a dc voltage output of 24V. The boost converter must deliver a power of 2W. Let IOUT=0.083A with a load resistance RL=289Ω. The output voltage will accept ± 5% ripple, approximately ± 1.2V. The switching frequency is 10 kHz. The Fig. 14 displays in (a) the IGBT gate signal generated by DSP and in (b) the output of opto-coupler 4N25 to isolate the DSP board to the boost converter power circuit.
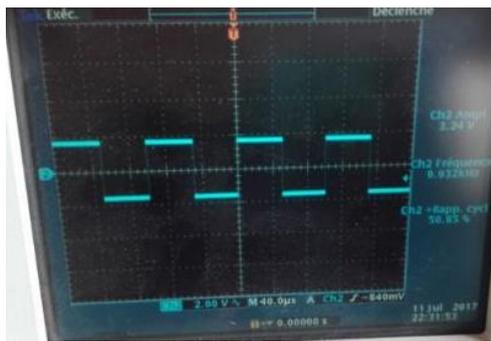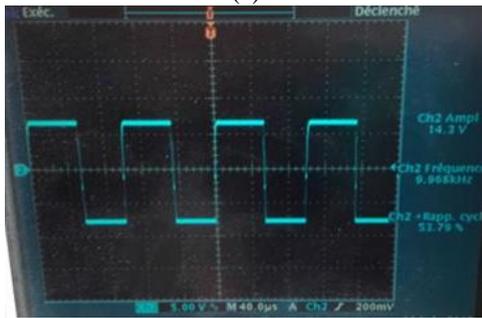
(a)
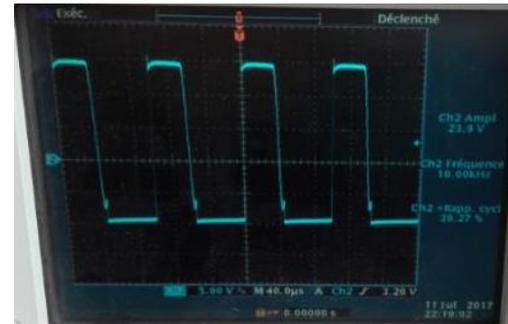
(b)

Figure 15: (a) IR2111 Driver output (b) Collector-Emitter signal of the boost converter

(b)

Figure 14: (a) IGBT gate signal generated by DSP (b) 4N25 opto-coupler output

The Fig. 14 (a) shows the digital output waveform of gate pulse for the boost converter IGBT switch generated by the DSP F2812 which offers a signal variation of 0-3.24V, the switching frequency is 9.968 kHz equals to the imposed frequency10kHz and the duty cycle is about 53.79%. The output signal of opto-coupler is amplified from 3,24V to 14.3V and the others parameters of switching frequency and duty cycle remain the same as before as it can be seen in Fig 14 (b).

The Fig. 15 illustrates in (a) the output of IR2111 Driver for boost converter IGBT and in (b) the Collector-Emitter output signal of the boost converter.
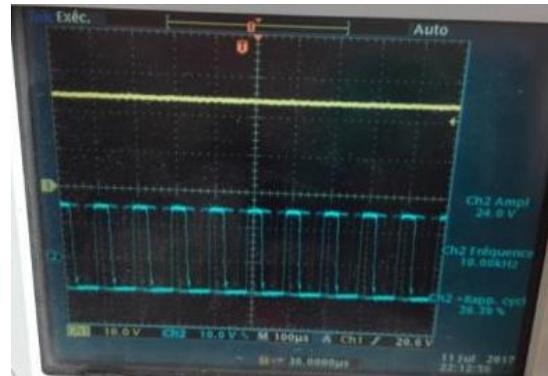
In results demonstrated in Fig. 15(a), The IGBT drivers apply +14.2V to the gate-emitter VGE of the IGBT boost converter when the input signal is logic high and 0V when the input signal is logic low. The gate resistors are selected as 10 ohms for the pulse implementation. For the results in Fig. 15 (b), the output signal of the collector-emitter VCE is boosted to 23,9V as amplitude value with a switching frequency of 10 kHz.

The Fig.16 shows in (CH1) the dc output voltage of the controlled boost converter and in (CH2) the collector-emitter VCE signal output of the IGBT boost converter.

Figure 16: (CH1).dc output voltage of the controlled boost converter, (CH2) collector-emitter VCE signal output of the IGBT boost converter
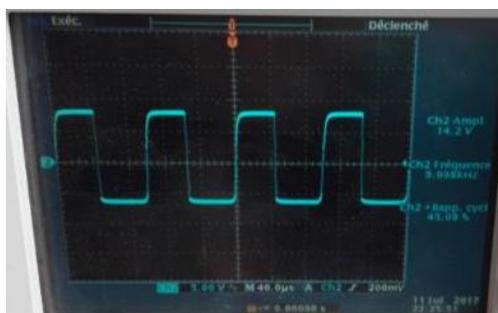
It can be seen from the Fig.16 that the dc link voltage is boosted average to 24V as shown in Fig. 16 (CH1). Also it has been observed that in spite of the load value variation, the two control loops allow us to keep a voltage of 24 V at the load terminal.

Final Global Prototype Card of Experimental Test

The Final global prototype card of experimental test including the boost converter; the three-phase rectifier and the intermediate interface of control has been implemented in a single card as shown in the Fig. 17.

(a)

The Fig. 18 displays the hardware implementation full scheme of the uncontrolled three phase rectifier plus boost converter with its intermediate interface.
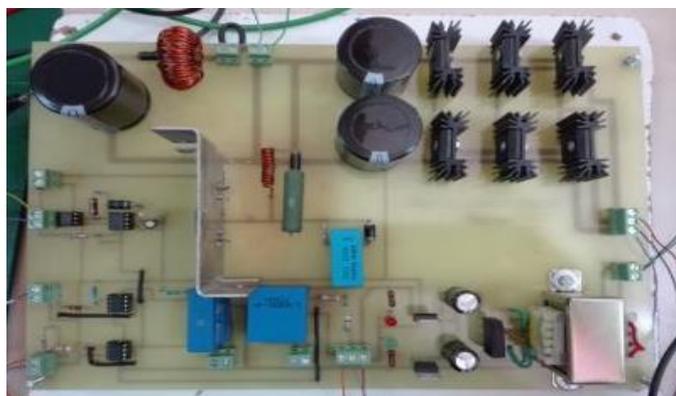

Figure 17: Printed test prototype board of the hardware power part with its intermediate interface

Figure 18: Hardware implementation full scheme of the uncontrolled three phase rectifier plus boost converter with its intermediate interface

CONCLUSION

This paper describes the DSP digital control implementation of the DC/DC boost converter connected with an uncontrolled three phase rectifier as an experimental first part of the hydraulic conversion chain.

The obtained results from the simulation and experimentation of this system match perfectly, they show that the DC output voltage remains almost constant even if the load varies; the control strategy based on the two cascade loops is fast and efficient.

The perspectives of this project are specified as follows:

- Connection with the synchronous generator as a rectifier supply source;

- Increase in power until 1.5Kw;

- Check the effectiveness of the control method with a wide variation of the load current.

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