Space-Vector-Modulation Scheme with Distance Mapping for Multilevel Inverters

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Abstract

In multilevel inverters, as the number of levels increases the complexity associated in the implementation of Space Vector Pulse Width Modulation also increases. In this paper a technique which significantly reduces this complexity with improved inverter performance is proposed. The sequence of switching vectors are most determinant for the voltage total harmonic distortion hence the output rms voltage of the inverter. In the proposed technique, voltage vectors sequence is identified with nearest three voltage vectors using distance calculation in the given sector of the hexagon. The distance mapping technique based on voltage reference vector position with respect to the nearest three voltage vectors are calculated. Identified three nearest vectors are sorted to obtain the switching sequence of the inverter. The switching sequence thus obtained achieves the reduction in total harmonic distortion. The dwell times are calculated for these switching vectors at each sampling instant using classical method, which is independent of the inverter levels without identification of the sector or region. This distance mapping space vector PWM is easily extended to higher levels of the inverters. This technique is verified through simulation and confirmed by hardware implementation for two level as well as for three level diode clamped Voltage Source Inverter.

Keywords: Distance Mapping, Space Vector Diagram, Space Vector Pulse Width Modulation, Nearest Three Vectors, Voltage Source Inverter, Multilevel, Switching Sequence.

INTRODUCTION

The SVPWM technique has been extensively investigated during the past decades. It is a vector approach to pulse width modulation for three phase inverters [1]. It confines space vectors to be applied according to the region where the output voltage vector is located. It is better than conventional Pulse Width Modulation techniques [2] because of features like better DC link utilization, better harmonic performance, reduction in device switching frequency and scope for optimization of switching sequence. In case of multilevel inverter, sector identification further needs region identification and implementation process gets tedious with the increase in number of level. Multilevel inverters outperform two level inverter in diversified ways like low total harmonic distortion in output voltage and current, low \( \frac{dv}{dt} \), low common mode voltage, decreased voltage on the power switches, capability to operate at lower switching frequency [3]. Hence multilevel inverters with space vector pulse width modulation as modulation scheme with higher value of number of levels, \( n' \); became worthy candidate for numerous researchers [4-18] and they come up with various approaches for its execution. The space vector diagram of \( n' \) level inverter is split into \( (n-1)^2 \) triangles each sector of 60°. A scheme which works on classification of triangles, where criterion of classification is on position of base of these triangles was proposed by in [4]. As the scheme frequently needs determination of triangles followed determination of category of triangles, memory consumption is more and operating speed gets affected. Hexagon decomposition method was presented in [5]. The three level space vector diagram is decomposed into six two-level hexagons. Then on the basis of the location of \( V_{ref} \) the appropriate two level hexagon is selected. The centre of this two level hexagon is then reallocated to the centre of the three level space vector diagram. After this reallocation the three-level space vector plane can be treated as a two-level space vector plane. The selection of NTV and subsequent calculation of their 'ON' durations are done as in a classical two-level inverter. On the similar lines, extension of this methodology is proposed in [6] by testing it for a five level inverter but substantial computational overload becomes unavoidable in the process.

The application of a 60° spaced g-h coordinate transformation instead of orthogonal \( \alpha-\beta \) system was suggested in [7] for the space vector modulation of multilevel inverters. However, this technique needs matrix transformations several times and lacks concrete approach for determination of the switching sequences. On the similar line
[8] presented a scheme but the unconventional g-h coordinate system is avoided. However, the formulae for switching states and duty cycle are changed frequently as they are subject to sector where \( V_{\text{ref}} \) is located. Moreover, absence of systematic approach for switching sequence design makes its implementation a complex job when the ‘\( n'\) goes up. The nearest three vectors for \( V_{\text{ref}} \) for any sector can be established by employing the reverse mapping of the inner two-level sub-hexagon to any prescribed outer two level sub hexagon [9]. In the process the multilevel space vector diagram is divided into a number of layers and identification of the layer in which \( V_{\text{ref}} \) lies is always required before proceeding for implementation of space vector modulation. The generation of the voltage space vectors by repeated ‘Triangularization’ scheme was introduced in [10]. It exploits the fractal arithmetic for SVPWM implementation and lookup tables are not warranted in the scheme. For higher number of levels the process of ‘Triangularization’ becomes lengthy as number of times it is to be repeated directly depends on ‘\( n'\’. The technique which uses instantaneous reference phase voltage amplitudes for the generation of the space vector pulse width modulation signals for multi-level inverters is presented in [11-12]. The lookup tables and sector mappings are not required.

The simplification of the tedious process of implementation of space vector pulse width modulation for multi-level inverters still remains a challenge and to deal with it some neoteric approaches [13-15] are presented. The techniques named as simplified space vector modulation and further simplified space vector modulation are proposed in which the simplification is achieved at the cost of increase in total harmonic distortion for modulation index above certain range [13]. A SVPWM scheme based on two orthogonal unit vectors that decouple the three phase components is presented in [14] whereas another space vector pulse width modulation scheme based on dwell times calculations based on a new approach of three non-orthogonal static reference frames is presented in [15].

This paper presents a simplified method for implementation of space vector pulse width modulation i.e. Distance Mapping Space Vector Pulse Width Modulation for multi-level inverters. It has advantages like no sector and region identification is needed, memory requirement reduced as look up tables are not required, sector based complex trigonometric functions not required, less computation burden and an unique and efficient switching sequence design. The significant contributions of this work are:

- A simplified method for selection of nearest three vectors using distance mapping is introduced which reduces complications of implementation of space vector pulse width modulation for multilevel inverter.

- An novel switching sequence based on distance mapping is presented which proves its efficiency with respect to harmonic content in output voltage.

In this work the proposed concept of space vector pulse width modulation is discussed comprehensively for two and three-level inverters and generalized algorithm is also given for multi-level inverters with any arbitrary value of ‘\( n'\’. Section II gives basics of conventional space vector pulse width modulation for two-level inverter. In Section III proposed Distance Mapping Space Vector Pulse Width Modulation and its implementation for two and three-level is discussed. Section IV gives generalized algorithm for its extension for multilevel inverters. Experimentation and discussions are given in section V.

CONVENTIONAL SPACE VECTOR PULSE WIDTH MODULATION METHOD FOR TWO LEVEL THREE PHASE INVERTER

In space vector pulse width modulation a sampled reference vector is synthesized by maintaining volts-second balance by the nearest three switching vectors. The representation of rotating reference voltage vector as well as all the switching state vectors for given sampling time is done in a complex plane by means of the d-q transformation.

\[
V_{\text{ref}} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \left( \frac{2\pi}{3} \right) & \cos \left( \frac{4\pi}{3} \right) \\ \sin \left( \frac{2\pi}{3} \right) & -\sin \left( \frac{4\pi}{3} \right) \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{1}
\]

Where \( V_d \) and \( V_q \) are d-axis and q-axis components of reference voltage \( V_{\text{ref}} \) in d-q plane respectively; \( V_a, V_b \) and \( V_c \) are three phase sinusoidal voltage components of reference voltage \( V_{\text{ref}} \) in a-b-c plane.

A two-level inverter as shown in Figure 1(a) can switch in eight different modes to generate voltage space vectors. There are eight possible ways the inverter can switch to create. Out of these, two zero voltage vectors are set at the centre and remaining six non zero voltage vectors form six peripheral vertices of hexagonal shaped space vector diagram as shown in Figure 1(b).

![Image](image-url)
The output voltage synthesis is formulated volt-time balance by the following equation

\[ V_{\text{ref}} T_3 = V_1 T_1 + V_2 T_2 + V_0 T_0 \]  

(2)

\[ T_1 = m T_s \sin \left( \frac{\pi}{3} - \phi \right) \]  

(3)

\[ T_2 = m T_s \sin \phi \]  

(4)

\[ T_0 = T_s - T_1 - T_2 \]  

(5)

where, \( T_3, T_2, T_0 \) are respective 'ON' times for vectors \( V_1, V_2, V_0 \); \( T_s \) = switching time; \( m \) = modulation index (M. I.), \( \phi \) = angle between the closest clockwise state vector and rotating reference vector \( V_{\text{ref}} \), as shown in Figure 1b.

The modulation index, \( m \), is defined by

\[ m = \sqrt{3} \frac{V_{\text{ref}}}{V_{dc}} \]  

(6)

where, \( V_{dc} \) = DC bus voltage and \( V_{\text{ref}} \) = magnitude of reference voltage vector.

The space vector pulse width modulation realization at a every sample time needs sector identification along with determination of the nearest three vectors, determination of the modulation index ‘\( m \)’ followed by determination of the dwell times and finally design of switching sequence.

**PROPOSED TECHNIQUE OF DISTANCE MAPPING SPACE VECTOR PULSE WIDTH MODULATION EXECUTION FOR THREE PHASE TWO LEVEL INVERTER**

As the reference vector \( V_{\text{ref}} \) rotates continuously in d-q plane, the distances between tip of rotating reference vector and all eight stationary switching vectors keep changing continuously. For a sampling instant if all these distances are calculated and sorted out to obtain nearest three vectors which form a triangle. For distance calculations the d-q plane can be mapped equivalent to x-y plane. Even for the same triangle the order among the nearest three vectors i.e. the first nearest vector, the second nearest vector and the third nearest vector changes with change in position of \( V_{\text{ref}} \). This observation is used for designing the switching sequence. The realization of Distance Mapping Space Vector Pulse Width Modulation for two level inverter for every sampling instant requires the determination of nearest three vectors \( V_{\text{ref}} \) along with all switching states, selection of nearest three vectors, their dwell times calculations and finally switching sequence design. The process of implementation of Distance Mapping Space Vector Pulse Width Modulation is accomplished by performing following steps:

A. Determination of X-Y coordinates of \( V_{\text{ref}} \).

B. Determination of X-Y coordinates of All Switching States.

C. Determination of Nearest Three Vectors by Distance Calculations.

D. Dwell Times Calculations:

E. Switching sequence design on the basis of distances of Nearest Three Vectors.

These steps are described in detail in subsections A to E as follows:

**Determination of X-Y coordinates of \( V_{\text{ref}} \).**

Mapping of x-y coordinates of \( V_{\text{ref}} \) can be done applying following steps:

**Step 1:** Select the constant value of Modulation Index and switching frequency \( (f_s) \) for which inverter is to be operated.

**Step 2:** Calculate magnitude of \( V_{\text{ref}} \) from Modulation Index and V_{dc} by using equation (6).

**Step 3:** For the first sampling instant angle of \( V_{\text{ref}} \) is set as \( 0^\circ \). Then,

\[ V_{dr} = |V_{\text{ref}}| \cos \theta_r \]  

(7)

\[ V_{qr} = |V_{\text{ref}}| \sin \theta_r \]  

(8)

where, \( V_d \) = direct axis or X axis coordinate of \( V_{\text{ref}} \); \( V_q \) = quadrature axis or Y axis coordinate of \( V_{\text{ref}} \); \( \theta_r \) = angle between the d axis and rotating reference vector \( V_{\text{ref}} \).
Step 4: After first sampling instant the process is repeated for 'P' times in a cycle and then repeated continuously for next cycles.

\[ P = \frac{1}{f_s} \cdot \frac{f_1}{f_s} \]  \hspace{1cm} (9)

\[ \delta = \frac{360}{P} \]  \hspace{1cm} (10)

\[ f_s = \frac{1}{T_s} \]  \hspace{1cm} (11)

\[ \theta_r(j+1) = \text{Initial angle } \theta_r + \delta \]  \hspace{1cm} (12)

where, \( P \) = total sampling points in one cycle i.e. \( 360^\circ \), \( \delta \) = angle of rotation of \( V_{ref} \), \( f_1 \) = fundamental frequency; \( f_s \) = switching frequency; \( T_s \) = sampling time, \( j = 1, 2, .....P \).

Determination of X-Y coordinates of All Switching States.

The magnitudes and respective angles of all eight switching vectors can be calculated on the basis of magnitude of the DC Bus voltage (\( V_{dc} \)) of two-level inverter power circuit, which is shown in Figure 1a. There x-y axis coordinates are obtained accordingly and can be stored in arrays \( X_{v[i]} \) & \( Y_{v[i]} \) as shown in equation (13). For two-level inverter there will be seven locations of eight switching states or stationary vectors as there is one redundant vector at the centre of space vector diagram i.e. Hexagon.

Determination of Nearest Three Vectors by Distance Calculations.

At any sampling point, the distances between tip of \( V_{ref} \) and all eight switching vectors are calculated as shown in Figure 2 and stored in an array \( D_{[i]} \)

\[ D_{[i]} = \sqrt{(X_{ref} - X_{v[i]})^2 + (Y_{ref} - Y_{v[i]})^2} \]  \hspace{1cm} (13)

where, \( D \) = distance between \( V_{ref} \) and any switching state; \( i = 0, 1, 2, ..... (n^2-1) \) \( (n = \text{number of levels of multi-level inverters}) \); \( X_{ref} \) = X-axis coordinate of reference vector; \( Y_{ref} \) = Y-axis coordinate of reference vector; \( X_i \) = X-axis coordinate of stationary vector; \( Y_i \) = Y-axis coordinate of stationary vector.

The nearest three vectors from \( V_{ref} \) for a particular sampling point are obtained by simply sorting out the distances of all switching vectors. For any sampling point let \( D_1, D_2 \) & \( D_3 \) be the distances of first nearest vector, second nearest vector and third nearest vector respectively.

Dwell Times Calculations:

For higher switching frequency, the sampling time \( T_s \) is small enough to treat the \( V_{ref} \) as a constant during the same. The ‘ON’ times duration of the nearest three vectors of the \( V_{ref} \) as shown in Figure 3 at any position in space vector diagram of ‘n’ level inverter can be computed by classical two level approach [16] which is independent of number of levels, by using following equations represented in matrix form:

\[
\begin{bmatrix}
T_1 \\
T_2 \\
T_3 
\end{bmatrix} = \begin{bmatrix}
V_{d1} \\
V_{d2} \\
V_{d3}
\end{bmatrix} \begin{bmatrix}
V_{dr} & V_{dq} & V_{d3} \\
1 & 1 & 1
\end{bmatrix}^{-1} \begin{bmatrix}
V_{dr} & V_{dq} \\
1 & 1
\end{bmatrix} \begin{bmatrix}
V_{d1} \\
V_{d2} \\
V_{d3}
\end{bmatrix}
\]  \hspace{1cm} (14)

where, \( T_1, T_2 \) & \( T_3 \) represent the "dwell times" of the Nearest Three Vectors; \( V_{d1}, V_{d2} \) & \( V_{d3} \) are direct axis or X-axis coordinates of nearest three vectors; \( V_{dq} \) & \( V_{d3} \) are quadrature axis or Y-axis coordinates of nearest three vectors; \( V_{dr} \) is direct axis or X-axis coordinate of reference vector \( V_{ref} \) & \( V_{dp} \) is quadrature axis or Y-axis coordinate of reference vector \( V_{ref} \). Nearest three vectors are treated in ascending order of distances from \( V_{ref} \). Refer Figure 3 which shows only \( V_{d1}, V_{d2}, V_{d3} \) & \( V_{dq} \) for the sake of simplicity.

The direct axis or X-axis coordinate of switching vector is defined by,

\[ V_d = |V| \cos \theta \]  \hspace{1cm} (15)

The quadrature axis or Y-axis coordinate of switching vector is defined by,

\[ V_q = |V| \sin \theta \]  \hspace{1cm} (16)

where, \( \theta \) = Angle between the \( d \) axis and stationary switching vector among Nearest Three Vectors and \( *= 1 \) or 2 or 3 (i.e. order of Nearest Three Vectors).
The direct axis or X-axis coordinate of \( V_{\text{ref}} \) i.e. \( V_{dr} \) and the quadrature axis or Y-axis coordinate of \( V_{qr} \) can be found by using equations (7) and (8).

**Figure 3:** \( V_{\text{ref}} \) and its component in d-q axis.

**Switching sequence design on the basis of distances of Nearest Three Vectors.**

The performance of inverter with respect to harmonic content in the output voltage and current is function of switching sequence design [17-18]. Distance calculations and sorting process not only contribute for identification of nearest three vectors at each sampling instant but they can be utilized in a novel way to design an unique switching sequence which contributes for lower harmonic contents also. The nearest three vectors are further identified as first nearest vector, second nearest vector and third nearest vector. Switching sequence is designed on the basis of distances of nearest three vectors. For a particular sampling point out of the nearest three vectors the first nearest vector applied first for its respective time duration \( T_1 \) followed by the second nearest vector for its respective time duration \( T_2 \) and the third nearest vector applied for its respective time duration \( T_3 \) in the end.

**Figure 4:** Selection of switching sequence: (a) Case 1 (b) Case 2.

For example for the position of \( V_{\text{ref}} \) as shown in Figure 4(a) first nearest vector = \( V_1 \); second nearest vector = \( V_0 \); third nearest vector = \( V_2 \). Whereas for the position of \( V_{\text{ref}} \) as shown in Figure 4(b) first nearest vector = \( V_2 \); second nearest vector = \( V_0 \) & third nearest vector = \( V_1 \). The above mentioned process holds good for one time instant or one sample only. This process is repeated for continuous operation of inverter. Redundancy in nearest three vectors is taken in to consideration and applied appropriately.

**Extension Of Distance Mapping Space Vector Pulse Width Modulation To Three Phase Multilevel Inverter:**

For implementation of Distance Mapping Space Vector Pulse Width Modulation to multi-level inverters with any arbitrary value of \( n' > 2 \), some modifications are required only in the subsection B of the section III as it is dynamic to \( n' \) i.e. number of levels in multi-level inverters. The remaining subsections i.e. A, C, D and E are independent of \( n' \) and can be implemented as explained for two-level inverters in section III. The subsection B deals with creation of space vector diagram which is critical for Distance Mapping Space Vector Pulse Width Modulation scheme.
The creation of space vector diagram depends on number of levels 'n'. For given value of V\textsubscript{dc}, though the area of space vector diagram remains same but number of switching vectors and number of redundant vectors along with their location on x-y plane depends on value of 'n' in multi-level inverters. Hence space vector diagram which tends to become complex with increasing 'n' is needed to be worked on. This is done by a code which gives x-y co-ordinates of all possible i.e. \( n^2 \) switching states associated with space vector diagram of three-phase inverter, the values of 'n' and V\textsubscript{dc} are treated as input parameter to the code.

The neutral point clamped three level inverter, for sake of simplicity. Its circuit diagram, space vector diagram in d-q plane and space vector diagram in x-y plane is shown in Figure 5(a), 5(b) & 5(c) respectively. There are 27 possible switching vectors out of which 7 vectors are redundant [2]. Hence in Figure 5, overall 19 locations of 27 possible switching vectors and its distances from V\textsubscript{ref} in x-y plane are highlighted. The flow chart shown in Figure 6 explains the generalized implementation of the Distance Mapping Space Vector Pulse Width Modulation technique for 'n' level three phase inverter. The calculations of x-y co-ordinates of

Figure 5: (a) Three-level inverter (Neutral Point Clamped); (b) Space Vector Diagram of three-level inverter; (c) V\textsubscript{ref} and its distance between all 27 switching states in space vector diagram of three-level inverter.

Figure 6: Control algorithm for Distance Mapping Space Vector Pulse Width Modulation for 'n' level three phase inverter.
stationary switching vectors which depends on "n" of multi-level inverters and x-y co-ordinates of continuously rotating reference vector are of primary importance here.

EXPERIMENTATION AND DISCUSSIONS

The proposed technique is validated by conducting the experiments on prototype of three phase two-level and three phase three-level space vector pulse width modulation inverter build in laboratory for different modulation index values. The parameters used for experimentation are DC bus voltage $V_{dc} = 150$ V, switching frequency $f_s = 4$ kH, sampling interval $T_s = 0.25$ ms, output frequency of inverter is 50 Hz.

The ratings of DC link capacitors $C_1$ and $C_2$ are 1000 µF, 200 V and star connected three phase R-L load is used with $R = 100$ Ω per phase and $L = 600$ mH per phase. The power semiconductor switch used for making inverter is insulated gate bipolar transistor (FGA25N120ANTD). The DC link voltage of inverter is generated from single phase diode bridge rectifier (KBPC3510). The dead time of 1 µs is maintained between complimentary switches through coding only. 74LS07 IC is used as a buffer and TLP250 IC is used as a gate driver. For three level circuit MUR8100E is used as clamping diode. Field programmable gate array Altera DE0 nano (cyclone IV) with QUARTES-II software is used for generation of gate pulses needed for the operation of the inverter. The snapshot of actual working hardware prototype with details is shown in Figure 7. Experimental results of line voltage and its harmonic spectrum i.e. fast fourier transform analysis are shown in Figures 8 and 9 for two level inverter whereas Figures 10 and 11 show the same for three level inverter.

![Hardware prototype](image)

*Figure 7: Hardware prototype of circuit for implementation.*

![Experimental result of line voltage waveform for M. I. = 1.0 (50 Hz) (CH2:10 ms/div, 50 V/div) (two-level inverter).](image)

*Figure 8: Experimental result of line voltage waveform for M. I. = 1.0 (50 Hz) (CH2:10 ms/div, 50 V/div) (two-level inverter).*

![FFT analysis of line voltage waveform for M. I. = 1.0 (two-level inverter).](image)

*Figure 9: FFT analysis of line voltage waveform for M. I. = 1.0 (two-level inverter).*

![Experimental result of line voltage waveform for M. I. = 1.0 (50 Hz) (CH2:10 ms/div, 50 V/div) (three-level inverter).](image)

*Figure 10: Experimental result of line voltage waveform for M. I. = 1.0 (50 Hz) (CH2:10 ms/div, 50 V/div) (three-level inverter).*
The performance of two-level and three-level inverters for simulated as well as experimental results with respect to percentage total harmonic distortion of line voltage over a wide range of modulation indices is shown in Figure 12. MATLAB simulink is used for simulation results. It is observed the percentage total harmonic distortion of line voltage improves for three-level inverter as compared to two-level inverter.

![Figure 12: % Total Harmonic distorsion Vs Modulation index for Distance Mapping Space Vector Pulse Width Modulation method for two and three-level Inverter.](image)

**CONCLUSION**

This paper presents new Distance Mapping Space Vector Pulse Width Modulation technique, which simplifies the implementation of space vector pulse width modulation for multi-level inverters in which sector and region identification, extra coordinate transformations and sector based complex trigonometric calculations are not required. Dwell time calculations for multi-level inverters are also simplified as the classical two-level method is used for it. The superior performance of Distance Mapping Space Vector Pulse Width Modulation with respect to harmonic content of line voltage underlines the efficacy of the novel switching sequence. For a wide range of modulation indices varying from 0.2 to 1.0, the two-level Distance Mapping Space Vector Pulse Width Modulation inverters achieves 4.4% average reduction in Line Voltage total harmonic distortion as compared with the conventional method. Similarly, the three-level Distance Mapping Space Vector Pulse Width Modulation inverters achieves 21.7% average reduction in line voltage total harmonic distortion as compared with the hexagon decomposition method. The simulation and hardware results for two-level and three-level three phase inverter validate the performance of the proposed method. Simplicity with efficacy proves to be the powerful feature of Distance Mapping Space Vector Pulse Width Modulation.

**REFERENCES**


