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A Comparative Analysis of Modified Cascaded Multilevel Inverter Having Reduced Number of Switches and DC Sources

Lipika Nanda[1], Prof. A. Dasgupta[2] and Dr. U.K. Rout[3]

[1]School of Electrical Engineering,
Kalinga Institute of Industrial Technology,
Bhubaneswar, Odisha, India.

[1]Orcid: 0000-0001-8176-8625

Abstract

Multilevel inverters , covering a wide power range are currently considered as a better industrial solution for high dynamic performance and power-quality demanding applications. In this converter ,for specific time intervals fewer switches will be conducting so switching loss is also reduced . To generate gating signal Phase Disposition Pulse Width Modulation (PDPWM) technique is used here. This paper represents overall THD for different levels and different carrier frequencies. In this paper switching loss,conduction loss of inverter have been discussed and hence inverter efficiency can be calculated. Simulation studies are presented by using MATLAB/SIMULINK.

Keywords: Bidirectional switch ,Switching loss,Symmetric MLI ,Asymmetric MLI,Total harmonic distortion and Voltage stress

INTRODUCTION

Multilevel inverters are divided into three categories, they are neutral point clamped , flying capacitor and cascade H-bridge [1]. Considering the number of components,high reliabilitand modular cascaded MLI is being chosen. As the number of level increases, the number of H-bridges also increases [2]. This makes the system more complicated. Depending upon the voltage source used cascaded MLI are classified into two, they are symmetrical and asymmetrical Cascaded MLI.[3] Dc voltages are having different values in asymmetrical Cascaded multilevel inverter. So the Inverters achieve higher number of voltage levels compared with symmetrical configuration for same number of power switches. DC sources are replaced by the capacitors to reduce the number of DC sources in a symmetrical cascaded topology. It may cause voltage balancing problem [4]- [7]. A different topology of MLI designed from several bidirectional switches is proposed in.[8] . The voltage stress across the switches is higher due to presence of bidirectional switches.[9]

RESEARCH METHOD

It has two voltage sources V_1 and V_2 along with two capacitors C_1 and C_2 which act like voltage divider circuit[6]. If the values of $V_1 = V_2$ it is treated as symmetrical otherwise asymmetrical. Existing Topology produces 7/9/11 levels with certain voltage combinations .

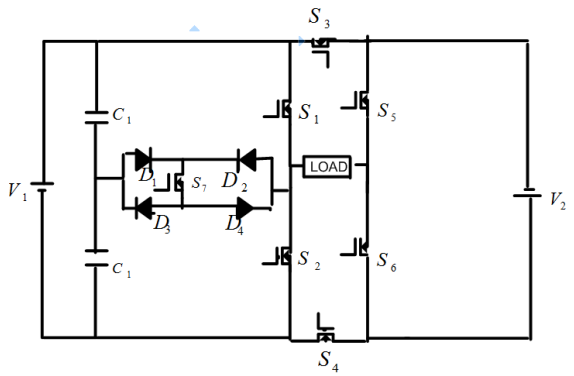

Figure 1. Existing Topology

Existing topology produces upto 11 levels and higher levels have not been achieved with this topology .Hence to achieve higher levels (i.e 13th and 17th) modified Topology has been proposed. With increase in number of levels THD had been reduced significantly in asymmetrical configuration. However this modified topology also achieves 9levels in symmetrical configuration.

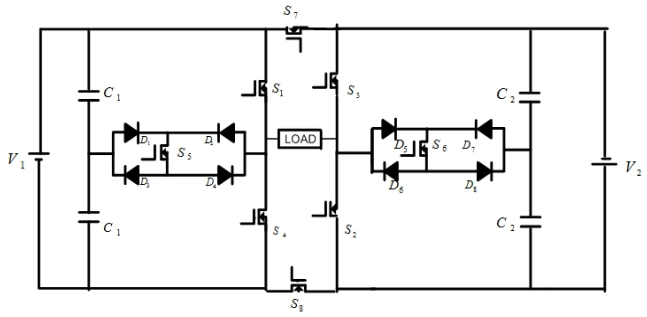

Figure 2. Modified Topology

MODES OF OPERATION

Different modes of operation of 13 level proposed topology have been represented in this paper for this implicity to reader whereas the same topology has been verified for 17levels also.

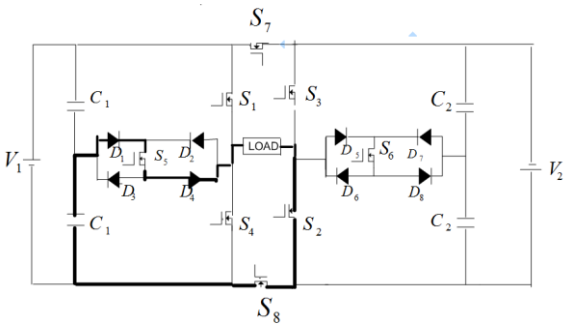

Figure 3: Mode of operation 1

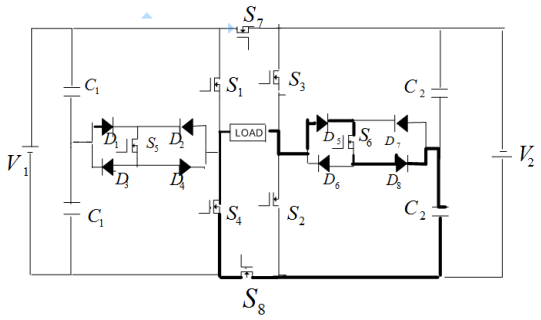

Figure 4: Mode of operation 2

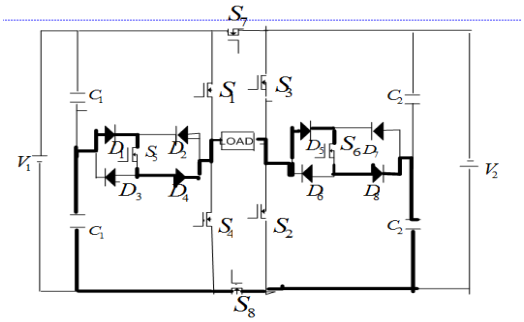

Figure 5: Mode of operation 3

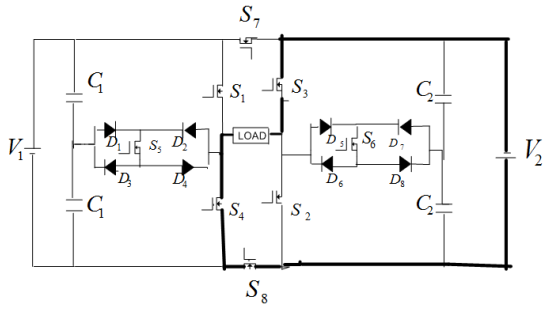

Figure 6: Mode of operation 4

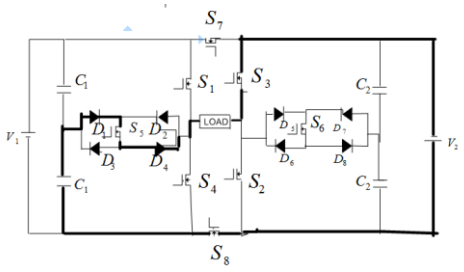

Figure 7: Mode of operation 5

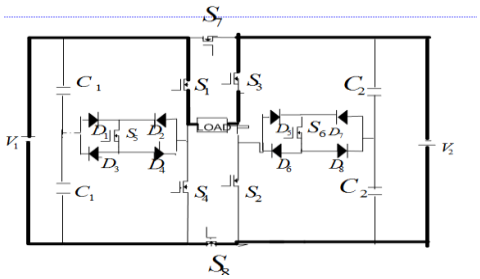

Figure 8: Mode of operation 6

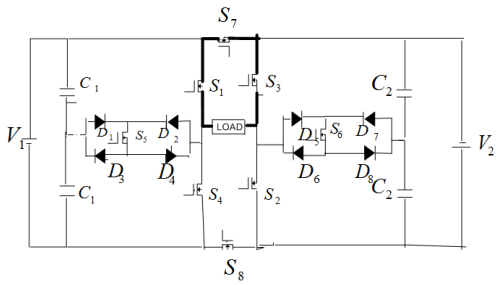

Figure 9: Mode of operation 7

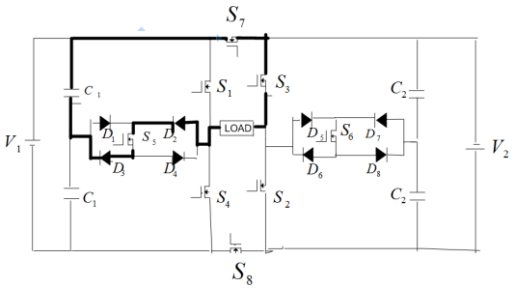

Figure 10: Mode of operation 8

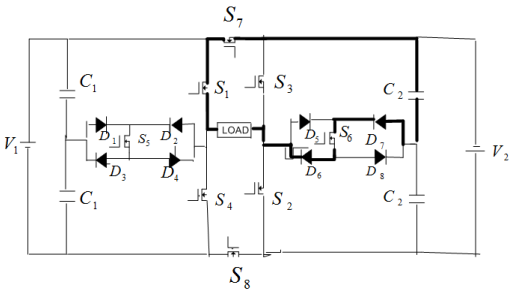

Figure 11: Mode of operation 9

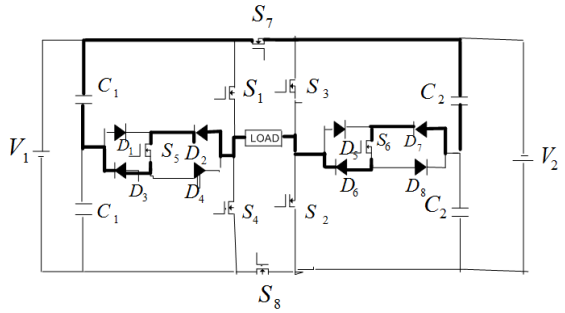

Figure 12: Mode of operation 10

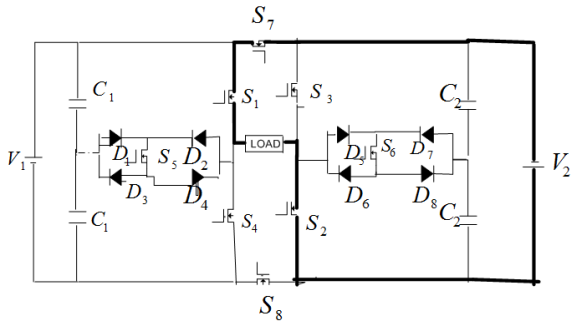

Figure 13: Mode of operation 11

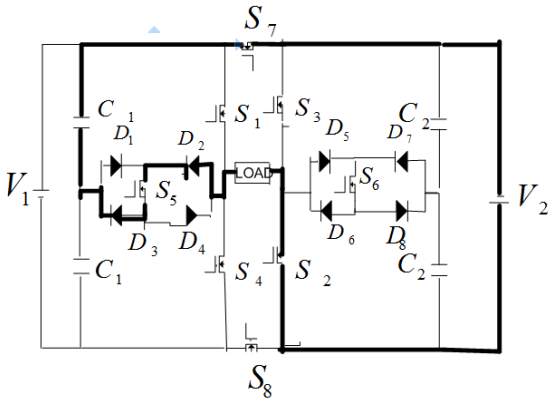

Figure 14: Mode of operation 12

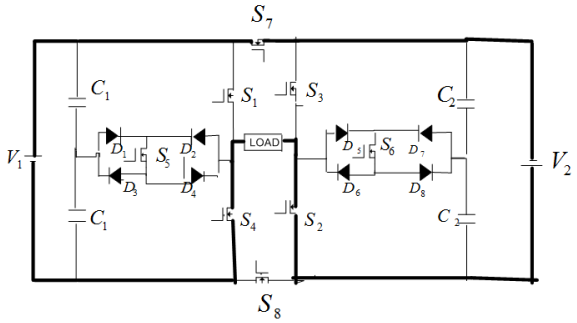

Figure 15: Mode of operation 13

SWICHING STATES

This section of the paper represents various switching states of proposed asymmetrical cascaded MLI. It shows V_1=V/2, V_2=V where V dc =V/4 to generate 13 levels and V_1=V, V_2=3V where V dc =V/2, to generate 17 levels. **T**his section also explains binary configuration where one source voltage value is double the value of other and trinary where one source voltage value is thrice the value of other source voltage.

The carrier based PWM method for multilevel inverters can be generally classified into two categories: phase shifted and level shifted modulations. Both can be applied to the cascaded multilevel inverter [8]-[9]. THD of phase shifted modulation is much higher than level shifted modulation. Hence level shifted modulation technique is being chosen.

Table 1. Different Switching Strategies

1 3 Levels				17 Levels		
Output	Conducting switches	Conducting Diodes		Output	Conducting switches	Conducting Diodes
V_{dc}	S_5 , S_2 , S_8	D1,D4		V_{dc}	S_5 , S_2 , S_8	D1,D4
$2V_{dc}$	S_6 , S_4 , S_8	D5,D6		$2V_{dc}$	S_1 , S_2 , S_8	NIL
$3V_{dc}$	S_5 , S_6 , S_8	D1,D4,D5,D8		$3V_{dc}$	S_8 , S_4 , S_6	D5,D8
$4V_{dc}$	S_8 , S_4 , S_3	NIL		$4V_{dc}$	S_8 , S_5 , S_6	D1,D2,D3,D4
$5V_{dc}$	S_8 , S_5 , S_3	D1,D4		$5V_{dc}$	S_1 , S_6 , S_8	D5,D8
$6V_{dc}$	S_8 , S_1 , S_3	NIL		$6V_{dc}$	S_8 , S_4 , S_3	NIL
0	S_1 , S_3 , S_7	NIL		$7V_{dc}$	S_8 , S_5 , S_3	D1,D4

$-V_{dc}$	S_5 , S_3 , S_7	D2,D3		$8V_{dc}$	S_8 , S_1 , S_3	NIL
$-2V_{dc}$	S_7 , S_1 , S_6	D7,D6		0	S_1 , S_2 , S_3	NIL
$-3V_{dc}$	S_5 , S_6 , S_7	D7,D6,D2,D3		$-V_{dc}$	S_7 , S_3 , S_5	D2,D3
$-4V_{dc}$	S_2 , S_1 , S_7	NIL		$-2V_{dc}$	S_7 , S_3 , S_4	NIL
$-5V_{dc}$	S_2 , S_5 , S_7	D2,D3		$-3V_{dc}$	S_6 , S_1 , S_7	D7,D6
$-6V_{dc}$	S_2 , S_4 , S_7	NIL		$-4V_{dc}$	S_6 , S_5 , S_7	D2,D3,D7,D6
x	x	x		$-5V_{dc}$	S_7 , S_6 , S_4	D7,D6
x	x	x		$-6V_{dc}$	S_2 , S_1 , S_7	NIL
x	x	x		$-7V_{dc}$	S_2 , S_7 , S_5	D2,D3
x	x	x		$-8V_{dc}$	S_2 , S_4 , S_7	NIL

MODULATION SCHEME

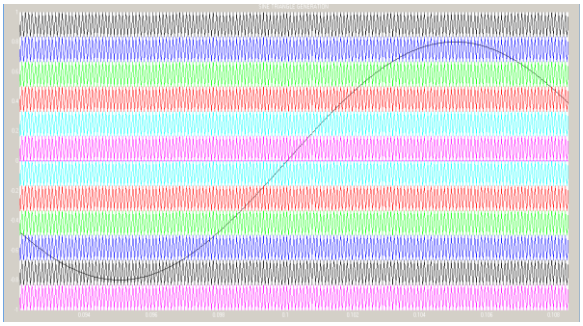

Figure 16. PWM signals for Modified Topology(13 levels)

SIMULATION RESULTS

The proposed topology simulations are carried out in MATLAB environment and results are compared. Following Figure 17.represents output voltage and current wave form at Carrier Frequency=10KHz,R=10Ω,L=25mH.

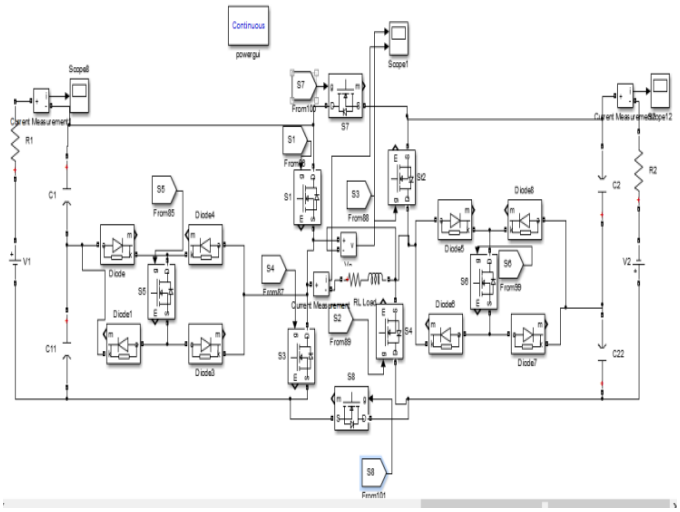

Figure 17(a). simulations for Modified Topology(13 levels)

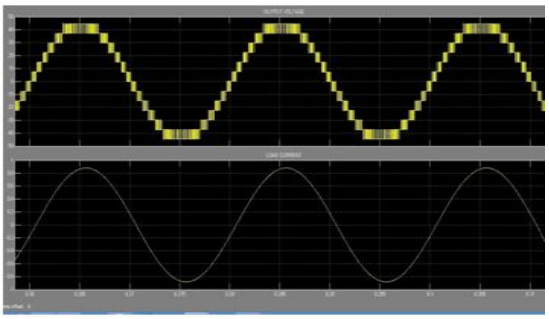

Figure 17(b). Simulations voltage signal and THD for Modified Topology(13 levels)

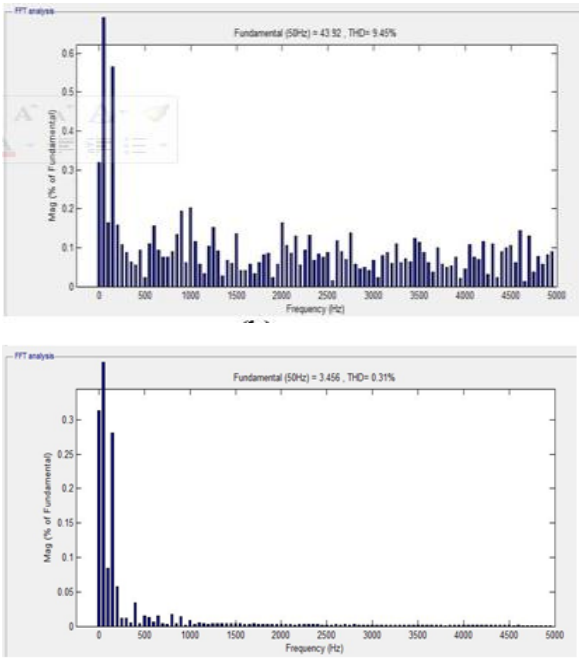

Figure 17(c) Current THD

RESULTANALYSIS & LOSS CA LCULATION

Proposed modified Topology has been simulated for 13 levels and 17 levels generation and results are represented in the following tables for comparison. From table 3 it has been

concluded that with increase in carrier frequencies the inverter losses increased at same Modulation index. FFT analysis for both voltage and current have been presented as the load is RL type. With increase in Modulation index the current THD reduces as observed from figure19.

Each Mosfet loss has been calculated from simulation result. The voltage and current wave forms are observed from simulation diagram of each switch and thus power is being calculated. From power pulse of each switch at different carrier frequencies the switching and conduction losses are calculated. At carrier frequency 10 KHz, different losses are calculated as shown below, in table 2.

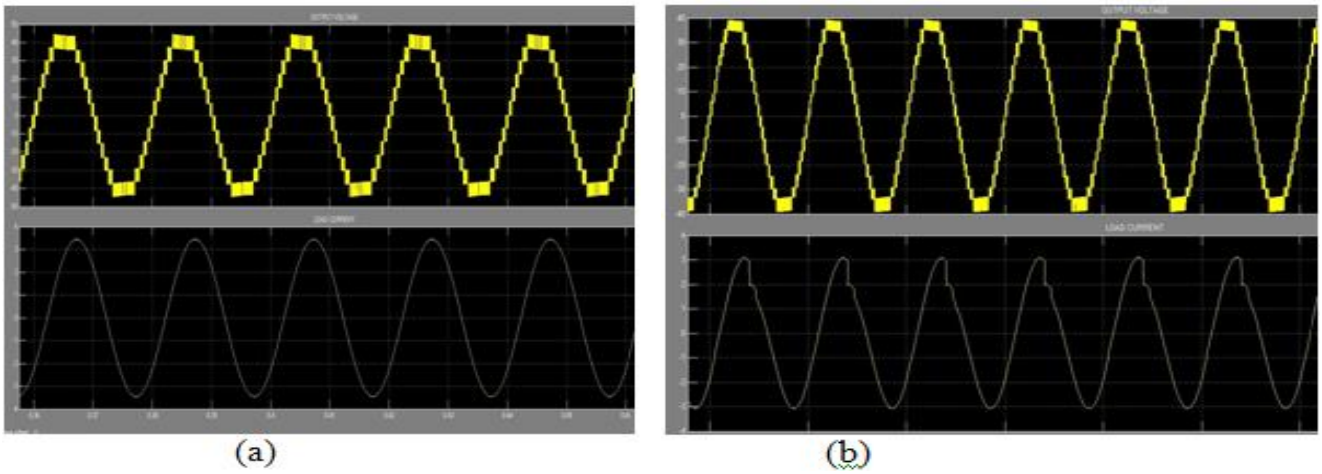

Figure 18.(a) Load voltage and current in 13 level at MI=1 **(b)** Load voltage and current in 17 level at MI=1

Table 2. Calculation of Switching, Conduction and Total Circuit loss at 10KHz Carrier Frequency

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Total
Switching loss (in W)	0.035	0.0016	0.0012	0.0023	0.05	0.0489	0.06	0.06	0.259
Conduction Loss (in W)	0.0051	0.0052	0.005	0.0052	0.0055	0.0051	0.005	0.045	0.081
Total Loss (in W)	0.0401	0.0068	0.0062	0.0075	0.0555	0.054	0.065	0.105	0.0249

Table 3. Loss at different carrier frequencies

Carrier Frequencies (in KHz)	Input power (in W)	Output Power (in W)	Inverer loss (in W)	V_{THD}	I_{THD}
1	62.26	56.7	8.56	8.66	1.91
3	65.9	57.20	8.7	9.92	1.45
5	66.83	57.6	9.23	10.52	1.05
7	68.11	58.6	9.51	10.54	0.74
10	69.49	59.22	10.27	9.34	0.31

Modulaion Index	V_{THD}	I_{THD}
0.6	15.2	0.12
0.7	13.8	0.18
0.8	12.42	0.22
0.9	10.72	0.25
1	9.34	0.31

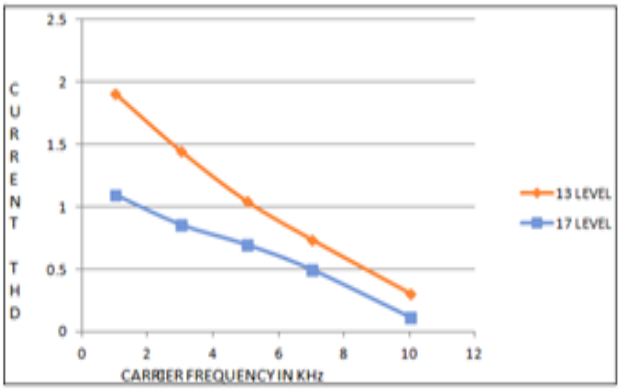

Figure 19. Current THD vs Carrier frequency

It shows with increase of carrier frequencies switching losses increases.

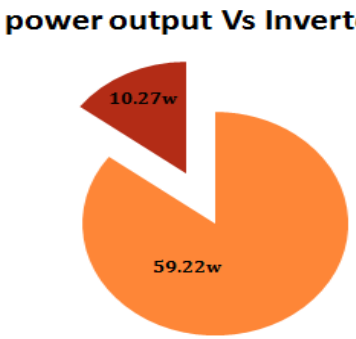

Figure 20. Output power vs inverter loss at 10KHz

CONCLUSION

In this paper, compared to conventional symmetrical and asymmetrical topologies the proposed topology have less number of switches and DC sources .The existing topology has been further modified to second topology in order to achieve higher levels with reduced THD. From simulation it has been observed that with increase in carrier frequencies THD in load current and the inverter efficiency reduces. At the same carrier frequency, the inverter efficiency is more in higher levels. With increase in MI voltage THD reduced significantly.

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