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Low-Power Linear Variable Gain Amplifier

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Abstract

This paper presents a low-power linear variable gain amplifier (VGA). This VGA gains its low-power linear properties with the help of the local feedback auxiliary (LFA) amplifier. The core of this LFA amplifier is based on flipped voltage follower (FVF) circuit. This VGA provides the flexibility to tune its gain with dual tuning voltages. Gain range of 15 dB to 16 dB with maximum bandwidth of 22 MHz can be provided by VGA. It exhibits a maximum power consumption of 74 μW from a supply voltage of 1.2 V. This VGA shows a minimum total harmonic distortion (THD) of −40 dB at input signal of 400 mVpp of 1 MHz. Simulation results based on 90-nm CMOS technology are presented to demonstrate the performance of the proposed VGA.

Keywords: VGA, LFA amplifier; FVF, THD.

INTRODUCTION

A variable gain amplifier (VGA) is an electronic amplifier that varies its gain, depending on control voltage [1, 2, 3]. In the last decade there is an ongoing interest to design low-power linear VGA. This is due to the demand that portable equipment, biomedical devices and several wireless devices are continuously required. There are several techniques to reduce the power consumption of the circuits [4, 5, 6, 7, 8], but still they consume high power more than 0.5 mW. Many techniques have been proposed to enhance the linearity of the differential pair. Most of them are variants of the classic source-degeneration, nonlinearity cancellation, signal attenuation [9, 10] techniques and feedforward linearization [11]. The linearity of these designs degrades drastically at high frequencies. Moreover, high distortion is observed over a large input range as these designs are not well suitable to operate in low-voltage environments. Another linearization technique is to operate input transistor in triode region [12], but disadvantage is it has limited transconductance value and smaller tuning range. A last example of linearization technique is to use pseudo-differential pair transconductor, but it needs an extra common-mode feedforward (CMFF) circuit to improve common mode rejection ratio (CMRR) [13]. So, it is thus necessary to investigate new CMOS amplifier-based VGA structures that further useful for low-power linear design.

In this work it has been concentrated to design a low power, linear VGA. For this purpose, flipped voltage follower (FVF) based VGA design is proposed in this paper. In this proposed design FVF is used to build low-voltage and low-power local feedback auxiliary (LFA) circuit. It also provides good linearity in its voltage transfer characteristics.

This paper is organized as follows: In section two, architecture of proposed VGA is discussed. This section is divided into six subsections: a) Operational Transconductor Amplifier (OTA), b) Flipped Voltage Follower (FVF), c) Gate Driven Gain Boosting Circuit, d) Local Feedback auxiliary (LFA) amplifier, e) Current Mirror OTA, f) Proposed Transconductor, g) VGA implementation. Section three provides the simulation details on this proposed VGA. Section four provides conclusion.

ARCHITECTURE OF PROPOSED DESIGN

Operational Transconductance Amplifier (OTA)

OTA is a voltage to current convertor that means voltage is provided in OTA's input terminal and current is generated in its output terminal. Owing to its fastness and capacitor driving capability, OTA is preferred than OPAMP [14]. The general expression of OTA gain is, $A_V = -g_m r_O$. Where, g_m is transconductance of small signal analysis, r_O is output resistance. OTA has high output and input impedances. The tunability of OTA is provided by its g_m and it is bias dependent. The impedance of its internal nodes is low. The output impedance can be increased by cascode technique but it reduces output signal swing.

In figure 1 presents an OTA. This is an operational transconductance amplifier which consists of an additional gain boosting stage. This additional gain boosting stage forms a negative feedback loop that keeps constant the drain-source voltage of the input transistor regarding of the input voltage, improving linearity [15]. PMOS transistors M_3, M_4 act as

current source load. V_C, V_{CP} are bias voltages. Bias current is I_{CM}. The tunability of this OTA can be achieved by V_{CN}, which controls I_{CM}. Thereby tuning of g_m is achieved as it depends on

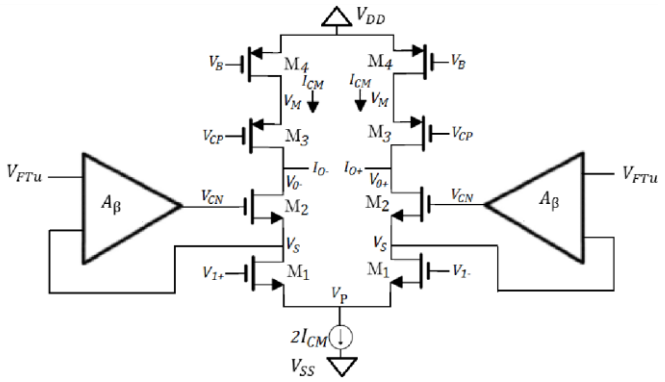

Figure 1: Operational Transconductance Amplifier (OTA)

I_{CM}. The tunability of this OTA can be achieved by V_{CN}, which controls I_{CM}. Thereby tuning of g_m is achieved as it depends on I_{CM}. Input Transistor, M_1 operates at triode region to improve the linearity.

Let V_S drain voltage and V_P source voltage of M_1, V_{O-} drain voltage of M_2 and M_3. For M_1 to operate in triode region; so;

$V_{CN} - V_{tn2} < V_{1+} - V_{tn1} + V_{GS2} - V_{tn2}$; for M_2 operates in saturation; so, $V_{O-} \geq V_{CN} - V_{tn2}$. Assuming M_2 is on edge of saturation,

$$V_{O-} < (V_{1+} - V_{tn1}) + (V_{GS2} - V_{tn2}) \quad \text{(i)}$$

Let V_M drain voltage of M_4 and source voltage of M_3. For M_4 operates in saturation, $V_{CP} + V_{SG3} \leq V_{DD} - V_{SG4} + |V_{tp4}|$. For M_3 operates in saturation, $V_{O-} - |V_{tp3}| \leq V_{CP}$. So,

$$V_{O-} \leq V_{DD} - (V_{SG4} - |V_{tp4}|) - (V_{SG3} - |V_{tp3}|) \quad \text{(ii)}$$

For, $M1$ in triode region,

$I_{CM} = \frac{1}{2} k_{n1}[2(V_{GS1} - V_{tn1})V_{DS1} - V_{DS1}^2]$, $(k_{n1} = \mu_{n1} C_{OX1}(\frac{W}{L})_1$; so $g_{m1} = \frac{dI_{CM}}{d\,V_{GS1}} = k_{n1} V_{DS1}$; $V_{DS1} = V_S - V_P$; so,

$$g_{m1} = k_{n1}(V_S - V_P) \quad \text{(iii)}$$

For, M_2 in saturation region,

$I_{CM} = \frac{1}{2} k_{n2}(V_{GS2} - V_{tn2})^2$, $(k_{n2} = \mu_{n2} C_{OX2}(\frac{W}{L})_2)$; Now, $V_{GS2} = V_{CN} - V_S$; so rewriting eq. (iii);

$$g_{m1} = k_{n1}(V_{CN} - V_P - V_{tn2}) - k_{n1}\sqrt{\frac{2I_{CM}}{k_{n2}}} \quad \text{(iv)}$$

From small signal analysis, OTA gain,

$$A_V = -g_{m1} R_O \quad \text{(v)}$$

Output impedance,

$$R_O = (g_{m2} r_{o1} r_{o2}) \,||\, (g_{m3} r_{o3} r_{o4}) \quad \text{(vi)}$$

Figure 1 is a balanced design. So same conditions will be applicable for V_{O+} also. The eq. (iv) exhibits that tunability of OTA is provided by its g_{m1} and it is bias (I_{CM}) and tuning voltage (V_{CN}) dependent. The other equations provide the operating conditions to keep the input transistors in triode region and other transistors in saturation region.

Flipped Voltage Follower (FVF)

FVF [16] is basically a controlled source follower. To understand FVF easily, source follower configuration is reproduced here for convenience. The main property of a source follower is, its gain is unity. Figure 2a presents a basic PMOS

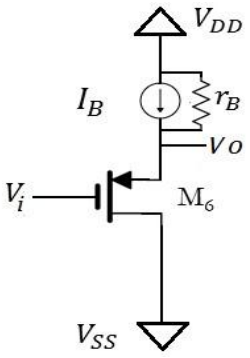

Figure 2a: Source Follower

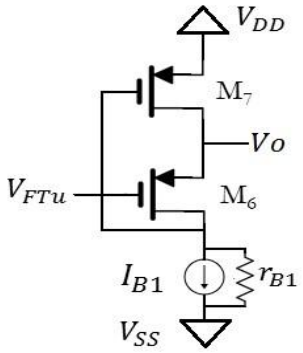

Figure 2b: FVF

source follower. Bias current is I_B. Ignoring body effect output voltage, $V_O = V_i + V_{SG6}$, where V_i is input voltage and V_{SG6} is the source to gate voltage of M_6 transistor. The current through M_6, I_6 is dependent on output current I_O. If I_O varies, I_6 will vary, leads to change in V_{SG6}. Irrespective of V_i, V_O will vary. In presence of large parasitic resistance in output node, V_O will reduce and gain will be less than unity. Source follower gain,

$$A_{SF} = \frac{g_{m6}}{g_{m6} + \frac{1}{r_{O6} \,||\, r_b}} \quad \text{(vii)}$$

r_{O6} is internal resistor of M_6 and r_b is the biasing resistor. $r_{O6} \,||\, r_b \gg 1$. So, ignoring $\frac{1}{r_{O6} \,||\, r_b}$, $A_{SF} \approx 1$. Output resistance,

$$R_{OSF} = \frac{1}{g_{m6}} \quad \text{(viii)}$$

So, to achieve a unity gain, I_6 should be always constant irrespective of I_O variation. It will stabilize V_{SG6}, leads to stable V_O. This purpose is fully achievable by FVF. Figure 2 presents a PMOS FVF. Two transistors M_6, M_7 are connected in cascode position. Input voltage, V_{FTu} is applied to the gate of M_6. Shunt feedback is applied from drain of M_6 to gate of M_7. Bias current I_{B1} is applied to the drain side of M_6. For the presence of shunt feedback, I_6 variation in M_6 can be sensed by M_7. During I_6 variation, M_7 sources required current from V_{DD} to keep I_6 constant irrespective of I_O. Shunt feedback also

creates a very low output impedance. The sourcing capability of FVF is high due to its low output impedance. The sinking capability is limited due to biasing current I_{B1}. FVF gain,

$$A_{FVF} = \frac{g_{m6}}{g_{m6}+\frac{1}{r_{b1}}} \quad \text{(ix)}$$

Where, r_{b1} is the biasing resistor. $r_{b1} \gg 1$. So, ignoring $\frac{1}{r_{b1}}$, $A_{FVF} \approx 1$. Output resistance,

$$R_{OFVF} = \frac{1}{g_{m6}g_{m7}r_{o6}} \quad \text{(x)}$$

Now $r_{b1} > r_{O6} \,||\, r_b$. So, $\frac{1}{r_{b1}} < \frac{1}{r_{b1} \,||\, r_b}$. So $A_{FVF} > A_{SF}$. So FVF provides better linearity than source follower. Also, $R_{OFVF} < R_{OSF}$. Assuming that transistor M_6 is in saturation, the condition of saturation for transistor M_7 is given by,

$$V_{SD7} = V_{DD} - (V_{FTu} + |V_{tp6}| + \sqrt{\frac{2I_{B1}}{k_{p6}}} > \sqrt{\frac{2I_{B1}}{k_{p7}}} \quad \text{(xi)}$$

Assuming that transistor M_7 is in saturation, the condition of saturation for transistor M_6 is given by,

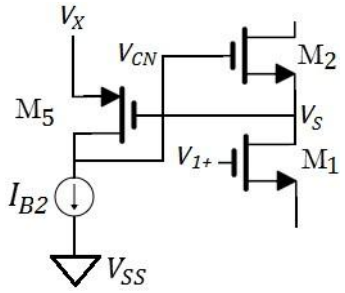

Figure 3: Gate driven gain boosting circuit

$$V_{SG6} - V_{SD6} = V_{DD} - (|V_{tp7}| + \sqrt{\frac{2I_{B1}}{k_{p7}}}) - V_{FTu} < |V_{tp6}| \quad \text{(xii)}$$

Eq. (xi) and (xii) shows that a very low voltage near to that of threshold voltage requires to operate FVF.

Gate Driven Gain Boosting Circuit

Gain boosting technique [17] is a common method to increase gain of a single stage operational amplifier. The gain boosting technique increases gain by boosting the cascode transistor or simply to increase the output impedance of operational transconductance amplifier by an additional gain stage. The effect is the combination of the high unity gain frequency of single stage design with the high dc gain of multistage design.

Figure 3 presents a PMOS gate driven gain boosting circuit. In Figure 3 the M_1, M_2 is the transistor of OTA. The bias current I_{CM} is feed backed from the source of M_2 to the gate of M_5. Again, drain voltage of M_5 is feed backed to gate of M_2. Hence M_2 and M_5 creates a current-voltage negative feedback. This helps OTA to increase its gain by boosting output impedance. Bias current I_{B2} limits the sinking capability of M_5 and helps to stable the feedback voltage.

From Figure 3, $V_{G5} = V_S$; $V_{CN} = V_{G2} = V_{D5}$. let $V_{S5} = V_X$; for operating $M5$ in saturation region; so,

$$V_{CN} \leq V_S + |V_{tp5}| \quad \text{(xiii)}$$

From small signal analysis, $V_{CN} = -g_{m5}(r_{o5} \,||\, R_{B2})\,(V_X - V_S)$; From Figure 1, $V_S = -g_{m1}r_{o1}V_{1+}$; so,

$$V_{CN} = -g_{m5}(r_{o5} \,||\, R_{B2})\,(g_{m1}r_{o1}V_{1+} + V_X) \quad \text{(xiv)}$$

R_{B2} biasing resistor. The boosted output resistance at the drain of $M2$ is approximately,

$$R_{\beta} \approx g_{m2}g_{m5}r_{o1}r_{o2}r_{o5} \quad \text{(xv)}$$

This simple circuit increases DC gain without hampering OTA's high unity gain frequency.

Local Feedback Auxiliary (LFA) Amplifier

The additional gain stage of OTA which is mentioned previous comprises of FVF and gate driven gain boosting circuit. These two circuits together make a LFA amplifier. Figure 4 presents LFA amplifier. The source of M_5 is connected with output of FVF. Individual circuits are discussed in previous subsections. Tuning voltage V_{FTu} of the circuit can be set very low. This allows a large tuning range to be achieved while a low level of distortion in the output current is maintained for a given input

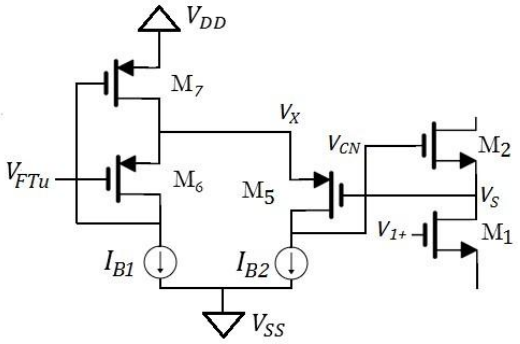

Figure 4: LFA amplifier

voltage range. From Figure 2b and Figure 3, it is obtained that $V_x = V_O$; $A_{FVF} \approx 1$; so $V_x \approx V_{FTu}$; so, rewriting the eq. (xiv),

$$V_{CN} = -g_{m5}(r_{o5} \,||\, R_{B2})\,(g_{m1}r_{o1}V_{1+} + V_{FTu}) \quad \text{(xvi)}$$

This design contains two independent feedback (discussed before) loop. So, it is a two pole feedback loop design. So proper design is required to enforce stability.

Current Mirror OTA

Current mirror OTA is the main building block of today's low power design [18]. Current mirror OTA provides low input impedance, high output impedance, high accuracy of current copy, high linearity, high dynamic range, high output swing, large bandwidth better than conventional OTA. Its main disadvantage is its gain become low than conventional OTA.

Figure 5 presents the current mirror OTA. The OTA structure is same as discussed in previous section. Only the tail current source ($2I_{CM}$ in Figure 1) is replaced with M_8 transistor. Now M_8, M_9, M_{12} and M_{13} forms a simple current mirror. Along with that M_3, M_4, M_9, M_{10} and M_{11} forms a cascode current mirror. Here I_{Tu} is the reference bias current and it is a function of V_{Tu}. So,

$$I_{CM} = \frac{(W/L)_8}{2(W/L)_{12}} I_{Tu} \quad \text{(xvii)}$$

Again, $$I_{CM} = \frac{(W/L)_4}{(W/L)_{11}} \frac{(W/L)_9}{(W/L)_{12}} I_{Tu} \quad \text{(xviii)}$$

Again, $$I_{CM} = \frac{(W/L)_3}{(W/L)_{10}} \frac{(W/L)_9}{(W/L)_{12}} I_{Tu} \quad \text{(xix)}$$

So,

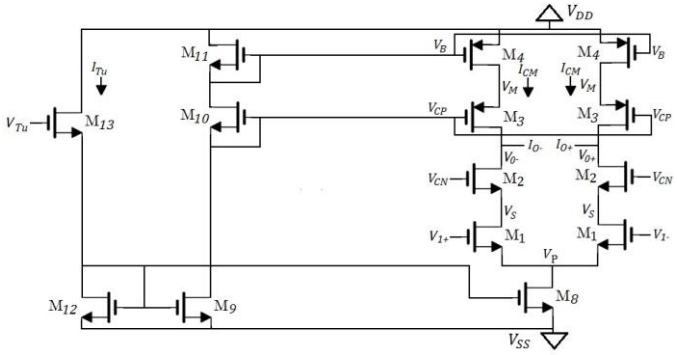

Figure 5: Current Mirror OTA

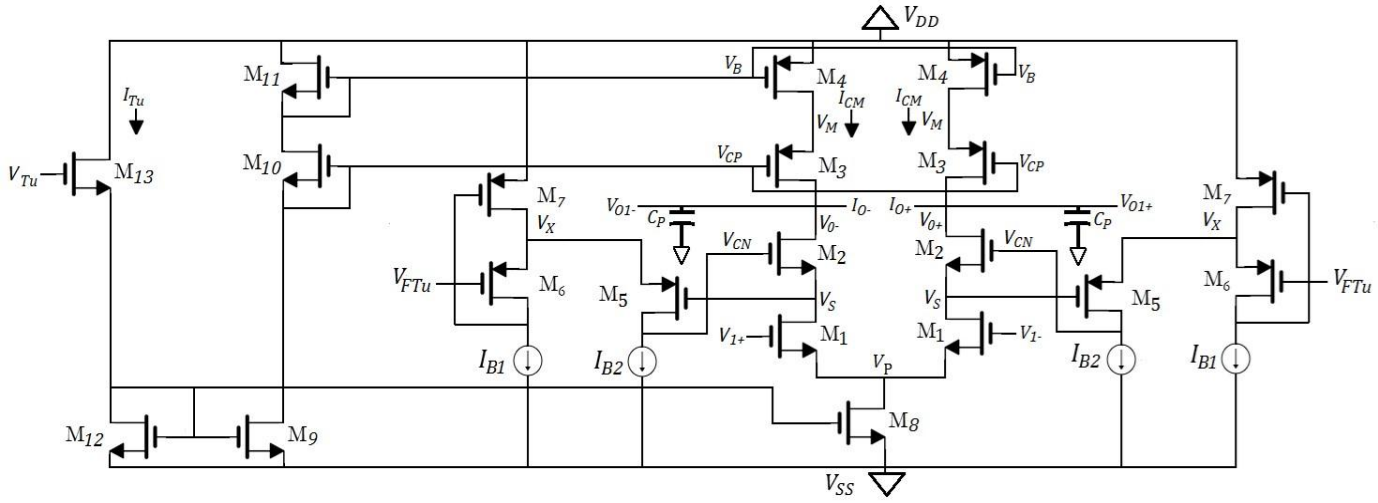

Figure 6: Proposed Transconductor

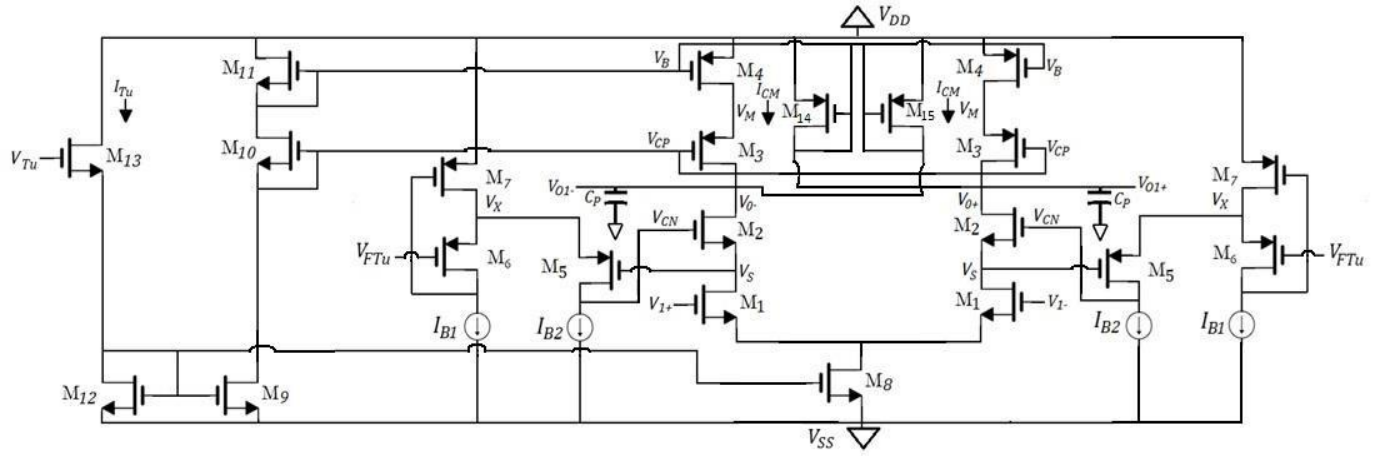

Figure 7: Proposed VGA

$$\frac{(W/L)_8}{2} = \frac{(W/L)_4\ (W/L)_9}{(W/L)_{11}} = \frac{(W/L)_3\ (W/L)_9}{(W/L)_{10}} \quad \text{(xx)}$$

From these equations proper dimensions of transistors can be realized of current mirror and OTA for proper operation.

Proposed Transconductor

All sub-blocks of proposed transconductor have been discussed. Using these sub-blocks, Figure 6 presents the whole structure of transconductor design, which is proposed. Input transistors M_1 operates in triode region and rest transistors operates in saturation region. The tunability of OTA is controlled by g_{m1} which is I_{CM} dependent and I_{CM} is V_{CN} dependent. Control voltage V_{CN} is generated by low-power and highly linear LFA circuit. FVF output V_X is converted into V_{CN}. Tuning voltage V_{FTu}; converts into V_X. The tuning voltage V_{FTu} is very low close to PMOS subthreshold voltage. The bias current I_{CM} is generated by copping reference bias current I_{Tu} of current mirror which is tuning voltage V_{Tu} dependent. So, in a nutshell the tunability of transconductor is depends on two tuning voltages, V_{FTu} and V_{Tu} and low-power and linear properties depend on LFA functionality. From equation (v), $A_V = -g_{m1}R_{CL}$; where, R_{CL} closed loop output impedance; From equation (iv), $g_{m1} = k_{n1}(V_{CN} - V_P - V_{tn2}) - k_{n1}\sqrt{\frac{2I_{CM}}{k_{n2}}}$; $R_{CL} = A_\beta R_O$; From equation (vi), $R_O = (g_{m2}r_{o1}r_{o2}) \parallel (g_{m3}r_{o3}r_{o4})$. A_β is LFA amplifier's gain. From eq. (xiv), $V_{CN} = -g_{m5}(r_{o5} \parallel R_{B2})\ (g_{m1}r_{o1}V_{1+} + V_{FTu})$; From eq. (xvii), $I_{CM} = \frac{(W/L)_8}{2(W/L)_{12}} I_{Tu}$; For, M_{13} in saturation region, $V_{SG13} = V_{DD} - V_{Tu}$; so,

$$I_{Tu} = \frac{1}{2}k_{p13}(V_{DD} - V_{Tu} - |V_{tp13}|)^2 \quad \text{(xxi)}$$

so,

$$A_V = -A_\beta(k_{n1}(-g_{m5}(r_{o5} \parallel R_{B2})\,(g_{m1}r_{o1}V_{1+} + V_{FTu}) - V_P - V_{tn2}) - k_{n1}\sqrt{\frac{\frac{(W/L)_8}{(W/L)_{12}}(\frac{1}{2}k_{p13}(V_{DD} - V_{Tu} - |V_{tp13}|)2)}{k_{n2}}})\,((g_{m2}r_{o1}r_{o2}) \parallel (g_{m3}r_{o3}r_{o4})) \quad \text{(xxii)}$$

So, it is observed that A_V is a function of V_{1+}, V_{Tu} and V_{FTu}. Now V_{1+} is fixed. So, it is a function of only V_{Tu} and V_{FTu}. So, tuning is accomplished by both of V_{Tu} and V_{FTu} tuning voltages.

VGA Implementation

This linear transconductor which is proposed in this paper is very useful to design a VGA. VGA is an essential building block of modern analog design [19]. Figure 7 presents the VGA architecture. This is implemented using proposed transconductor in feedback configuration. Transistors M_{14} and M_{15} are act as feedback resistors. These resistors are switched to implement different gains. This architecture provides fixed deterministic gain.

SIMULATION RESULTS

In this section simulation results of proposed VGA are discussed. The circuit has been realized in a standard 90-nm CMOS process and simulated with CADENCE VIRTUOSO. All circuits have been tested with the supply voltage set to 1.2 V. Table 1 gives the required value of I_{B1}, I_{B2}, V_{Tu} and V_{FTu} for setting the operating conditions and tuning of VGA. This parameters range keep input transistors in triode region and all other transistors in saturation region. Figure 8 presents the gain curves of VGA. The gain of VGA is measured by sweeping the V_{Tu} (tuning) and V_{FTu} (fine tuning) voltages. The gain range is approximately from 15 dB 16 dB. The maximum bandwidth is 22 MHz (0 dB gain). Figure 9 shows the gain and phase curve together which exhibits phase margin is 99. Figure 10 presents the output voltage curve w.r.t to V_{Tu} of VGA. It exhibits the output voltage is proportional to V_{Tu}. Figure 11 presents the output voltage curve w.r.t to V_{FTu} of VGA. It exhibits the output voltage is proportional to V_{FTu}. Figure 12 presents DC characteristics of VGA. The DC characteristics of VGA is measured by sweeping the V_{Tu} (tuning) and V_{FTu} (fine tuning) voltages. Figure 13 and Figure 14 exhibits the HD3 and THD curve of differential input signal of 400 Vpp with varying frequency from 100 KHz to 1 MHz. The THD in 1MHZ is −40 dB. The maximum power consumption is 74 µW. All simulated output results are summarized in Table 2 and comparison of this work with other works are summarized in Table 3.

CONCLUSION

A low power linear VGA has been presented. Proposed VGA utilizes FVF and current mirror OTA for low power purpose and improve linearity. Cascoding technique and gain boosting technique is used in OTA to improve the gain of VGA. It also shows its low noise property. This VGA has a maximum gain of 16 dB with −40 dB linearity. Furthermore, the VGA operates up to 22 MHz frequency. It consumes a total power of 74 µW under supply voltage of 1.2 V.

Table 1: Parameters value

Parameters	Value
I_{B1}	4µ
I_{B2}	20µ
V_{Tu}	713 mV-733 mV
V_{FTu}	174 mV-205 mV
C_P	1 pF

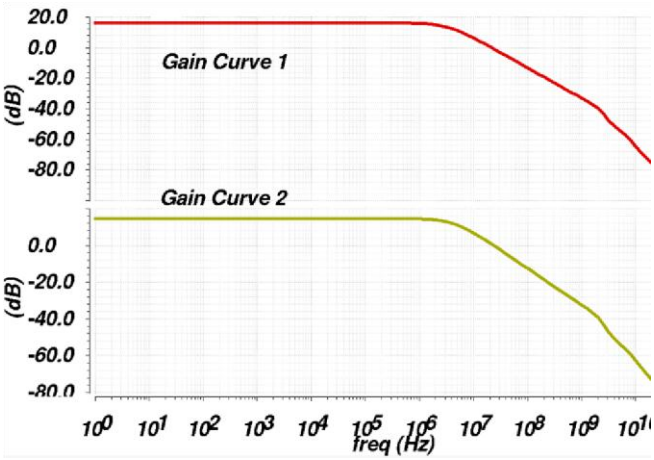

Figure 8: Gain curve

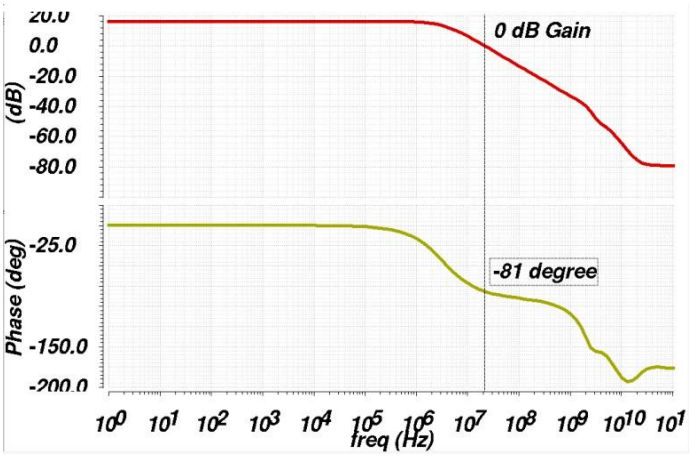

Figure 9: Gain and Phase curve

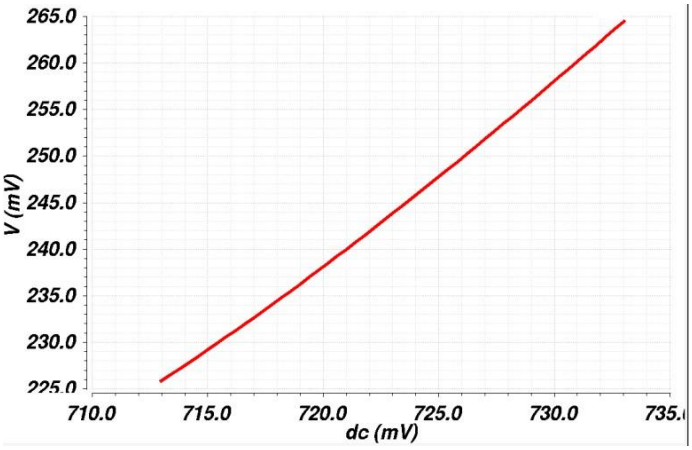

Figure 10: Output Gain vs Tuning (VTu) Voltage

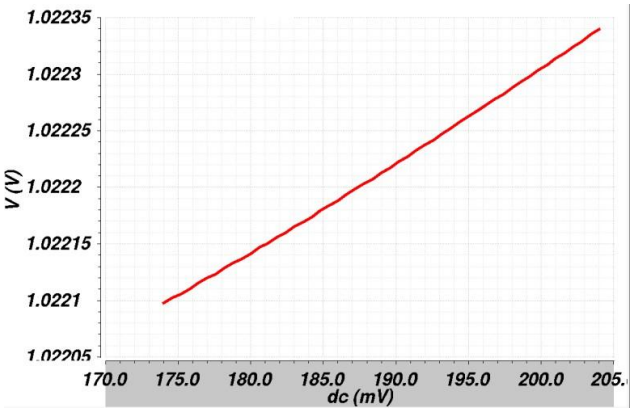

Figure 11: Output Gain vs Fine Tuning ($VFTu$) Voltage

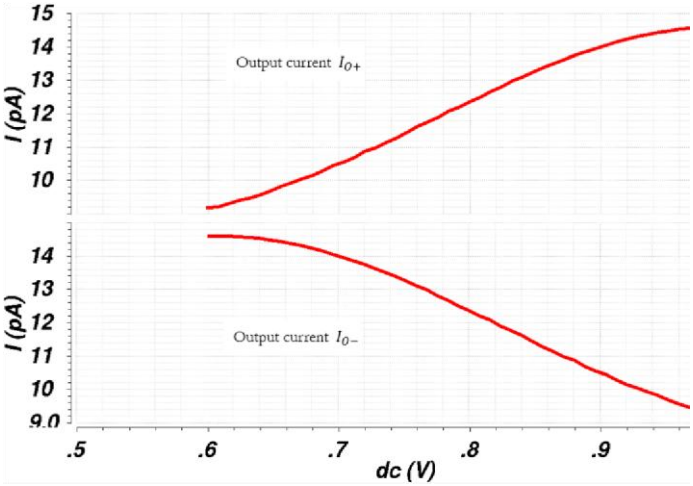

Figure 12: DC characteristics

Table 2: Simulation result of proposed VGA

Output Characteristics	Simulation Values
Gain (dB)	15 to 16
Phase Margin	99^0
Bandwidth (MHz)	22
Linearity (THD, dB)	−40 (400 Vpp at 1 MHz)
Power Consumption (µW)	74
Noise (nV/sqrt (Hz))	53

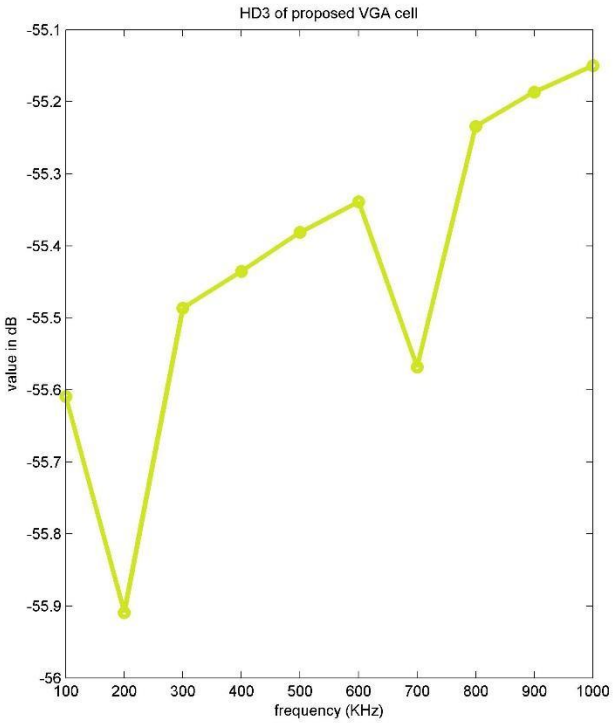

Figure 13: HD3 of proposed VGA

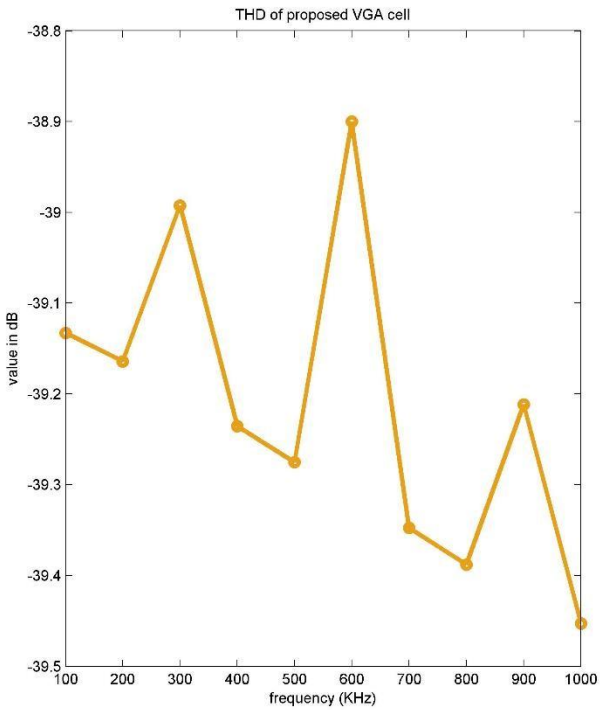

Figure 14: THD of proposed VGA.

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