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AC Analysis of Octree based Buffer Using Various Data Conditioning Flip Flops

Ngangbam Phalguni Singh[1,*], Dr. Ndyetabura Y. Hamisi[1] and Dr. Hashimu Uledi Iddi[2]

[1]Department of Computer Science & Engineering, College of Information and Communication Technology, University of Dar es Salaam, Dar es Salaam – P.O.Box 33335, Tanzania.
[2]Department of Electronics and Telecommunication Engineering, College of Information and Communication Technology, University of Dar es Salaam, Dar es Salaam – P.O.Box 33335, Tanzania.

Orcid ID: 0000-0003-1621-8939

Abstract

This paper presents the AC (Analog Current) analysis of low power buffer using various conditional Flip Flops. The delay buffers are used to reduce the power consumption in Information and Communication Technology (ICT) devices at nano-scale CMOS technology. The power dissipation increases accordingly when the switching function increases in the sequential devices used in various blocks. Switching activities depend on the clock network and clock transitions. Clock slew plays a pivotal role. Octree is employed to reduce the activity of the clock distribution network. The clock distribution is employed with various types of flip flop: Semi-Dynamic Flip Flop (SDFF), Conditional Data Mapping Flip Flop (CDMFF), and Cross Charge Control Flip Flop (XCFF). Distribution of the clock signal is controlled by these flip flops. The clock signal can be used only when necessary; avoiding unnecessary internal capacitor charging if the output remains the same. This will also control the uncertainty in transition time, data/clock slew and logic level. It also minimizes the propagation delay time (t_{pd}) and setup time (t_{su}). This will have direct impact on the reduction of power in the data storage of computer design also. The viability of the design is verified by the simulation using Mutisim with both CMOS realization. Sustainability of the proposed analysis is also supported by the theoretical analysis and comparison.

Keywords: Delay Buffer, ICT, CMOS, Octree, ICT, SDFF, CDMFF, XCFF.

INTRODUCTION

In the past few decades, the AC analysis focuses on the synchronizer Flip Flops. The aim of this paper is to analyze the frequency responses of the data conditioning Flip Flops based on the amplitude and phase. These Flip Flops are used for designing the low power buffer. There are three different delay components for a general synchronous system: (i) the memory storage elements (ii) the logic elements (iii) the clocking circuitry and distribution. This paper focuses on the logic elements (i.e. Flip Flops). The characteristics of the logic elements constrain the design of the clock distribution networks [1].

In most VLSI devices, the clock network and clocked data elements are the main sources of power dissipation. The clocking system and interconnects consumes about 20%-40% of the total system power in a design [2] [3]. In the elements such latches and flip flops, when there are switching activities in their internal capacitance, it results in power dissipation. This may happen with every clock transition/pulse into the sequential element. By increasing the clock interconnection capacitance, the clock voltage swing can be reduced [4]. But the sequential elements can retain their state and their output the same, before and after the clock pulse; when they are expected to change. This contributes in unnecessary dissipation of power due to clock transition. Power dissipation can be minimized by designing the flip flops in such a way that they can gate the clock and use the clock when needed.

There are various synchronizing Flip Flops like D-flip flop, T-flip flop, JK-flip flop and RS-flip flop. These are called as cyclic logic circuits [5]. These can be used in designing the buffer.

But this paper will discuss the AC analysis of the data conditioning Flip Flops such as Semi-Dynamic Flip Flop (SDFF), Conditional Data Mapping Flip Flop (CDMFF), and Cross Charge Control Flip Flop (XCFF).

PROPOSED DATA CONDITIONING FLIP FLOPS

Data conditioning Flip Flops are used to control the clocking and switching systems. These Flip Flops can be any type of the following:

a) Semi-Dynamic Flip Flop (SDFF): This flip flop consists of a hybrid architecture derived from the merits of dynamic and static D-flip flop structures [6]. The conventional diagram is drawn in Figure 1. As the elimination of the delay and area along with one or more logic stages of the flip-flop can be done, the pipeline overhead can be reduced. The SDFF has large clock load as well as the large pre-charge capacitance. Because

of these factors, even though the speed is high, the efficiency is less concerning the power consumption [7]. But the performance of internal precharge structure and a static output are good. It contains dynamic frontend and a static output. The latching operation is possible because of the clock overlapping. The major sources of power dissipation in the conventional semi-dynamic designs include redundant data transitions and large precharge capacitance [6]. It is still best suited for high performance designs, though its power consumption is moderate. The AC analysis is shown in the figure 5 (a) and figure 5 (b).

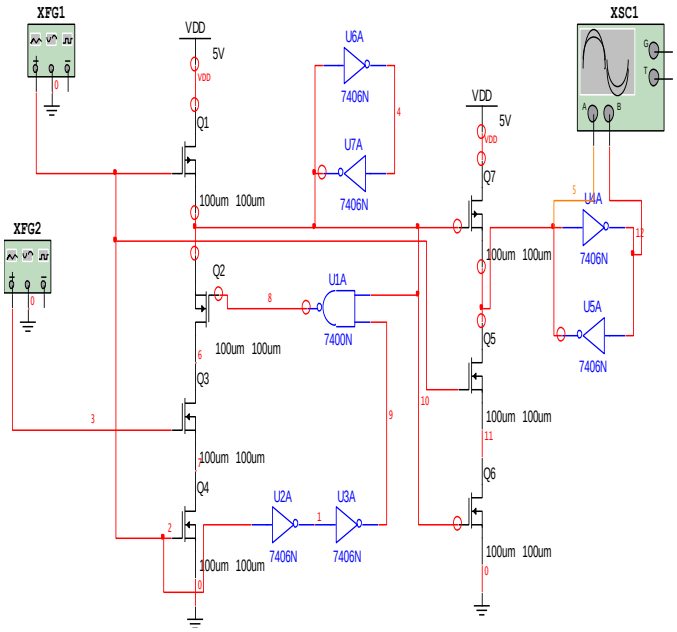


Figure 1: Conventional diagram of SDFF

b) Conditional Data Mapping Flip Flop (CDMFF): A feedback structure is introduced to conditionally feed the data to the flip flop. The diagram is shown in Figure 2. Whenever the redundant event occurs, the unwanted transistors are not triggered [6]. The switching power is reduced by using energy recycling circuit. When there is a low voltage drop, the current flow across devices is restricted. And the energy stored in the capacitors is recycled [2]. The conditional structures in the critical path tends to increase the hold time and the data to output delay of the flip flop. Sometimes it leads to increase in the power dissipation. Large precharge in the capacitors occurs when the pull-up and pull-down transistors are driven by the precharge node at a time. These transistors drive large output loads; contributing more capacitance at the precharge node. The AC analysis is shown in the figure 6 (a) and figure 6 (b).

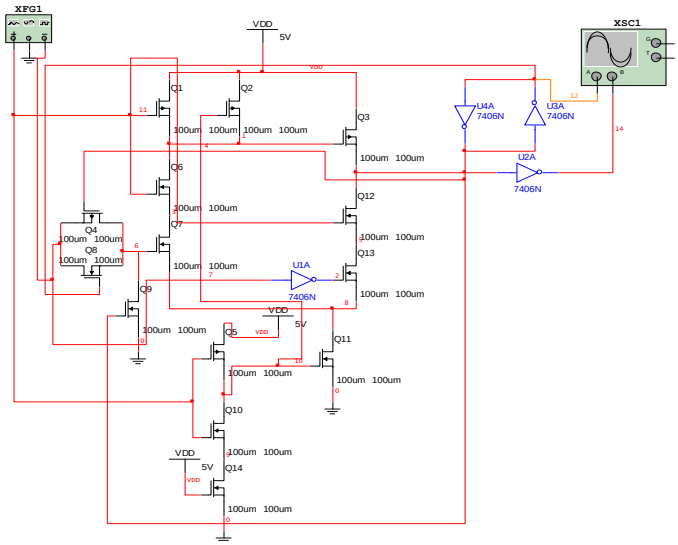


Figure 2: Conventional diagram of CDMFF

c) Cross Charge Control Flip Flop (XCFF):

The pull-up and pull-down transistors are driven at the output side separately. The diagram is shown in Figure 3. There are two dynamic nodes. Only one dynamic node will be switched in one clock cycle; resulting in low power consumption. Without compromising the speed degradation, the clock driving load is reduced. When the complex functions are embedded into the design, the redundant precharge and the effect of charge sharing become uncontrollably large [6]. The AC analysis is shown in the figure 7 (a) and figure 7 (b).

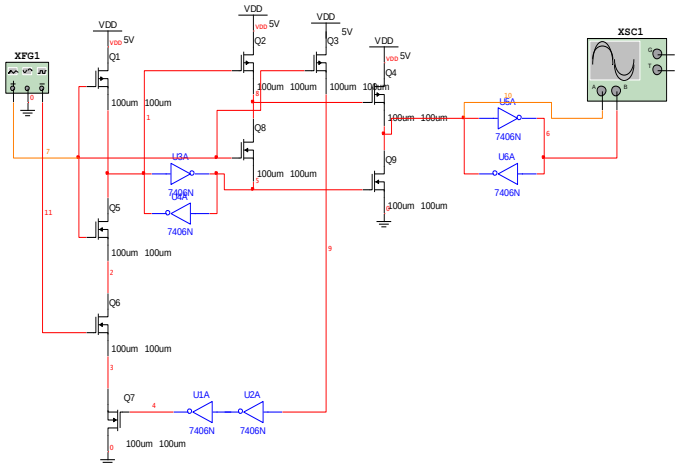
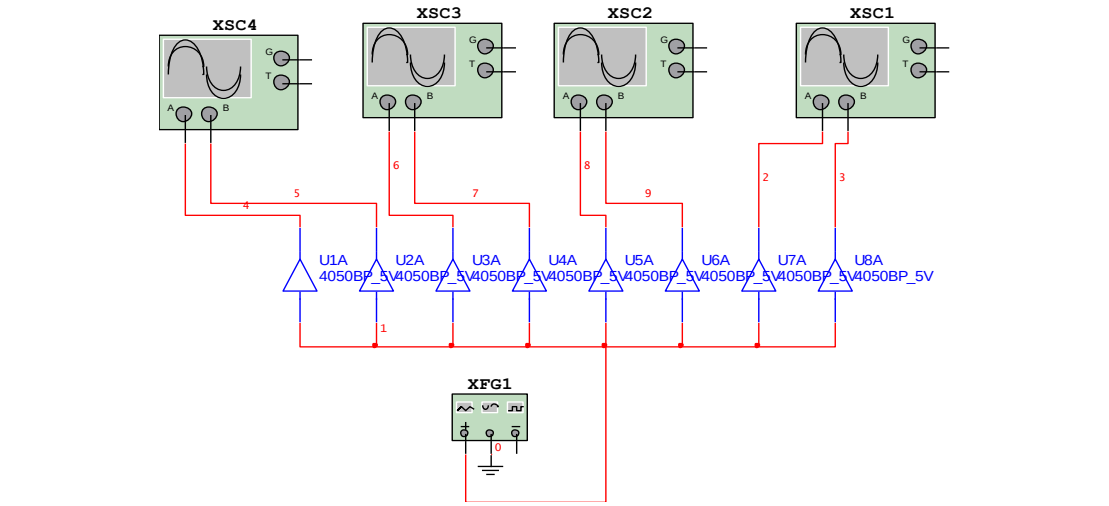
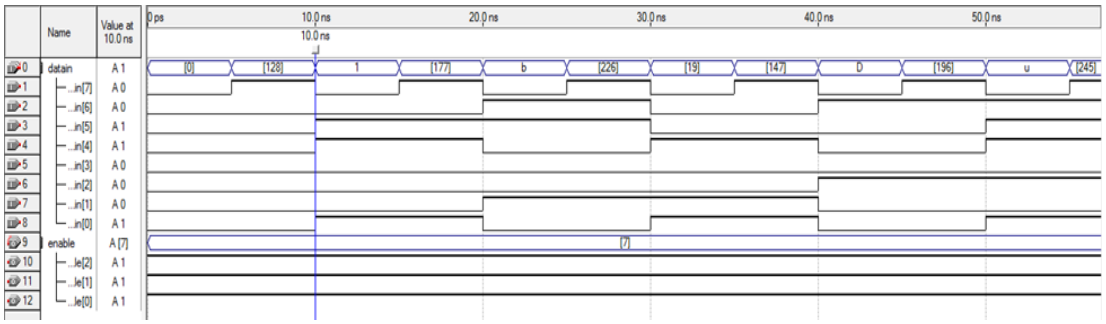


Figure 3: Conventional diagram of XCFF

Clock gating design at RTL is coarse and it often fallouts in large wire length overhead. The circuit is shown in Figure 4 (a) using buffers. The optimization space can be limited in the clock gating if it is considered only at the clock tree synthesis; as the registers can be fixed. The simulation is shown in Figure 4 (b). So an Octree clocking system is introduced with C-element [8] [9].



(a)



(b)

Figure 4: (a) Octree Diagram (b) Octree Simulation

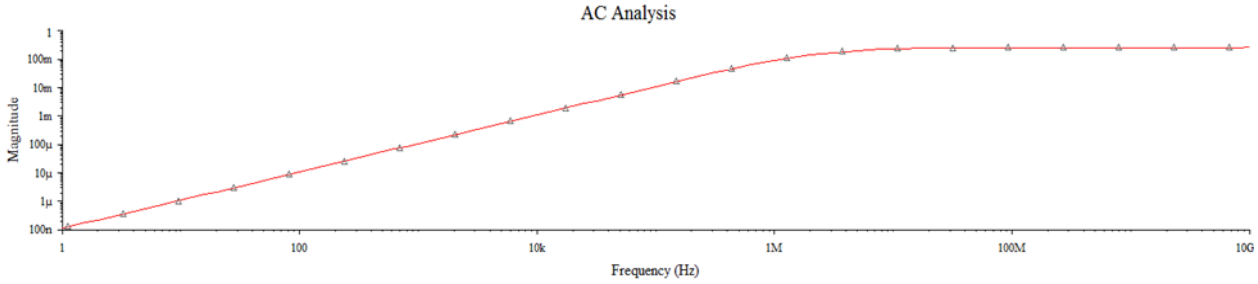
AC ANALYSIS

The frequency response is analyzed with respect to the amplitudes and the phase. The three data conditioning Flip Flops are individually simulated to observe the AC analysis using Multisim software. This analysis will give the quantitative measure of the output spectrum of the Flip Flop. It gives the closed-loop system improved response. The readings are noted and listed in the following table 1.

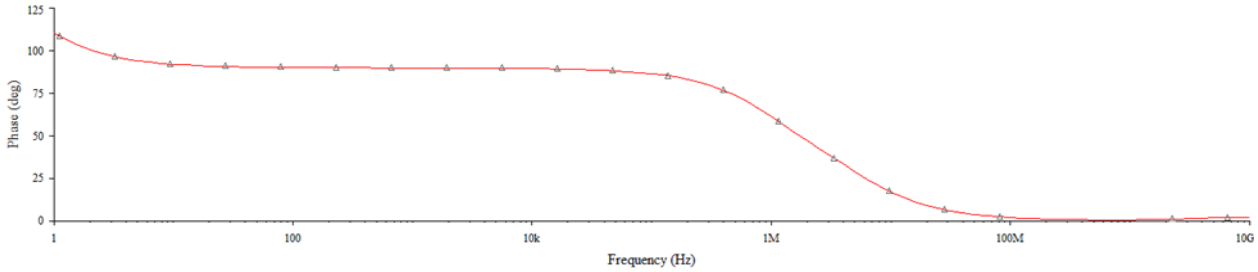
Table 1: AC Analysis and comparison of various Data Conditioning Flip Flops.

SL.NO.	TYPES OF FLIP FLOP	Output Impedance (Ω)	Input Impedance (Ω)	FREQUENCY															
				1 Hz		100 Hz		1 KHz		10 KHz		100 KHz		1 MHz		10 MHz		100 MHz	
				A	P	A	P	A	P	A	P	A	P	A	P	A	P	A	P
1	SDFF	0	87.10563G	1.2E-7	110	1.1E-6	92	1.1E-5	90	0.0001	89	0.0011	89	0.0108	86	0.0904	61	0.23	16
2	CDMFF	0	95.41323G	2.1E-14	92	2.05E-13	90	2.05E-12	89	2.05E-11	89	2.02E-10	80	1.03E-09	31	1.32E-09	-5	6.09E-10	-61
3	XCFF	0	111.26117K	1.19E-07	106	1.12E-06	91	1.12E-05	90	0.0001	90	0.0011	89	0.0011	88	0.1087	72	0.3565	17

A – Amplitude, P – Phase in degree

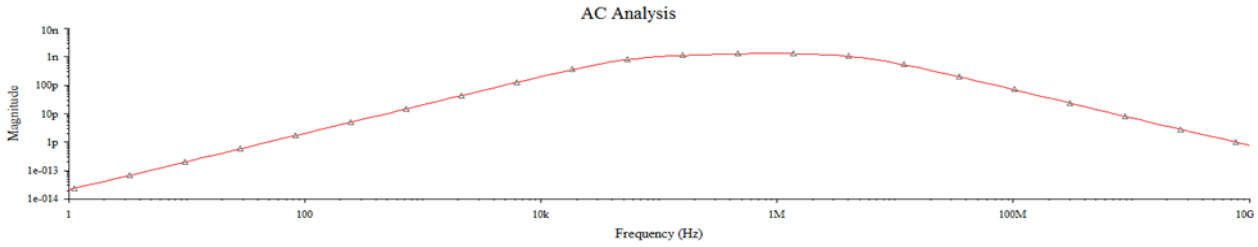


(a)

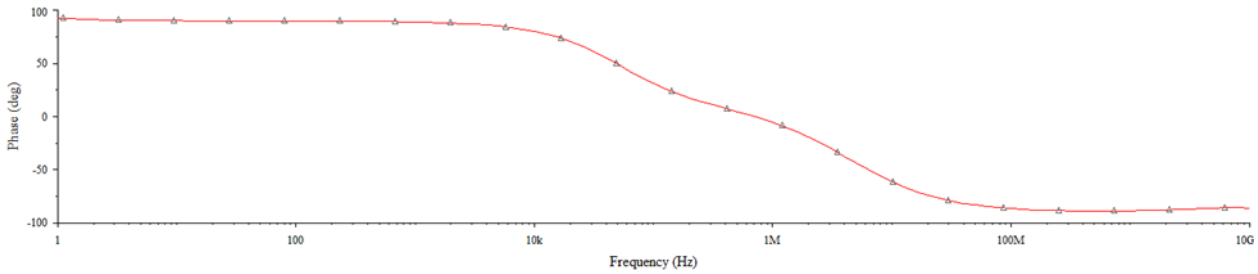


(b)

Figure 5: AC Analysis of SDFF with (a) Amplitude (b) Phase

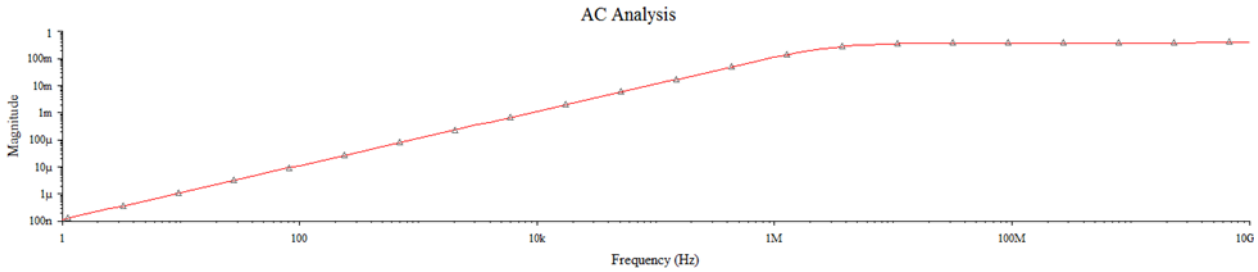


(a)

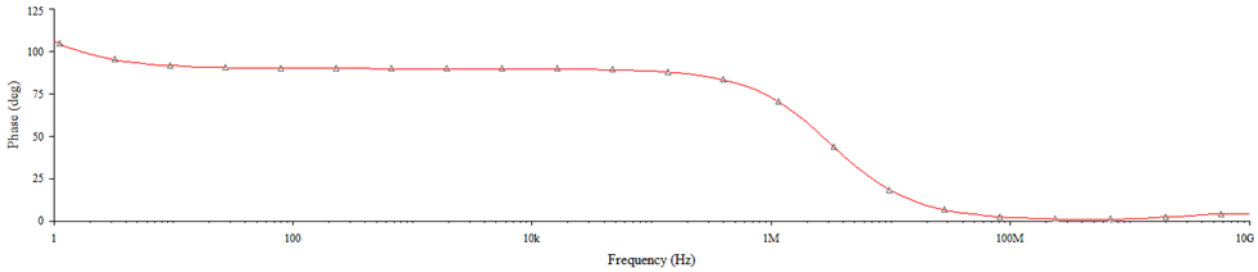


(b)

Figure 6: AC Analysis of CDMFF with (a) Amplitude (b) Phase



(a)



(b)

Figure 7: AC Analysis of XCFF with (a) Amplitude (b) Phase

CONCLUSION

The AC analysis for the Octree based data conditioning Flip Flops are discussed with their respective input impedances. This analysis shows that the excessive data transition can be done without increasing loading on the global clock signal. Octree technique is used to decrease the loading of the input and output data bus. High input impedance and low output impedance are required for low power designs in VLSI Design.

CONFLICT OF ITEREST

The authors declares that there is no conflict of interest regarding the publication of this paper.

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