International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 19 (2017) pp. 8346-8353

DDFF based Low Power Dissipation in Ring Counter using Octree

Mr. Ngangbam Phalguni Singh[1,*], Dr. Ndyetabura Y. Hamisi[1] and Dr. Hashimu Uledi Iddi[2]

[1]Department of Computer Science & Engineering, College of Information and Communication Technology, University of Dar es Salaam, Dar es Salaam – P.O.Box 33335, Tanzania.

[2]Department of Electronics and Telecommunication Engineering, College of Information and Communication Technology, University of Dar es Salaam, Dar es Salaam – P.O.Box 33335, Tanzania.

Orcid ID: 0000-0003-1621-8939

Abstract

This paper presents a low power buffer that offers low power dissipation in Information and Communication Technology (ICT) devices. The design is realized with (Combinational elements) C-Element, gated-clock driver (Octree) and Dual Dynamic node pulsed hybrid Flip Flop (DDFF). Clock Slew is controlled by C-elements. The delay buffers are accessed in the form of Ring Counter. The viability of the design is verified by the simulation using Mutisim, Quartus and Microwind with both CMOS and Cyclone EP1C3T100C6 realization. Sustainability of the proposed design is also supported by the theoretical analysis and comparison. The C-elements are gated with the clock signal to reduce the activity along the clock distribution network. It also reduces the loading of global clock signals thereby reducing the power dissipation. Previously there has been discussion about power dissipation in ICT devices with various Flip Flops and clocking techniques separately. This paper combines these two techniques to further reduce the power dissipation in the ICT devices. The data path is much reduced with the employment of the Octree clocking distribution system. And selection of clock signal is done with the C-element. The clock signal is used only when necessary; avoiding unnecessary internal capacitor charging if the output remains the same.

Keywords: Buffer, Clock slew, (Combinational elements) C-elements, (Information and Communication Technology) ICT, Octree, (Dual Dynamic node pulsed hybrid Flip Flop) DDFF, Ring Counter.

INTRODUCTION

In the past few decades, many researchers are focusing on the power dissipation in the ICT devices. The different delay components for a general synchronous system are: (i) the memory storage elements (ii) the logic elements (iii) the clocking circuitry and distribution. Most of them focus on the first two components. Proper emphasis should be given on the logic elements, the clocking circuitry and distribution.

Nowadays, different types of Flip Flops have been realized using the advantages of conditional selection of the data [1] [2]. This can be done by controlling the switching activities. Also the counter has been designed and proposed to further reduce the power dissipation [2]. There are various Flip Flops like D-flip flop, T-flip flop, JK-flip flop and RS-flip flop, which present output depends on the present inputs, but also on the preceding inputs. These are called as cyclic logic circuits [8]. Various topologies of Flip Flops can be used to control the clock signals in Ring Counter. They are Double Edged Triggered Flip Flop (DETFF), Semi-Dynamic Flip Flop (SDFF), Conditional Data Mapping Flip Flop (CDMFF), Cross Charge Control Flip Flop (XCFF) and Dual Dynamic node pulsed hybrid Flip Flop (DDFF). Most of the papers discussed about the memory storage elements and the logic elements like dual edge triggered [3][4], Flip Flops [2], data mapping [5] and many more. But recently some researchers started focusing in the buffer design and clock distribution like buffer sizing [6] [7], clock network [8] [9], Octree [10] [11], etc.

The aim of this paper is to present a DDFF based low power buffer using Octree. The circuit elements and the clock distribution network are combined to obtain low power dissipation. It can be realized with CMOS and Cyclone EP1C3T100C6. Ring counter is developed using DDFF to control the clocking and switching systems. The clock distribution network is designed based on the characteristics of the logic elements [8]. This network is designed to satisfy the critical timing constrains.

In section 2, power dissipation is explained. Dual Dynamic node pulsed hybrid Flip Flop, C-Element and Octree and Proposed buffer/ring counter using DDFF are explained in section 3, 4 and 5 respectively, followed by conclusion in section 6.

POWER DISSIPATION

In most VLSI devices, the clock network and clocked sequential elements are the main sources of power dissipation [5]. The clocking system and interconnects consume about 20%-

40% of the total system power in a design [12] [13]. In sequential elements such as latches and flip flops, when there are switching activities in their internal capacitance, it results in power dissipation. This may happen with every clock transition/pulse into the sequential element. By increasing the clock interconnection capacitance, the clock voltage swing can be reduced [14]. But sometimes the sequential elements retain their state and their output the same, before and after the clock pulse; when they are expected to change. This contributes in unnecessary dissipation of power due to clock transition. Power dissipation can be minimized by designing the flip flops in such a way that they can gate the clock and use the clock when needed.

There are various factors that decide the power dissipation in buffer design. It is determined by frequency f, supply voltage V, data activity α, capacitance C, leakage, and short circuit current [5]. The following equation can be considered:

$$P = P_{dynamic} + P_{short\ circuit} + P_{leakage} \quad (1)$$

The dynamic power is also known as switching power loss. The short circuit power is due to the finite rise and fall time of input signals. It keeps both the pull up and pull down networks to be ON for a short while. Power Leakage occurs when the threshold voltage decreases to maintain the performance as the supply voltage scales down.

$$P_{dynamic} = \alpha f C V^2 \quad (2)$$

$$P_{short\ circuit} = I_{short\ circuit}\, V_{dd} \quad (3)$$

$$P_{leakage} = I_{leakage}\, V_{dd} \quad (4)$$

Octree clock distribution technique is used in this design. Octree distribution network will activate only those drivers along the path leading to the addressed memory word. Thus the power wastage in drivers can be eliminated with this technique [10].

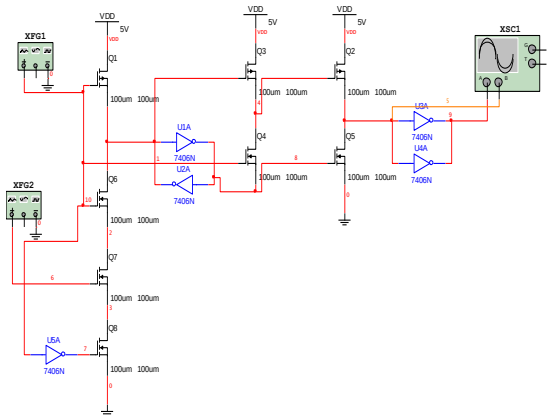
Octree system is used to distribute the main clock signal to other eight distribution paths every cycle. If the output of Ring Counter remains unchanged, unnecessary charging of the internal capacitor can be avoided by using the Flip Flops.

Switching activities depend on the clock network, and clock transitions while triggering the Flip Flops deployed. DETFF is triggered by using both the positive and negative edges of a clock pulse. Double clock edge triggering method reduces the power by decreasing frequency f in equation (2). The conventional way of designing DETFFs is to duplicate the latch part of the single edge flip-flop to achieve sampling input data at both clock edges [10] [13] [11]. The SDFF has large clock load as well as the large pre-charge capacitance. Because of these factors, even though the speed is high, the efficiency is less concerning the power consumption [2] [11]. But the performance of internal precharge structure and a static output are good. It contains dynamic frontend and a static output. A feedback structure is introduced to conditionally feed the data to CDMFF. Whenever the redundant event occurs, the unwanted transistors are not triggered [1]. There are two dynamic nodes in XCFF. Only one dynamic node will be switched in one clock cycle; resulting in low power consumption. Without compromising the speed degradation, the clock driving load is reduced. When the complex functions are embedded into the design, the redundant precharge and the effect of charge sharing become uncontrollably large [1].

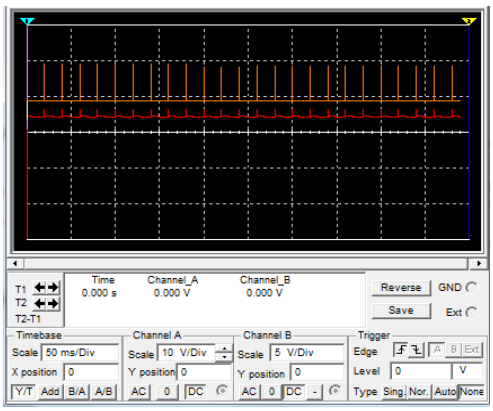
From the above Flip Flops, DDFF is best suited for designing the low power buffer.

DUAL DYNAMIC NODE PULSED HYBRID FLIP FLOP (DDFF)

There are two types of operation: Evaluation Phase (when clock is high) and Precharge Phase (when clock is low). DDFF eliminates the unwanted transitions resulting when the input data is stable at zero. It also represents speed, power efficient method to reduce the pipeline overhead. Instead of selecting the conditional node, it has the unconditionally shut off mechanism and provide the clock signal only when it is required [2]. The simulation is as shown in figure 1 (b). The power dissipation is 1.655 nW. Transmission gate based Flip Flop can be used to further reduce the power dissipation [16].



(a)



(b)

Figure 1: (a) Conventional diagram of DDFF (b) Waveform of DDFF

C-ELEMENT AND OCTREE

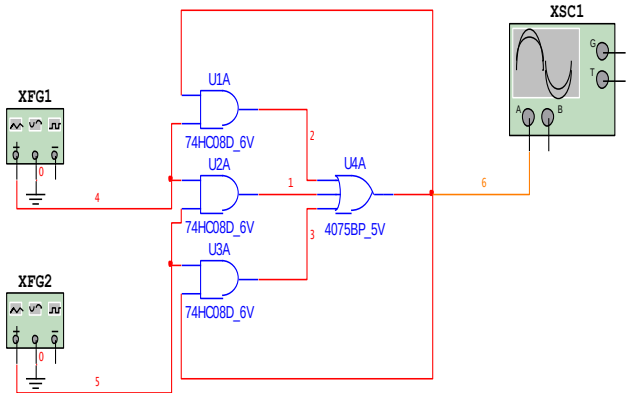
The C-element is used to reduce the excessive clock loading with handshaking protocol. The logic express for C-element is given by:

$$C_{next} = AB + BC + CA \quad (5)$$

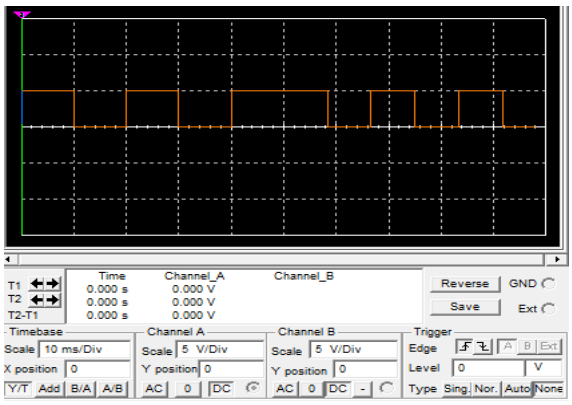
Where A as well as B are its two inputs and C_{next} as well as C are the next and current outputs. If A = B, then the next output will be the same as A. Otherwise it remains unchanged.

When the input of the last DDFF in the previous block changes to —1 making both two inputs of the C-element the same, the clock signal in the current block will be turned on. When the output of the first DDFF in the current block is asserted, then both inputs of the C-element in the previous block go to —0 and the clock for the previous block is disabled [10]. The output of C-element can only be changed when it can avoid the possibility of glitches, a crucial property for a clock gating signal. Figure 2 (b) shows the simulation of C-Element.

The clock signal can be connected to the gates of NMOS transistors or to inverters using the VL supply to reduce this loss [13]. Short circuit current loss occurs due to incomplete turned off of PMOS transistors. This gating function, used to turn off the clock to some of the functional module for some extended period of time, is called as C-element.



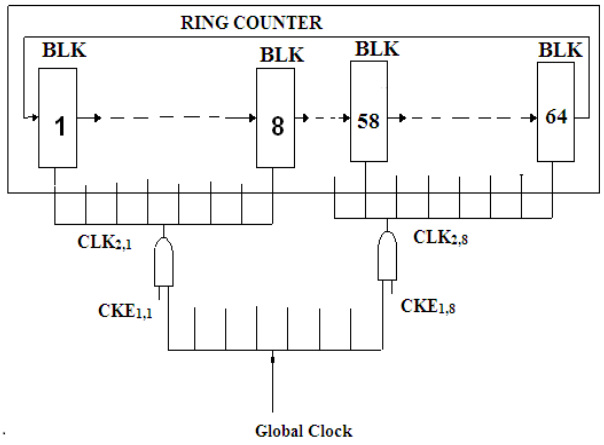
(a)



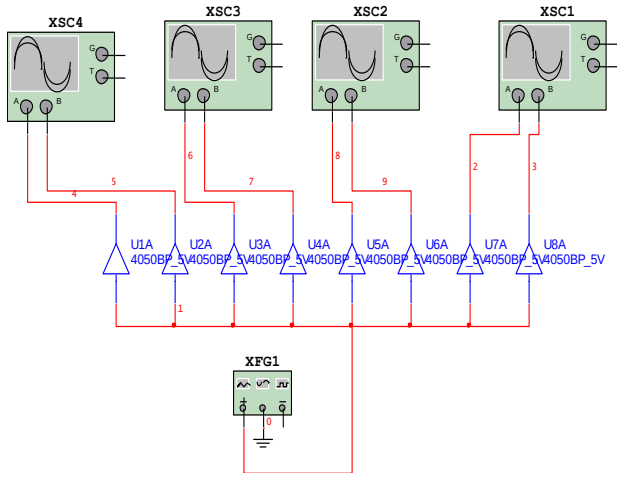
(b)

Figure 2: (a) C-Element Diagram (b) C-Element Simulation

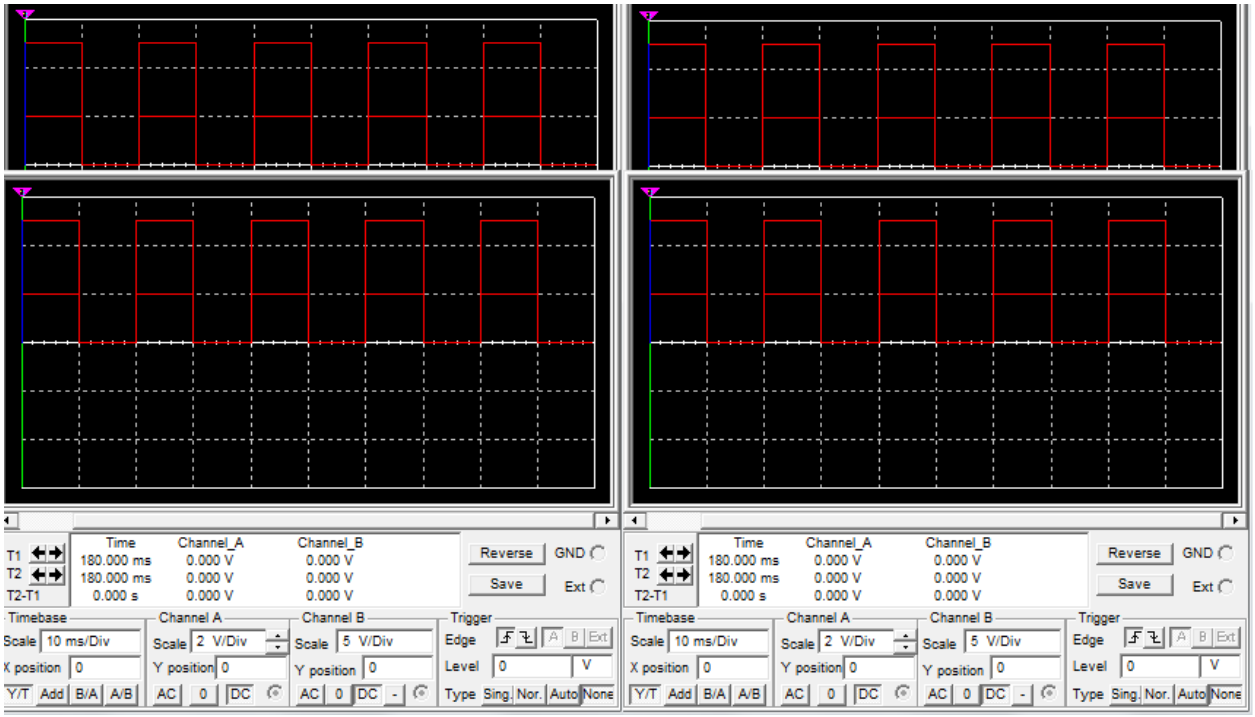
Clock gating is the widely used technique to reduce clock tree power. Most of the previous works are restricted to either Register Transfer Level (RTL) or clock tree synthesis stage [21]. Clock gating design at RTL is coarse and it often fallouts in large wire length overhead. The optimization space can be limited in the clock gating if it is considered only at the clock tree synthesis; as the registers can be fixed. So an Octree clocking system is introduced with C-element [10]. Figure 3 (a) shows a clock gating tree structure using Octree for 64 blocks as example. Figure 3 (b) shows the connection to eight blocks using Octree. Figure 3 (c) shows the simulation of the circuit for eight blocks showing the clock signals in each block. All the signals are synchronized as per the main global clock. Sixty four blocks ($64 = 8^2$) can be triggered with only two clock cycles and minimum clock path. Since the clock cycle and clock path are reduced, the power dissipation is also reduced. A large portion of the dynamic power dissipation typically comes from toggling the clock node [14]. Figure 3 (d) shows the Octree simulation controlled by C-Elements.



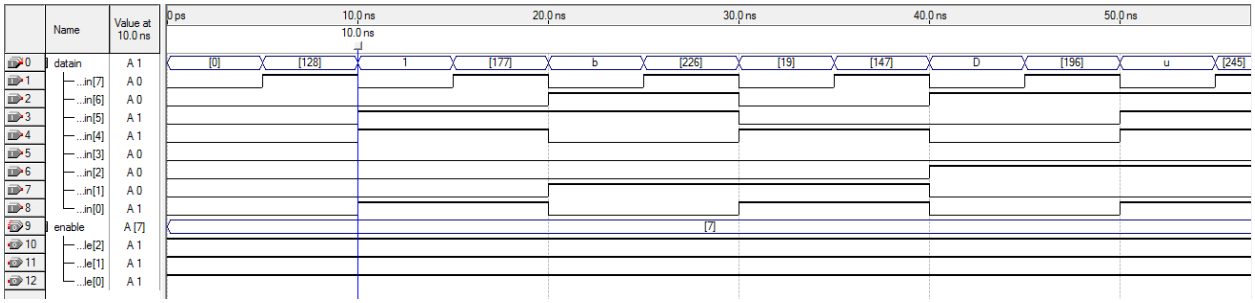
(a)



(b)



(c)



(d)

Figure 3: (a) Block diagram of Octree (b) Octree Diagram (c) Octree Simulation (d) Overall Simulation of Octree

The generation of a clock tree topology minimizes the uncertainty of the clock signal delay to the most critical data paths [22].

PROPOSED BUFFER/RING COUNTER USING DDFF

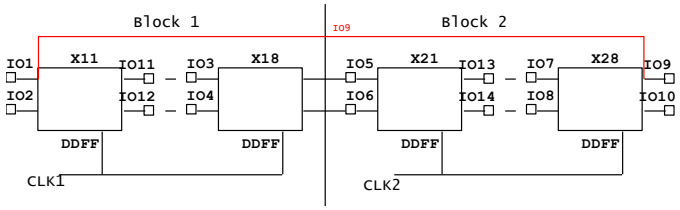
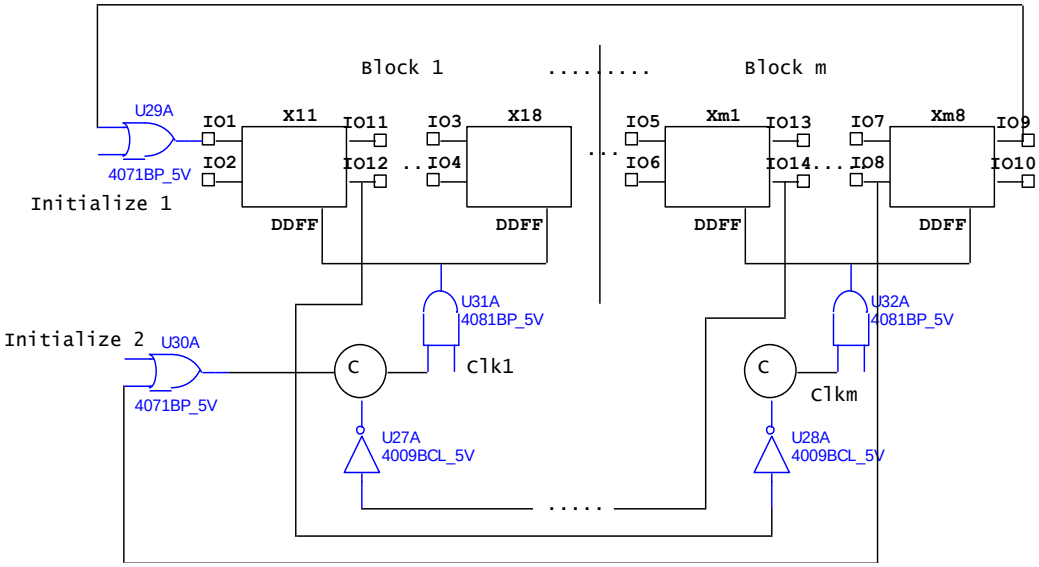
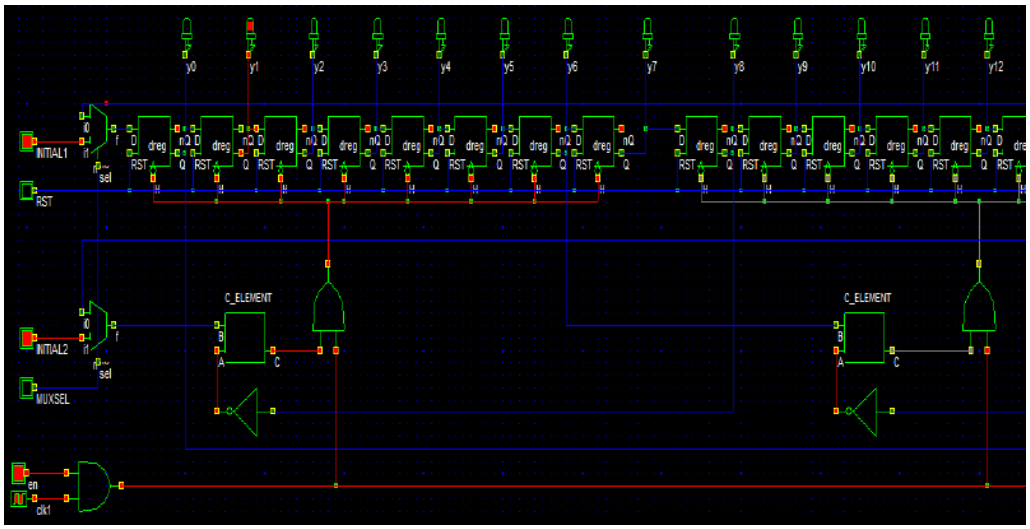


Figure 4: Block Diagram of Ring Counter using DDFF

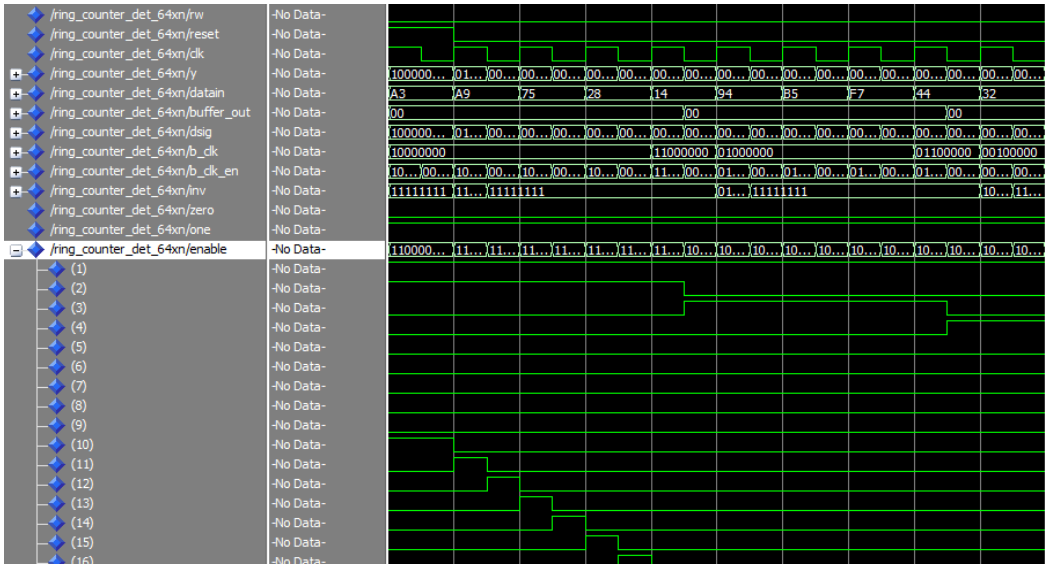
Some functional blocks containing flip flops may be idle for some period [17]. DDFF can be connected to design a Ring Counter as shown in figure 4. In each block, there can be eight DDFFs triggered by a global clock signal. There can be ***m*** number of blocks as in figure 5 (a). In the ring counter, DDFFs are utilized to reduce the operating frequency and the C-element gated-clock strategy is proposed [18]. A novel gated-clock-driver tree is then applied to further reduce the activity along the clock distribution network. The Octree clocking system is employed to reduce the length of clock path. CMOS analog buffer with high output drivability allows very compact, low-power analog voltage buffer with wide bandwidth and high slew rate [19]. Counter can be used for address generation since the memory words are accessed sequentially [20]. The schematic diagram is shown in figure 5 (b). Figure 5 (c) and 5 (d) show the simulation for input enable and buffer.


Block 1
Block m
U29A
4071BP_5V
Initialize 1
IO1
IO2
X11
IO11
IO12
IO3
IO4
X18
IO5
IO6
Xm1
IO13
IO14
IO7
IO8
Xm8
IO9
IO10
DDFF
U31A
4081BP_5V
U32A
4081BP_5V
Initialize 2
U30A
4071BP_5V
C
Clk1
Clkm
U27A
4009BCL_5V
U28A
4009BCL_5V

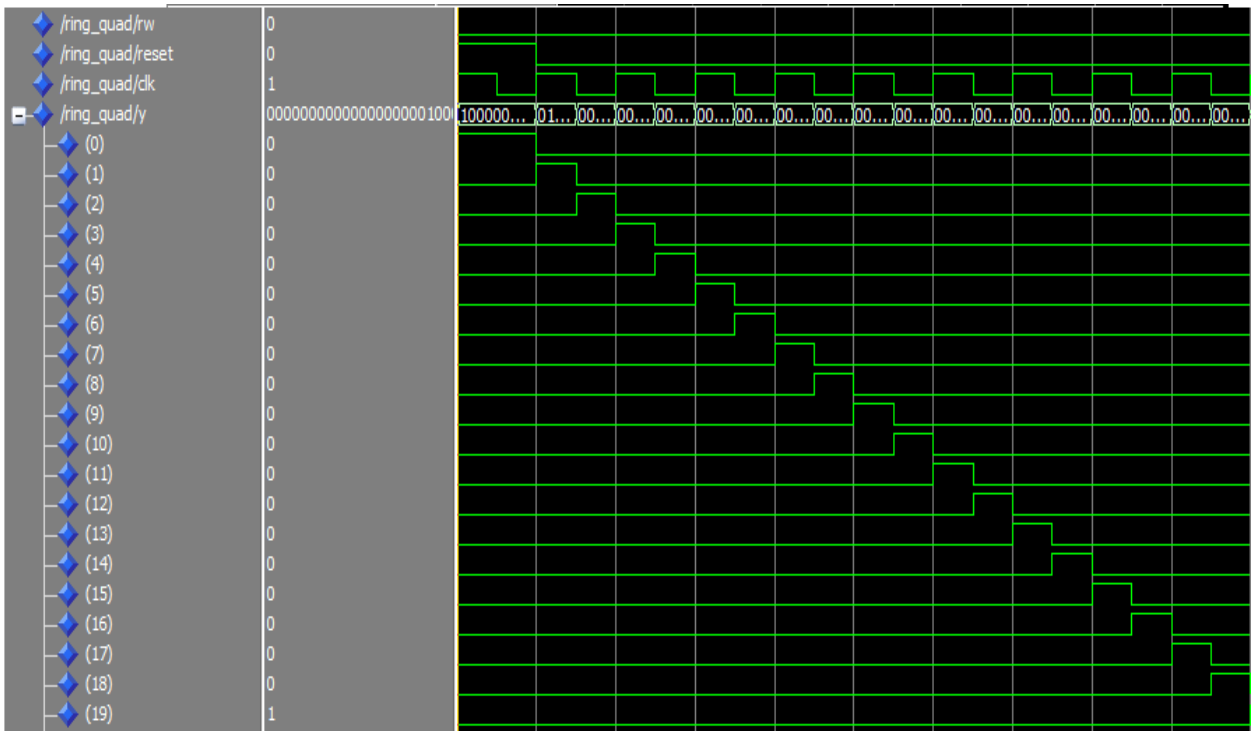
(a)


INITIAL1
RST
INITIAL2
MUXSEL
C_ELEMENT
C_ELEMENT

(b)


/ring_counter_det_64xn/rw
/ring_counter_det_64xn/reset
/ring_counter_det_64xn/clk
/ring_counter_det_64xn/y
/ring_counter_det_64xn/datain
/ring_counter_det_64xn/buffer_out
/ring_counter_det_64xn/dsig
/ring_counter_det_64xn/b_clk
/ring_counter_det_64xn/b_clk_en
/ring_counter_det_64xn/inv
/ring_counter_det_64xn/zero
/ring_counter_det_64xn/one
/ring_counter_det_64xn/enable
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)
(14)
(15)
-No Data-

(c)



(d)

Figure 5: (a) Block diagram of Buffer with Octree gated by C-Element (b) Schematic of Buffer (c) Simulation of Input Enable (d) Simulation of Buffer

Flip Flops have their respective clock driving power and corresponding power dissipation. The comparison table and graph are given below:

Table 1: Comparison of power dissipation

Types of flip flop	Number of transistors	Maximum Power Dissipation (nW)	Clock Driving Power (µW)
DETFF	33	3.3	35
SDFF	23	2.088	27
CDMFF	22	4.290	6
XCFF	21	1.919	7
DDFF	18	1.655	5

In the figure 6, the DETFF has the highest power dissipation with maximum number of transistors. If the number of transistor is more, the switching activities are also higher. So the power dissipation is high. Whereas in DDFF, the number of transistor is less and correspondingly the power dissipation is reduced with minimum clock driving power.

The comparison graph with the above parameters are given below:

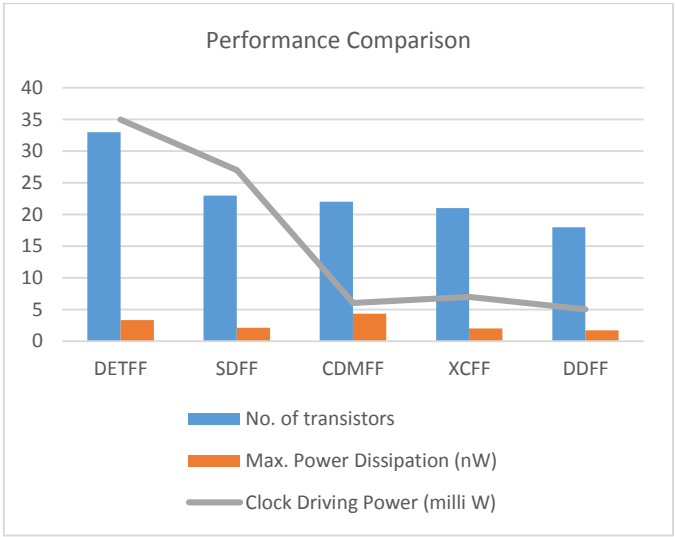


Figure 6: Comparison graph of performances of Flip Flops

CONCLUSION

A system using Octree technique to design a low power buffer is studied and analyzed by using DDFF. The ring counter/buffer with enhancement techniques can effectively reduce the excessive data transition without increasing loading

on the global clock signal. Octree technique is used to decrease the loading of the input and output data bus. The minimum power dissipation is given by DDFF as shown by the experiment results. Thus the dissipation is reduced with the proposed design.

Conflict of Interest:

The authors declare there is no conflict of interest with the publication of this paper.

REFERENCES

[1] M. Akila (2014) "A Novel Analysis on Low-Power High- Performance Flip-Flops," 90(16), pp. 32–37.

[2] R. S. Dharshini (2014), "The Energy Efficient Dual Dynamic Node Pulsed Hybrid Flip-Flop Featuring Dual Mode Logic And Clock Gating," in *National Conference on Information Processing & Remote Computing*, pp. 1–7.

[3] D. Bhargavaram and M. G. K. Pillai (2012), "Low power dual edge triggered flip-flop," in *2012 International Conference on Advances in Engineering, Science and Management (ICAESM)*, pp. 63–67.

[4] R. Hossain, L. D. Wronski, and A. Albicki (1994), "Low power design using double edge triggered flip-flops," *IEEE Trans. Very Large Scale Integr. Syst.*, 2(2).

[5] K. Jindal and V. K. Pandey (2013), "Design of Conditional Data Mapping Flip-Flop for Low Power Applications," *Int. J. Sci. Mod. Eng.*, 1(5), pp. 72–75.

[6] C. J. Alpert, A. Devgan, and S. T. Quay (1999), "Buffer insertion with accurate gate and interconnect delay computation," *Proc. Des. Autom. Conf. (Cat. No. 99CH36361)*.

[7] M. K. Hani and N. Shaikh-Husin (2008), "Simultaneous routing and buffer insertion algorithm for interconnect delay optimization in VLSI layout design," in *Proceedings of the International Conference on Microelectronics, ICM*, pp. 175–178.

[8] E. G. Friedman (1993), "Clock distribution design in VLSI circuits-An overview," *1993 IEEE Int. Symp. Circuits Syst.*.

[9] D. Grunwald, C. B. Morrey, P. Levis, M. Neufeld, and K. I. Farkas (2000), "Policies for dynamic clock scheduling," in *OSDI'00: Proceedings of the 4th conference on Symposium on Operating System Design & Implementation*, p. 6.

[10] E. Kanniga, N. I. Singh, and K. S. R. Rathnam (2013), "Gated-Demultiplexer Tree Buffer for Low," *Int. J. Adv. Res. Electr. Electron. Instrum. Eng.*, 2(10), pp. 4652–4659.

[11] Ngangbam Phalguni Singh, (L) Richard Hans Mgaya, Ndyetabura Y. Hamisi (2016), "OCTREE BASED LOW POWER BUFFER USING DETFF AND SDFF," in *Proceedings of the 4 th International Conference on Mechanical and Industrial Engineering MIE ' 2016 HARNESSING NATURAL RESOURCES FOR SUSTAINABLE INDUSTRIAL*, pp. 162–165.

[12] R. Nithyalakshmi, P. S. Rajamani, P. G. V. Design, and K. S. R. C. Engineering (2013), "Power Efficient Counter Design Using Conditional Pulse Enhancement Flip-Flop," ,2(2), pp. 447–452.

[13] P. Zhao, J. McNeely, P. Golconda, M. A. Bayoumi, R. A. Barcenas, and W. Kuang (2007), "Low-power clock branch sharing double-edge triggered flip-flop," *IEEE Trans. Very Large Scale Integr. Syst.*, 15(3), pp. 338–345.

[14] V. S. Sathe, J. C. Kao, and M. C. Papaefthymiou (2008), "Resonant-clock latch-based design," in *IEEE Journal of Solid-State Circuits*, 43(4), pp. 864–872.

[15] N. Karthika and S. Jayanthy (2014), "Design of Hybrid Pulsed FlipFlop Featuring Embedded logic," *IOSR J. VLSI Signal Process.*, 4(2), pp. 68–74.

[16] X. Wang and W. H. Robinson (2010), "A low-power double edge-triggered flip-flop with transmission gates and clock gating," in *Midwest Symposium on Circuits and Systems*, pp. 205–208.

[17] P. C. Hsieh, J. S. Jhuang, P. Y. Tsai, and T. D. Chiueh (2009), "A low-power delay buffer using gated driver tree," *IEEE Trans. Very Large Scale Integr. Syst.*, 17(9), pp. 1212–1219.

[18] C. C. Yu (2007), "Design of low-power double edge-triggered flip-flop circuit," in *ICIEA 2007: Second IEEE Conference on Industrial Electronics and Applications*, pp. 2054–2057.

[19] C. Sawigun, J. Mahattanakul, A. Demosthenous, and D. Pa (2008), "A low-power CMOS analog voltage buffer using compact adaptive biasing," in *European Conference on Circuit Theory and Design 2007, ECCTD 2007*, pp. 1–4.

[20] S. A. Tawfik and V. Kursun (2007), "Buffer insertion and sizing in clock distribution networks with gradual transition time relaxation for reduced power consumption," in *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems*, pp. 845–848.

[21] W. Shen, Y. Cai, X. Hong, and J. Hu (2010), "An effective gated clock tree design based on activity and

register aware placement," *IEEE Trans. Very Large Scale Integr. Syst.*, 18(12), pp. 1639–1648.

[22] D. Velenis, M. C. Papaefthymiou, and E. G. Friedman (2003), "Reduced delay uncertainty in high performance clock distribution networks," in *Proceedings -Design, Automation and Test in Europe, DATE*, pp. 68–73.