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Design of Adders with Less number of Transistor

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Abstract

A brief evaluation of the various parameters associated with adders with minimum number of transistors in the Very Large Scale Integrated Circuit (VLSI) technology is studied in this paper and their analysis is carried out in a very lucid manner. Minimization of the chip area as well the increase in the number of transistors per area has been increasing rapidly in recent years, this has led us to go for various implementations of logic to match the trade-offs between power utilization, voltage scalability and time delay. The adders that are implemented in this research are named as 10T and 14T adders. These adders are simulated using the *"electric vlsi cad software"* in deep submicron technology node and the results are compared in terms of power dissipation and time delay.

As deep submicron technologies are known to experience increasingly larger variations in process parameters, their impact on the performance of the two proposed adders is studied. The different technology nodes are extracted from the Predictive Technology Model (PTM) and the respective delays are calculated for the adders.

Keywords: CMOS, Adders, Deep Submicron Process, Threshold Voltage, Power, Delay, Nano scale,Power Dissipation

INTRODUCTION

A world without electronics is out of imagination in the present generation. We are so dependent on technology that it has encompassed our regular work basis so much that it is unthinkable to separate ourselves from it. Every day in our life we use a different electronic devices to make our life much more sophisticated. On the whole, we are very much dependent on electronics as it sophisticates our everyday life. For instance, the development of cellular telephones has reformed the world of communication. The mobile phone was acquainted with the general population in 1993, with included options like: texting, GUI etc. Touch screen technology was introduced which was quick to replace the old customary buttons However a steep rise in the usage of these devices has been observed from the past decade [1]. As indicated by a late study, a mammoth 5.92 billion people out of 7.4 billion of the total world's populace uses the cellular telephone [3]. A lot of research and development is going on today to make electronic devices much more robust and smaller. Imagining the world without technology is out of the question today.

The frequent applications of Digital Signal Processing (DSP) can be found in computers, wireless devices, home automation systems etc. However it is implemented with a processor called as the Digital Signal Processor. The DSP chip is programmable chip which allows us to incorporate various algorithms in the form of instructions in it. The adder is the most basic part of the DSP chip. Technological advancements in the recent years led us to shift from high power to low power, low speed to high speed, more area to less area, figure 1 below shows the variation of supply and threshold voltages with different technology nodes is shown below.

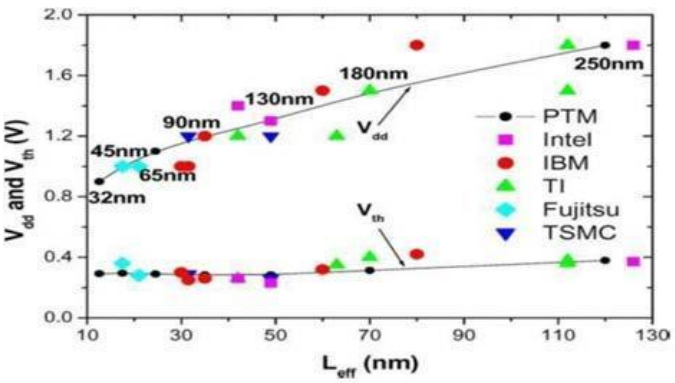
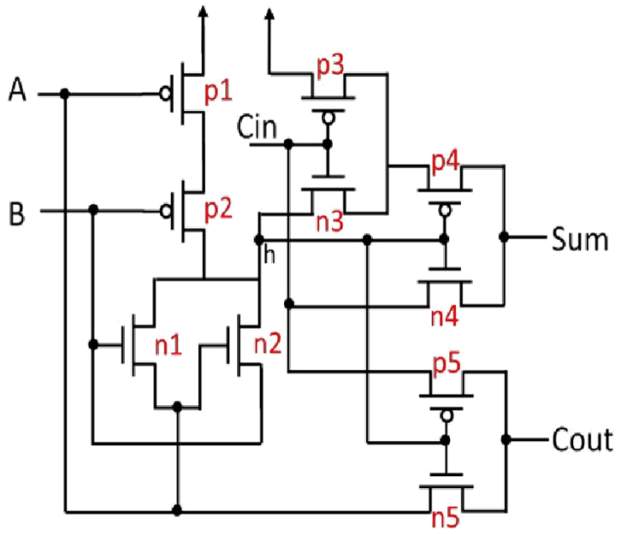


Figure 1: The variation of supply and threshold voltages with different technology nodes

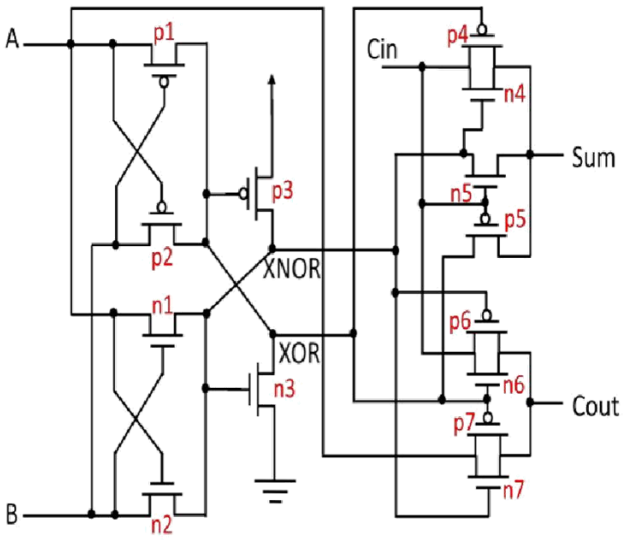
DESIGN OF ADDERS

The CMOS technology allows us to implement the same logic in different styles. The most regularly used logic is the Static CMOS logic which is mainly compromised of a circuitry to pull the voltage to VDD with pMOS transistors and circuitry to pull the voltage to ground with nMOS transistors. Another method known as "Domino logic" is also frequently used method for increased-speed and minimal area circuit designs which uses either one of the nMOS or pMOS devices. As a substitute for the conventional CMOS Pass, a new logic family was

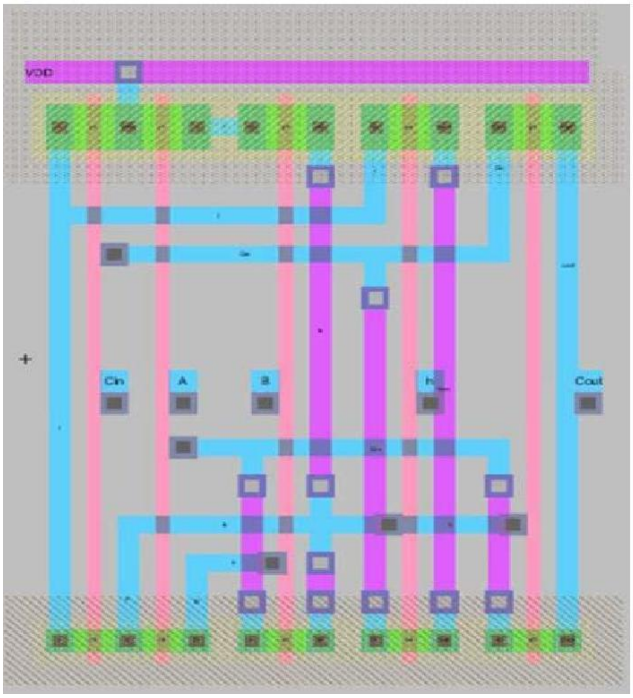
introduced for the transmission of data known as "Pass Transistor Logic". Although the Static CMOS is mostly known for its robustness, it uses both pMOS and nMOS in its design which in-turn increases the number of transistors. To overcome this we propose two adders with smaller transistor counts, known as 10T and 14T [3]. In this paper we mainly focus on the performance of the proposed adders and compare it with the Static CMOS logic. To simulate the proposed circuits in deep sub-micron process various interconnect parameters like the parallel plate capacitance, fringing capacitance the width and length of the wires are required. The work done in reference [3] was helpful in implementation of the proposed logic. The LVS (Layout vs. Schematic) tool in electric vlsi cad software was used to generate the layout and circuit diagram as shown in the figure 2.



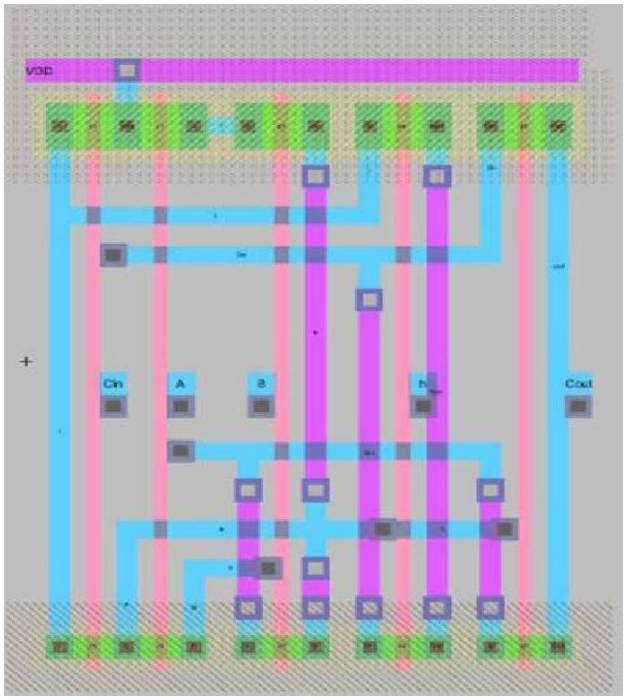
(a) 10T Adder Circuit



(b) 14T Adder Circuit



(c) 10T Adder Layout



(d) 14T Adder Layout

Figure 2: Circuit and Layout Design of Adders

RESEARCH METHODOLOGY

This Paper was implemented using the "Electric VLSI CAD" software. For obtaining the accurate results, various parasitics are to be incorporated in the research. Reference [8] provides a deep and valuable insight for the calculations of these parasitics in different technology nodes. The obtained parasitic values are inserted into the layout design which enables us to obtain the SPICE models including the capacitance values.

After designing the layout, the calculated values of metal and interconnect parasistics are entered in the software. The whole idea of assigning the values of capacitances to the proposed research is to obtain the accurate results without which there will be no point of doing this research. The values of capacitances that are used in this paper are summarized in the table 1.

Table 1: Parasitic Capacitance Values used in Technology Node.

	Technology Node (nm)	90	65	45	32	22	16
Metal_1	Plate Capacitance ($aF/\mu m^2$)	82.639	97.396	221.35	251.54	357.27	470.73
	Total Fringe Capacitance ($aF/\mu m$)	209.534	164.631	187.085	185.325	208.085	227.912
Metal_2	Plate Capacitance ($aF/\mu m^2$)	55.093	64.931	147.57	167.69	238.18	313.82
	Total Fringe Capacitance ($aF/\mu m$)	16.1246	12.6694	14.397	15.2798	18.6462	21.164
Polysilicon	Plate Capacitance ($aF/\mu m^2$)	165.28	194.79	442.71	503.08	714.55	941.46
	Total Fringe Capacitance ($aF/\mu m$)	148.776	117.998	139.633	133.932	146.916	155.776

The obtained SPICE code from the design forms the base for the entire simulation. The code is obtained from the layout which contains the information about the connections between devices and various parasitics for the proposed technology node. In order to match the analysis the code is changed updated. This comprises of the increment/decrement of voltages and loads to perform the simulations. The inputs are specified as A, B, Cin. This is done to check whether our extracted net list fulfils the functionality of adder and also to measure the time delay from the input to the output.

RESULTS

This section describes the simulations done in this research. This includes the scaling of the supply voltages, calculating the delay and the power dissipation.

LOAD vs. DELAY:

An external capacitive load is attached to the adder in order to determine its driving capability. The capacitive load C load value is added manually to the generated SPICE code that comprises of the delay calculations for the worst case. By maintaining constant supply voltage the load capacitance is varied from no load to maximum load in steps. The results that are obtained for 10T and 14T adders are summarized in the tables 2 and 3

A graph is plotted for load vs. delay for different adders as shown in the figure below. The performance of the 14 transistor adder is superior to static CMOS, the reason being that there is only one pass transistor that acts as a bridge between I/O. The MOSFET's that are connected to V ground rail (p3, n3) acts as DD and feedback in 14 transistor circuit to make sure the voltage makes peak to peak transition on the inner nodes of the transistors. The 10 transistor circuit on the other hand has its output connected to the input By a single pMOS or nMOS path. However, due to this reason the10 transistor adder has reduced voltage swings (VDD-V) in its T nodes. Hence for larger loads the 10 transistor adder has the bad delay-load proportionality when compared with other adders.

Table 2: Load vs. Delay for 10T Adder

Technology node (nm)	(fF)	Rise time (ns)	Fall time (ns)
90	0	0.11753	0.10665
	5	0.14054	0.13325
	10	0.15563	0.14678
	20	0.185	0.17297
	50	0.26929	0.24782
	100	0.41219	0.37189

Table 3: Load vs. Delay for 14T Adder

Technology node (nm)	(fF)	Rise time (ns)	Fall time (ns)
90	0	0.11753	0.10665
	5	0.14054	0.13325
	10	0.15563	0.14678
	20	0.185	0.17297
	50	0.26929	0.24782
	100	0.41219	0.37189

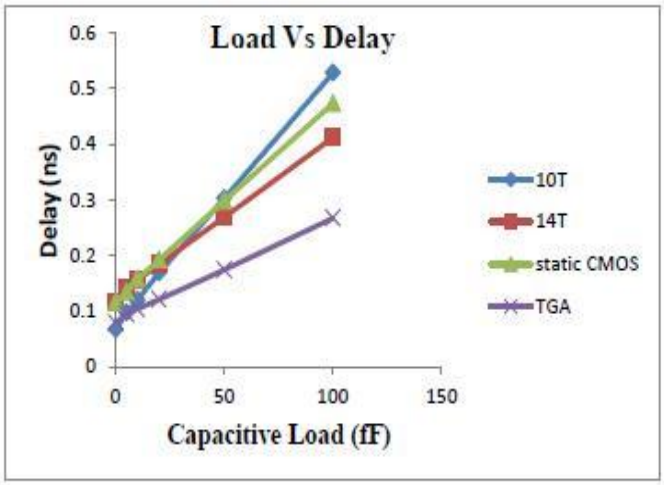


Figure 3: Load vs. Delay for Various Adders

VOLTAGE SCALING vs. DELAY:

A "Fan out of Four" inverter is connected to the proposed circuit in order to compute the delay vs. voltage scaling. We again extract the SPICE model to calculate the delay. The 10 Transistor adder is based on the pass transistor logic style involving both PMOS and NMOS.

The performance of this adder is worst due to the reason that the voltage levels degrades so much, that it makes difficult for the system to set noise margin levels. In other words, due to poor noise margin the output gets corrupted due to which we are not able to differentiate between 1's and 0's. So it makes no sense to compare the 10 transistor adder with any other adders. However, this parameter is calculated with 14 transistor adder as shown in the table 4.

Table 4: Voltage vs. Delay values for 14T Adder

Technology node (nm)	Voltage (V)	Rise time (ns)	Fall time (ns)
90	1.0	0.17097	0.19563
	1.1	0.1561	0.18204
	1.2	0.14862	0.14272
	1.3	0.1403	0.13121
	1.4	0.1343	0.11567
	1.5	0.12777	0.10502

The graph for various adders is plotted by taking the voltage on horizontal axis and delay on vertical axis as shown in the figure 4 . Deterioration of the voltage swing can be seen in the nodes of MOSFET's in 14 transistor adder due to scaling down of the supply voltage leads to increased delay of the 14T adder. Despite the fact that the feedback because of MOSFET between supply rails VDD and gnd(p3, n3) can rebuild the voltage swing, but are no longer efficient when the power supply value equals twice the value of threshold voltage of NMOS (VTn). The TGA provides the best performance in this case with reduced supply voltage as the transistors does not get affected by a declined voltage swing (VDD- VT).

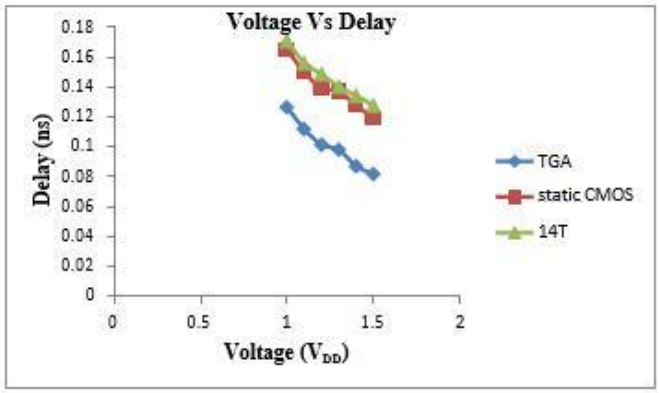


Figure 4: Voltage vs. Delay for various adders

POWER DISSIPATION

The FO4 load that has been used in the calculation of voltage scaling is also used in the calculation of power. The circuit shown in the figure 5 is used connected at the output of the full adder and is used to calculate the total power dissipated by the adder. The circuit comprises of a parallel combination of resistor Ry and a capacitor Cy. A power supply (VDD) is connected to one end of the circuit and another dc power supply (VCC) having an initial voltage of zero volts is connected on the other end. The updated SPICE code is again obtained and the values of Cy, Ry are entered manually.

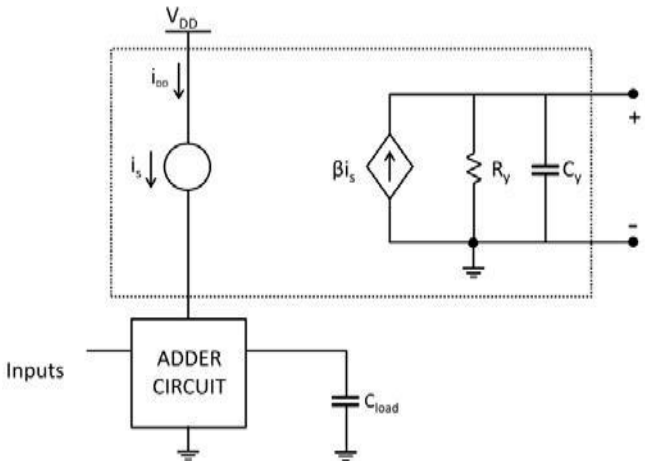


Figure 5: Circuit for Calculation of Power Dissipation.

The power dissipation for the 10 transistor adder is not calculated for the same problem that has been discussed in the voltage scaling section above. The resultant values for the 14 transistor adder are given in the table 5.

Table 5: Power Dissipation of 14T Adder

Voltage (V)	Initial step size V_1 (µV)	Final step size V_2 (µV)	Power (µW)
1.0	0.78369	15.156	0.3593
1.1	0.87799	17.531	0.4163
1.2	0.92324	19.981	0.4764
1.3	1.047	22.768	0.5430
1.4	1.0987	25.714	0.6153
1.5	1.1788	29.116	0.6984

A graph is drawn between the power dissipation and the supply voltage for different adders as shown in the figure 6.

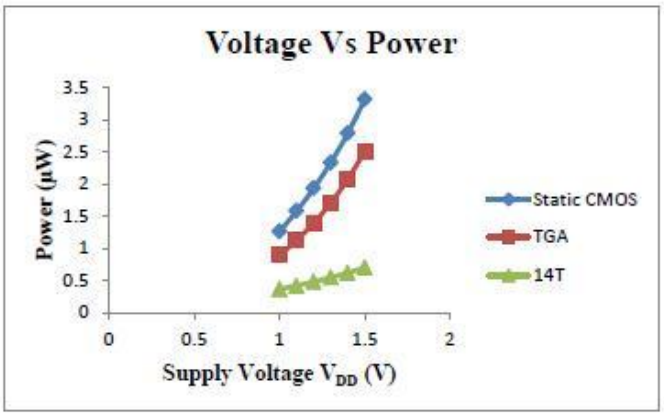


Figure 6: Voltage vs. Power results for different Adders

CONCLUSION

The main idea behind this paper was to compare the designed adders with the most conventionally used adders like static CMOS, Transmission Gate Adder (TGA), Pass Transistor Logic (PTL) etc., However we find from this study that low transistor count adders (10T and 14T) do not perform up to the mark in terms of delay when implemented in nano scale CMOS technologies.

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