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Synthesis of Blind Adaptive Beamformer using NCMA for Smart Antenna

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Abstract

For the ever growing demands and challenges of wireless communication applications, usage of smart antenna is very much beneficial. Beamformer is an important module of smart antenna whose design and development is a great challenge. It demands performance enhancement, at reduced cost and size, with minimized system development times. Beamformers' performance depends on the choice of the algorithm. Advancements in the integrated circuits technology have paved a way for the fabrication of modules on a single chip. Traditional approaches of hardware design for any algorithm based system are time consuming and elaborative, due to separate hardware and software design paradigm. In this paper an approach that would speed up the beamforming algorithm development process and synthesis of beamformer using simulation tools is presented. In this work a simplified approach that would aid for the design of single chip solution for blind adaptive beamformer is presented. Normalized Constant Modulus Algorithm (NCMA) blind adaptive beamforming algorithm is considered for simulation using Matlab HDL coder ®tool and synthesis is performed using Mentor Graphics' precision synthesis RTL plus ® tool. Synthesis results in terms of resource utilization and its functional verification using mentor graphics modelsim are presented.

Keywords: smart antenna, beamformer, blind adaptive beamforming, cma, fpga, quadrature amplitude modulation (qam), synthesis.

INTRODUCTION

Smart Antenna Systems are one of the solutions to meet the demanding challenges of efficient and powerful wireless communication systems [1]. Typical representation of smart antenna is shown in Fig. 1. An antenna array which has the ability to radiate maximum in desired direction and at the same time minimise its radiation in other direction is called as "smart antenna". This ability of smart antenna is known as "Beamforming" and the module that implements beamforming is known as "Beamformer".

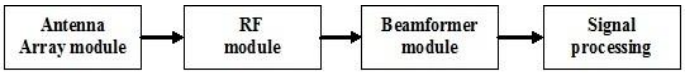

Figure 1: Representation of typical smart antenna system

Beamformer receives the processed signals from antenna array and radio frequency (RF) module, as the signals received by the antenna array are of high frequency continuous signals in nature. Beamformer's output which is the required signal will be used further processing to collect the required information. Smart antenna can be at both transmitter and receiver side.

Beamformers' performance can be assessed by the choice of the algorithm. Beamforming algorithms can be broadly categorized as blind adaptive algorithms and non-blind adaptive algorithms. The techniques in which it is required to know the direction of arrival of the required incoming signal or which require techniques to estimates the direction of the required signal are termed as "non-blind adaptive beamforming algorithms". Both temporal and spatial reference beamforming algorithms are of non-blind type. Blind adaptive beamforming algorithms are those which do not depend on the information of direction of the required incoming signal, instead rely on the properties of the desired signal. Constant modulus algorithm (CMA) was first blind adaptive beamforming algorithm developed utilizing the constant modulus property of digital modulated signals. Blind adaptive beamforming algorithms involve reduced computational complexity and well suited for digital data communication involving frequency modulation techniques such as quadrature amplitude modulation (QAM). In time based or location based wireless applications involving digital transmission usage of blind adaptive beamforming algorithms would be very much efficient. Blind adaptive beamformer is a one which uses blind adaptive beamforming algorithm to

achieve beamforming [4].

For the beamformer design the chosen beamforming algorithm needs hardware implementation. Typical hardware implementation platforms are digital signal processors (DSPs), field programmed gate arrays (FPGAs) and application specific integrated circuits (ASICs). Among the three platforms FPGAs will offer greater advantages and benefits in terms of design, cost and performance [3] [7]. With the existing advanced semiconductor integration technologies and tools, it is possible to develop single chip solution for beamformer for smart antenna system. The design objective would be to minimize the design cost by effectively utilizing resources in order to meet the design specifications. Typical processing steps to develop single chip solution for any algorithm based processing system using FPGA are shown in Fig. 2.

Specification or requirements of the algorithm or system (beamformer in this case) are captured and behavioral description in the form of hardware description language (HDL) is developed. HDL description is synthesized to get register transfer level (RTL) description, followed by gate level synthesis. Optimization for the performance in terms of timing and area is performed at gate level. Physical description involves mapping, place and route on FPGA to develop single chip solution and other FPGA board based applications. During this design cycle of the system, developed RTL code may be needed to be modified or altered in case of any changes in the functionality of the system. Traditional design flow with separate hardware- software paradigm does not provide any means for the testing and verification of the system. Also, appropriate hardware model required for the final implementation cannot be obtained from the traditional design process. For the design and development of a cost effective and powerful system and to address the issues hindering the design process, a suitable methodology and adequate tools is the pre requisite [5].

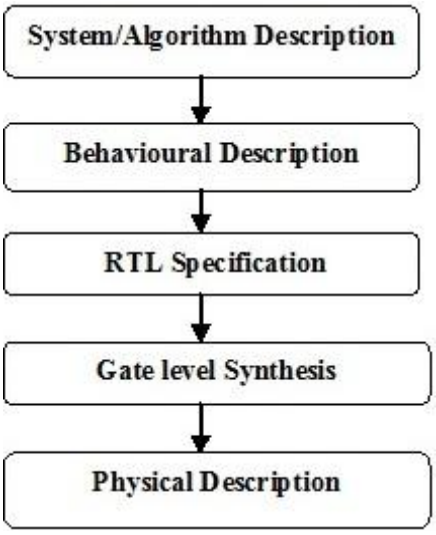

Figure 1: Design flow for FPGA based single chip solution

Most of the research in terms of beamforming algorithms is restricted only to simulation and not have proposed towards synthesis of them. Research related to synthesis of algorithms is mostly C-language based and in literature synthesis of beamformers has not been carried out. In this work synthesis of blind adaptive beamformer using NCMA algorithm for development of single chip solution is presented. For implementation of this work HDL coder ® tool of Matlab and Precision Synthesis Plus tool ® of Mentor Graphics are utilized.

The organization of rest of the paper is as follows; objective and scope are discussed in section 2, along with beamformer design and development process, section 3 addresses the implementation and the obtained results discussion, followed by the conclusion in section 4.

BACKGROUND

Motivation for this research work is the demand for the powerful and cost effective wireless communication systems. Growth in the users of wireless communication and its applications in recent past have been very active. Advancements in FPGA technology in terms of their capabilities have enabled their extensive use in design of complex systems such as wireless communication. There has been a great challenge for the research in the design of wireless communication and its modules to meet their demands and requirements in terms of performance, speed and cost. In the view of these aspects, beamformer, which can be regarded as core of smart antenna, its simulation and synthesis is the primary objective in this work. In this work synthesis of blind adaptive beamformer using Mentor Graphics' precision synthesis RTL plus ® tool for NCMA beamforming algorithm is performed.

A. Relevant Works

An approach for hardware implementation DSP algorithms for wireless applications using QAM decoder is presented is in [6]. Here, synthesis and verification of QAM decoder using C-language approach is performed. Significance of adaptive beamforming and functioning of Least Mean Square (LMS) beamforming algorithm is presented in [7] and Verilog code simulation for FPGA implementation is also carried out. Utilization of HDL coder in automatic generation of synthesizable Verilog code for image processing application is discussed in [8]. It also presents the synthesis results using Xilinx ISE in terms of it resource utilization of the selected FPGA device. A method to speed up the design process using simulation and synthesis tools such as Mentor Graphics, in particular precision synthesis RTL plus tool for FPGA synthesis can be found in [9] [10].

B. Beamformer design and development process

The development process of FPGA based algorithm system involves the steps of requirement specifications, testing and verification followed by the implementation. An important aspect of the system design is reusability, which has to be considered in prior so that the developed system can be modified in future. A good design methodology with appropriate tools will provide excellent environment for the design and development of a cost effective, powerful and compact system [5].

A single chip solution for beamformer independently as DSP system designer would be of simulation of developed algorithm and verification of the obtained results using different tools. FPGA design starts from the RTL level, which involves validation of the design against hardware specifications and developing test benches. This also includes synthesizing, mapping followed by place and route (PAR) cycles which will represent the physical or transistor description. Such design cycle approach will increase the development time significantly and hence the time to proto-type and time to market will be increased.

One of the steps to reduce the development time will be adopting simplified design methodology, reduced iterations at RTL level and integration of software-hardware work flows. Model based approach would be beneficial that would ease up the integration and hence reduces the system development time. The availability of advanced tools for the systems design and development has contributed greatly to speed up the system design process.

The representation of model based unified DSP and FPGA design flow which is performed in this work is shown in Fig. 3. As depicted in the flow chart, design flow starts with specifications of the beamformer in terms of number of array elements, spacing between them, required array gain are to be captured. An algorithm is to be developed as per the specifications in Matlab environment. Developed algorithm must be compatible with HDL coder, which has to be of the form of function and a test bench. As Verilog supports integer or real number arithmetic operations only, any complex number mathematical processing has to be implemented using these arithmetic operations. Developed algorithm would be simulated for functional verification and modified if required and simulated again. Verilog code and test bench of the algorithm was generated using HDL coder, which will be simulated using any modelsim tool. Verification of HDL code will also be performed along with test bench, which is termed as co-simulation. HDL coder will also generate a tool command language (TCL) script that is to be used with synthesis tools. Generated tcl file will be imported for synthesizing of generated Verilog code. Synthesis would be performed under design constraints and performance is verified using selected target device. Developed algorithm can be deployed on FPGA board for development of single chip solution. This approach can also be used in development of FPGA-SoC based wireless applications.

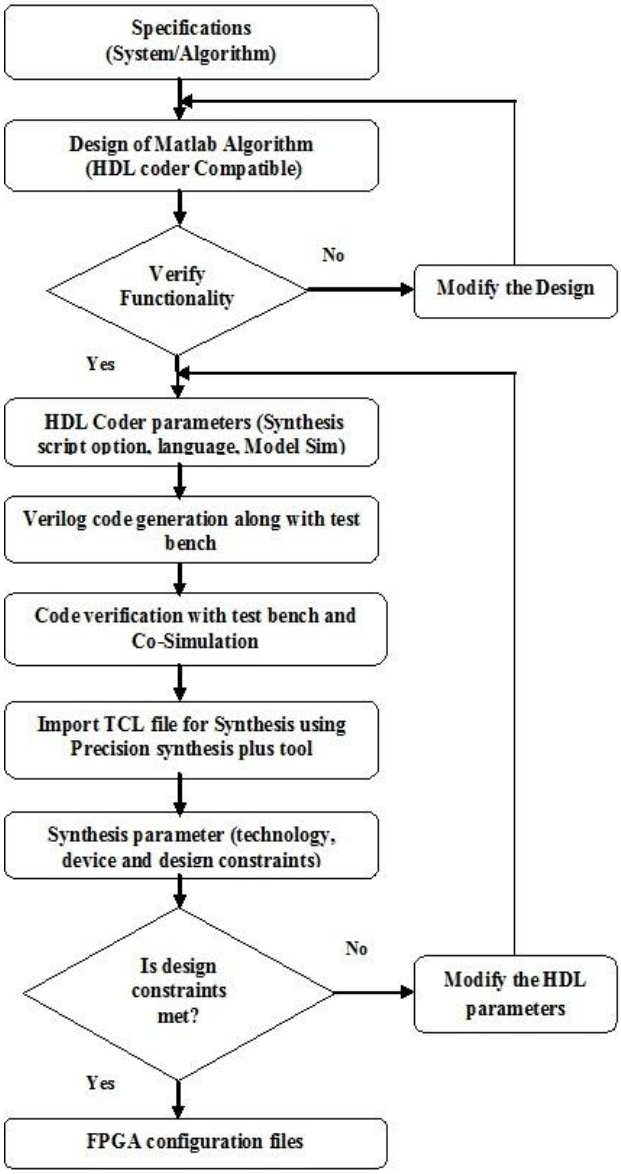

Figure 3: Flow chart depicting the design flow performed

Implementation Results and Discussion

Implemented work is extended version of our previous work [4] in which NCMA's performance was verified, which was better than Hamming constant modulus algorithm (HCMA) [11]. Obtained results of [4] are represented here again for reference in Fig. 4 and 5. As it can be observe from the figures, antenna array response without beamforming will be uniform in all the directions, because of the fact that the array elements are of Isotropic in nature. After beamforming the array gain is concentrated in desired direction, which is 25^{o} degree in this case. Generated Verilog code was simulated using mentor graphics modelsim tool and simulation result is shown in Fig. 6. It was observed that the array gain obtained

is exactly same as with the Matlab version of the order of 13 db. Figure 7 shows the snapshot of successful completion of HDL code generation and its verification.

Here, synthesis of NCMA to aid towards the development of single chip solution of blind adaptive beamformer is performed. HDL coder requires the algorithm to be in the form a function and test bench. Therefore, NCMA algorithm was modified in the form of a function and test bench and division of complex numbers was performed by rationalizing with complex conjugate because Verilog does not supports complex number arithmetic. Beamformer specifications considered are as follows: number of array elements is 4 with spacing of ʎ/2 between them. Numbers of samples considered are 100 with 16-point QAM format and with a step size of 0.05 with desired direction of 25°. Beamformer parameters and their values are summarized in table 1.

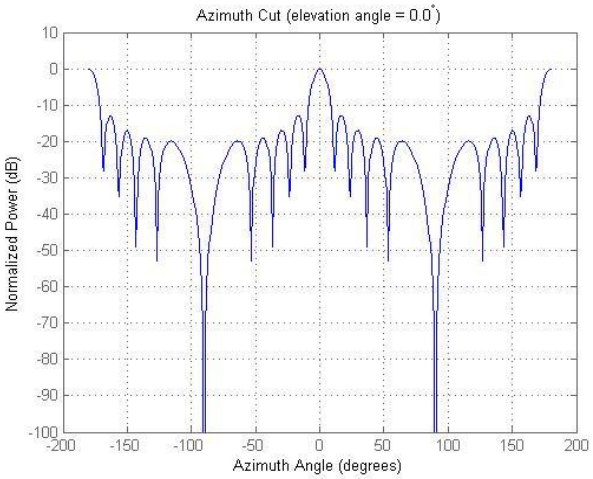

Figure 4: Array response before beamforming

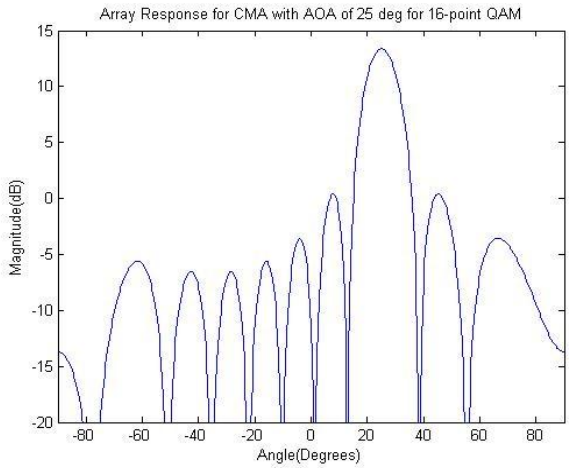

Figure 5: Array response gain using NCMA

Table 1: Beamformer design parameters considered

Parameters	Array elements	Spacing	Samples	Desired direction	Step size
Values	4	ʎ/2	100	25°	.05

Generated verilog code using HDL coder was simulated using mentor graphics modelsim and simulated result is shown in Fig. 6. It was observed that the array gain obtained is exactly same as with the Matlab version of the order of 13 db as shown in Fig. 5. Figure 6 shows the snapshot of successful completion of HDL code generation and its verification.

For the synthesis of blind adaptive beamformer with NCMA using precision synthesis RTL plus tool, TCL file was imported from the HDL coder tool. Target device chosen was Altera's cyclone V family of device (5CGXFC7D7F31C), which is one of low cost and low power family industry standard device. It was observed that there is a slight reduction in array response gain because of the floating to fixed point conversion to 14-bits resolution during HDL code generation. NCMA co-simulation result is shown in Fig. 8.

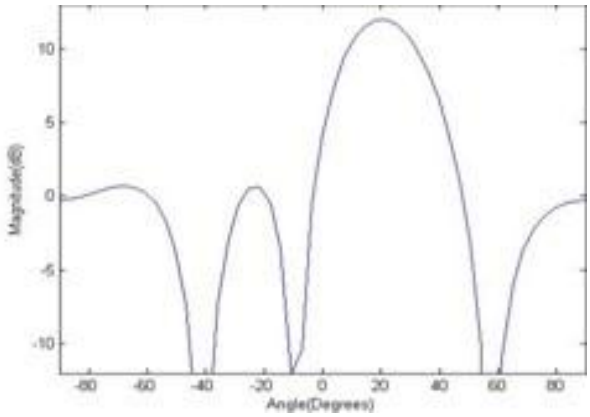

Figure 6: NCMA simulation result using Verilog code

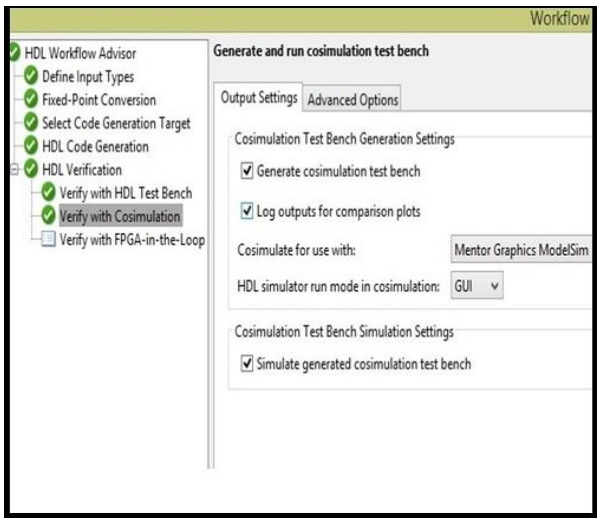

Figure 7: Snapshot of successful HDL code generation

Verilog code generated by the HDL coder was optimized by loop rolling and registers pipeline techniques. Generated Verilog code was verified Mentor Graphics ModelSim SE10.3f and the result is shown in Fig. 9. Synthesis results of NCMA using precision is shown in Fig. 10 along with the resource utilization information in Fig. 11. Table 2 shows the resource utilization for RTL synthesis for the Altera cyclone V device used for synthesis.

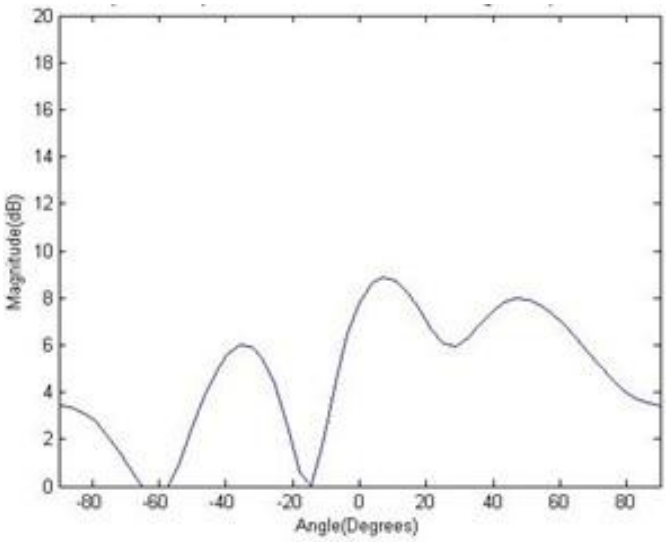

Figure 8: NCMA co-simulation result

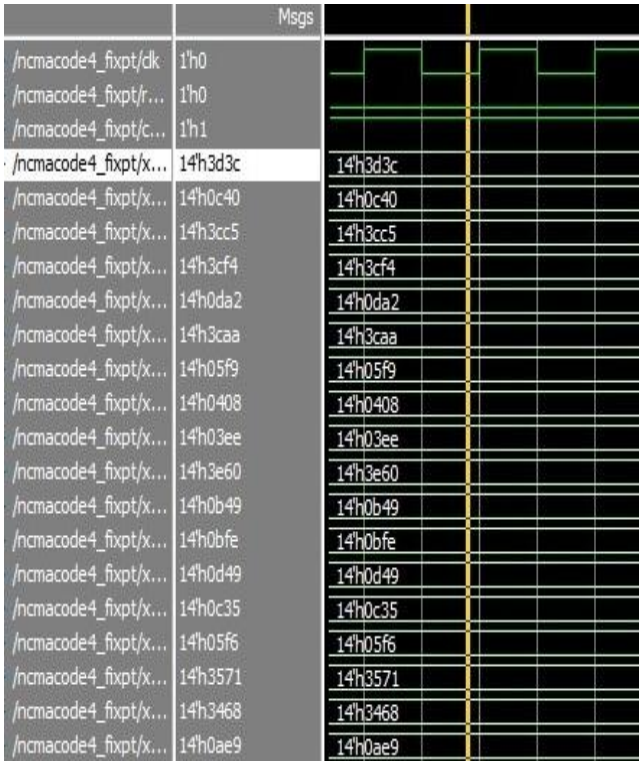

Figure 9: Modelsim waveforms of co-Simulation result

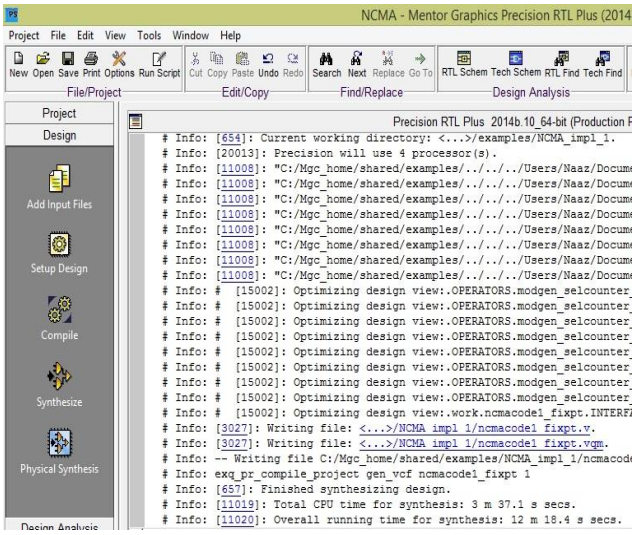

Figure 10: Synthesis report of NCMA

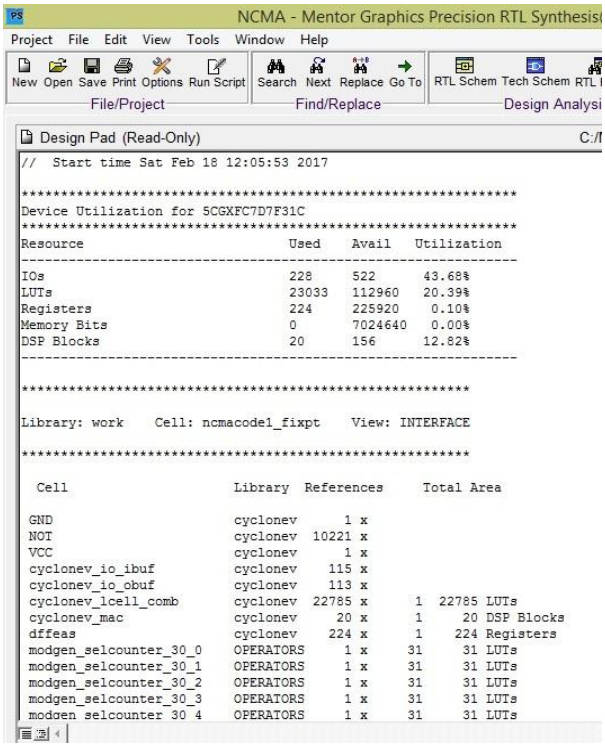

Figure 11: Resource utilization report generated result

Table 2: Resource utilization of the device 5CGXFC7D7F31C

Resources	Used	Available	Utilization (%)
IOs	228	522	43.68
LUTs	23033	112960	20.39
Registers	224	225920	0.10
DSP blocks	20	156	12.82

CONCLUSION

Smart antenna system will be significant in meeting the demands and challenges of current and future wireless communication applications. Design and performance of the beamformer module will be significant in implementation of smart antenna functionality. The utilization of simulation and synthesis tools will speed up the beamformer module for the smart antenna system design.

In this work, NCMA which is modified form of basic CMA algorithm was considered for the synthesis of blind adaptive beamformer. HDL coder of will generates optimised and synthesisable HDL code which would simplify and speed up the design process compare manual HDL coding. From the results it was evident that the performance of Verilog form of NCMA was almost same as its Matlab form of the order of 13db. HDL coder will also generate TCL script for the generated Verilog code, which would be used with synthesis tools, in this work Mentor Graphics' precision synthesis RTL plus tool. Mentor graphics tools are significant in design and development of industry standard solutions. Physical aware synthesis of NCMA beamformer using Altera cyclone V device was performed and the resource utilization is presented. It was observed that for such complex signal processing NCMA algorithm resource utilization was very much less, which means that the beamformer module can be easily designed with the FPGA device.

Even though comparative performance was obtained from Verilog simulation NCMA, but over all response in terms of array gain and beamforming has been degraded slightly. One of the reasons for this degradation would be the conversion of floating point numbers to fixed point numbers with fixed resolution. NCMA implementation with Matlab was with 1000 samples and array elements were 10, in this study number of samples and array elements were reduced to 100 and 4 respectively. This is due to the fact that, computer simulation time will increase with larger input data and also the FPGA device density is also limited. For the design of simple and low cost FPGA based wireless communication system, proposed approach would prove to be effective.

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