Performance Analysis of Cascaded Multilevel Inverter Based DSTATCOM

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Abstract

In this paper, a single-phase Seven-Level and Five-Level cascaded H-Bridge Inverter (CHB) based Distribution Static Compensator (DSTATCOM) is presented. A simple control algorithm based on inverse park PLL was proposed for both five-level and seven-level inverters. Synchronous Reference Frame theory (SRF) as control algorithm is used for reference source current extraction and to generate gating pulses for the DSTATCOM. The main aim of the CHB is to eliminate source current harmonics and improve input power factor in the single-phase distribution system. The multilevel inverter has some limitations in its applications due to high complexity and size. The proposed control algorithm has two components, converting the load current into stationary reference frame coordinates and estimation of peak amplitude of load currents. Hence, a simple and reliable controller with ease of implementation was developed. The algorithm for single-phase DSTATCOM is aiming to perform with accurate tracking performance under step changes in load currents and to provide good dynamic compensation. In this paper, Inverse-Park transformation is adopted for generating quadrature component of current because of its dynamic performance under all varying conditions. The performance of the control algorithm is tested and evaluated using MATLAB/Simulink.

Keywords: Distribution Synchronous Compensator (DSTATCOM), Cascaded H-Bridge Inverter (CHB), Power Quality (PQ), Phase-Locked Loop (PLL).

INTRODUCTION

In recent years, harmonics is the most important issue in terms of power quality. Due to wide-spread of power electronic devices in commercial, industrial and domestic loads. In distribution systems, the usage of non-linear loads such as computers, variable/adjustable speed drives, LED lighting systems and compact fluorescent lamps etc are using widely and prone to harmonics. These harmonics are causing severe problems such as power losses in equipments, malfunctioning of devices, damaging of sensitive loads and motor failures. Therefore, it is a serious concern in distribution systems for both consumers and suppliers to eliminate harmonics and meet the requirements of IEEE 519-1992 or IEC 61000-3-2 [1]-[2].

The harmonics produced by the loads are causing grid voltages to be distorted. Conventionally, passive filters are employed for harmonic mitigation and reactive power compensation. But, these suffer from disadvantages like, cost, bulkiness, resonance and fixed compensation [3]. Therefore, a dynamic solution is preferred that fits the compensation is a DSTATCOM. The role of DSTATCOM is to compensate harmonic currents and reactive power with improved power factor produced by the load. The controller has to track the step changes in the load accurately and to choose reference current properly for better compensation.

Keeping accuracy and reliability in view, many techniques are proposed in literature for quadrature signal generation. Zero Crossing Detector (ZCD) [4] method is simple but, sensitive to grid variations. The most widely used method is synchronous reference frame theory and SOGI based theory [4]-[5]. It is less accurate to unbalanced and lower harmonic components. But, SRF theory with inverse park transformation based algorithm is found satisfactory under distorted conditions with low computational burden. However, application and implementation of this control strategy for a five level cascaded H-bridge active power filters has not gained much attention in the literature.

Multilevel inverters have gained much attention due to its enormous advantages over conventional voltage source inverters. The conventional two-level inverter is also capable of handling reactive power, harmonic reduction and power factor improvement under various load changes. But, due to advancement of power electronic devices and controllers, multilevel inverters have shown their ability to compensate power quality problems with simplicity, low cost, reliability and high-quality output. There are many topologies proposed in the literature [7]-[9]. Flying capacitor based inverter, neutral point clamped inverter and cascaded H-bridge type multilevel inverter is found suitable for DSTATCOM application with ease of control.

In this paper, CHB type of multilevel inverter is used to reduce the rating of the devices used and elimination of harmonics with an increase in levels of the converter. This method also reduces the switching losses and decreases the ratings of the DC link capacitors used. The control algorithm is found effective in linear/ non-linear and increase in load conditions. In order to all these topologies, various PWM techniques were also proposed in the literature which includes selective harmonic elimination based PWM, Multilevel space vector based PWM and Carrier based PWM etc [10]-[24]. The main advantage of this CHB inverter is increasing of switching
levels by increasing the number of H-bridges in the circuit. This paper uses a simple SRF based control in addition with inverse park transformation based PLL to generate quadrature signal for harmonic elimination and reactive power compensation.

A CHB based DSTATCOM is proposed in this paper, Non-linear load conditions under steady state and dynamic conditions are carried out using Simulink, simpower systems block set and its performance found satisfactory.

**PROPOSED CONFIGURATION AND CONTROL ALGORITHM**

The CHB based DSTATCOM shown in Fig. 1. Each H-bridge consists of a two-leg Voltage Source Converter (VSC) consisting of 8 IGBT switches for five-level and Three VSC’s with 12 IGBT switches with separate DC sources for each VSC as shown in Fig. 2. DSTATCOM is connected in between source and load in parallel through an interfacing inductor L at the point of common coupling (PCC). The proposed controller for DSTATCOM is capable of maintaining the total harmonic distortion (THD %) within the limits by eliminating the harmonics in the source current. Power factor correction, reactive power and harmonic compensation is also done even under varying linear and nonlinear load conditions to test the performance of the controller. The DSTATCOM can be operated with required active and reactive power injection by adjusting the magnitude and phase of the system. The ratings of the proposed system are listed in appendix. The rating of the DSTATCOM should be 15% more than the Load rating for safer and economic operation.

**Inverse Park Transform**

Fig.3 shows the structure of inverse park transformation. In this method, two loops are formed that are nonlinear and interdependent. In order to eliminate algebraic loops, First-order low pass filters are employed for each d and q signal. Park transformation is done (i.e, dq0/dq0s) and these outputs are used for inverse park transformation as shown in fig.3.

**Figure 1:** Line Diagram of the Proposed System.

**Figure 2:** Cascaded H-Bridge Multilevel Inverter

**Figure 3:** Inverse Park Transformation based Quadrature Signal Generation

**Figure 4:** Block Diagram of Reference Source Current Generation
\[
\begin{bmatrix}
V_a \\
V_p
\end{bmatrix} = \begin{bmatrix}
\cos \theta & \sin \theta \\
-\sin \theta & \cos \theta
\end{bmatrix} \begin{bmatrix}
V_a \\
V_p
\end{bmatrix}
\]

(1)

The dynamics of the phase detector mainly depends on the low pass filter that is used after the transformation to filter out any noises or harmonics that are present in \( V_a \) and \( V_p \).

\[ LPF(s) = \frac{w_c}{s + w_c} \quad \text{where, } w_c \text{ is the cut-off frequency} \]

(2)

The difference from other PLL’s is generating a dummy voltage signal from the feedback loops.

**B. Reference Current Generation**

The peak amplitude of active component of current is calculated as shown in Fig. 4. The Load current is sensed and supplied to inverse park transformation to generate quadrature signals (I_{aα} and I_{aβ}) and then transformed back to I_d and supplied to a low-pass filter. The output is then added with the output generated by the DC voltage control loop to produce reference active component of current (I_{dP} + I_{dC}). The measured voltage (V_{dc}) across the two DC capacitors for five-level (V_{dc1}+V_{dc2}) and three capacitors for seven level (V_{dc1}+V_{dc2}+V_{dc5}) are summed and compared with the DC bus reference voltage \( V_{dc^*} \). The error of the signal at \( n \)th sampling instant is given by:

\[ V_d(n) = V_{dc^*}(n) - V_{dc}(n) \]

(3)

The voltage error \( V_d(n) \) is then supplied to Proportional-Integral controller to regulate the DC bus voltage of DSTATCOM. At \( n \)th sampling instant, the output of the PI controller is as:

\[ I_{dP}(n)=I_{dP}(n-1)+K_p(V_{dc^*}(n)-V_{dc^*}(n-1))+K_iV_{dc}(n) \]

(4)

Where, \( K_p \) and \( K_i \) are proportional gain and integral gains of the PI controller. \( V_{dc^*}(n) \) and \( V_{dc}(n) \) are the DC bus voltage errors in \( n \)th and \( (n-1) \)th instant and \( I_{dP}(n) \) and \( I_{dP}(n-1) \) are the amplitudes of active component of currents at the fundamental reference current in \( n \)th and \( (n-1) \)th instant.

The average magnitude of current (I_{dP}) and the output of the PI controller (I_d) are summed up and transformed to I_α (reference source current) from \( d\theta \) component and then compared with the actual source current to produce error magnitude of current and then supplied to a PWM controller to generate gating pulses to the multilevel inverter.

**SIMULATION RESULTS AND DISCUSSION**

In this section, the proposed control algorithm is evaluated and tested using MATLAB / Simulink on a single-phase distribution system loaded with linear and non-linear loads. Fixed time step of 20µs with ode3 (Bogacki - Shampine) solver is chosen for simulation.

Few test cases are performed for evaluation of DSTATCOM are:

- The performance of the controller when a linear load is applied is shown in Fig.5 when time t=0.4s to 0.5s. In Fig.6, Non - linear load is applied from time t=1s to 2s and increase in load from time t=2s to 3s is shown in Fig.7. A mixed load (Linear and Non-linear load) is applied from time t=3s to 4s as shown in Fig.8. All these test cases are performed under sinusoidal grid conditions. The five-level and seven-level results are shown and prove that the seven-level inverter is found more effective with low total harmonic distortion. The five-level inverter shows a staircase output across the inverter whereas the seven-level inverter output is near sinusoidal. This indicates that the filter capacity that is required is more for five-level inverter compared to seven-level inverter. The performance under dynamic conditions is found satisfactory. The DC bus voltage regulation, reactive power and harmonic compensation with power factor improvement shows the effectiveness of the controller. A sinusoidal PWM strategy was employed for gating the inverters. THD (%) of all the four cases mentioned above are presented in table-I prove the effectiveness of the controller.

**CONCLUSION**

In this paper, a simple and effective control algorithm based on SRF theory and Inverse-Park based transformation based PLL for single-phase five-level and seven-level cascaded H-bridge inverters has been analyzed, compared and validated using MATLAB / Simulink. This theory is adopted to work in sinusoidal grid voltage conditions and Non-Linear load conditions. The source current THD (%) is maintained within IEEE 519-1992 limits in both the inverter configurations. Seven-level inverter has proven more promising and reliable compared to five-level inverter. Seven-level also reduces the cost of additional filtering component that is required and low rating DC bus capacitors can be used which makes the overall cost low. The control algorithm is very promising and easy to implement because of its simple structure and accuracy. The harmonic compensation and power factor is effectively done under all steady-state and dynamic conditions. The injected current of the DSTATCOM was also very close to the reference values and proved a smooth and reliable profile. The DC link voltage is well balanced in seven-level converter compared to five-level cascaded H-bridge Inverter. Therefore, a Seven-level CHB is preferred for low to medium power ratings at the distribution level.

<table>
<thead>
<tr>
<th>Table-I</th>
<th>THD (%) of Test Cases (Table-I)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Five-level</td>
</tr>
<tr>
<td>Fig No.</td>
<td>I_s</td>
</tr>
<tr>
<td>5</td>
<td>2.47</td>
</tr>
<tr>
<td>6</td>
<td>3.15</td>
</tr>
<tr>
<td>7</td>
<td>2.76</td>
</tr>
<tr>
<td>8</td>
<td>2.40</td>
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</tbody>
</table>

**APPENDIX (Table-II)**

- **Grid Voltage & Frequency**
  - Single-Phase, 230V, 50Hz
- **Source-side Impedance**
  - Rs=0.1 Ω, Ls =2.5mH
- **Non-linear: Single-phase diode bridge rectifier**
  - R=40Ω, L= 250mH
- **Linear Load**
  - R=40 Ω, L=250mH
- **PWM Switching frequency**
  - 2kHz
- **Reference voltage of DC bus**
  - 400V
- **Interfacing inductor**
  - L=1.5mH
- **Gains of PI controller for DC bus**
  - \( K_p=0.32 \), \( K_i=6 \)
Figure 5: Performance of CHB with Linear Load (5 and 7 Level CHB)

Figure 6: Performance of CHB with Non-Linear Load (5 and 7 Level CHB)
Figure 7: Performance of CHB with Increase in Non-Linear Load (5 and 7 Level CHB)

Figure 8: Performance of CHB with Linear and Non-Linear Load (5 and 7 Level CHB)
REFERENCES


