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Low Voltage Low Power Folded Cascode OTA Design For RF Applications

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Abstract

This paper deals with the design of a folded cascode operational transconductance amplifier (OTA) intended to be used for low power and wide band radio frequency (RF) applications. First, a detailed description of the OTA topology is done in order to optimize the MOS transistor sizing. Second, the folded cascode OTA, which works for frequencies that lead to a base band circuit design used for RF application, is optimized using the transistor sizing methodology. Simulation results are performed using Advanced Design System tool with 0.18µm CMOS process. The designed folded cascode OTA has a 73 dB DC gain and provides a gain bandwidth product of around 2.3 GHz. The input-referred in-band noise density (IRN) is 2.6nV^2/Hz and the output-referred noise (ORN) of 6.2 nV^2/Hz. The designed circuit consumes only 0.5 mW under a 1.8V supply voltage. Based on the optimized circuit, we have implemented a second order Gm-C filter. The simulation results indicate that this filter achieves a Band pass of 737 MHz.

Keywords: Folded cascode OTA, low power, optimization, Heuristic Algorithm, wide band RF application, secGm-C filter.

INTRODUCTION

Nowadays, due to the increasing demand of system on chip (SoC) productions, high performance analog integrated circuit design such as operational transconductance amplifier (OTA) in CMOS technology becomes a big challenge. The OTA circuit is well known for its high bandwidth in open-loop configuration [1], which makes it proper for widespread application such as Bluetooth, Global System for Mobile (GSM) Communication, Wide Band Code Division Multiple Access (WCDMA), Ultra Wide Band (UWB) are used in multimode transceiver.

In the literature, we show that the OTA is one of the most important building blocks in many analog circuit applications, such as including multipliers [2,3], continuous-time - filters [4, 5], voltage-controlled oscillators (VCOs) [6] and continuous time sigma-delta modulators [7]. This block converts input voltage to output current with a linear transformation factor.

The OTA should provide sufficient transconductance gain with acceptable linearity and power consumption. Moreover, a proper phase margin which guarantees the stability is needed. Also, the common mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR) represent two important specifications of an OTA. Therefore, there are some tradeoffs between bandwidth, phase margin, CMRR, PSRR, gain, linearity and power consumption when designing the OTA design.

Operational transconductance amplifiers are very useful building blocks in analog integrated circuits with an wide range of applications like continuous-time filters, data converters, variable gain amplifiers and tunable signal generators [8, 9] etc. Very often the transconductance amplifiers are characterized in terms of achievable linearity over a significant input range along with low noise and current consumption.

Our target was to design a folded cascode OTA circuit and its application in GM-C filter for wide band radio applications.

This paper is organized as follows. The operation of the folded cascode OTA architecture was introduced in section II where the characterization of the OTA circuit is detailed. The optimization strategy is presented in Section III together with optimized characteristics for the OTAs. Simulation results are reported in section IV. In section V, we have implemented a Gm-C low-pass filter. Finally, the conclusion drawn from this work and possible future works are presented in Section VI.

THE FOLDED CASCODE OTA ARCHITECTURE

A. PMOS Input Transistor

Depending on system needs, OTA circuit with a wide differential input range and good G_m is highly desired. For this reason, the PMOS transistor has been chosen. For comparable device dimensions and bias currents, the NMOS input differential pair provides larger gain than a PMOS pair. But, PMOS transistors input pair was used in the FC OTA in order to achieve a maximum gain and a low noise [10]. In this paper, an optimized OTA is presented to improve input dynamic range which operates at a low supply voltage with reduced power consumption.

B. Architecture Analysis

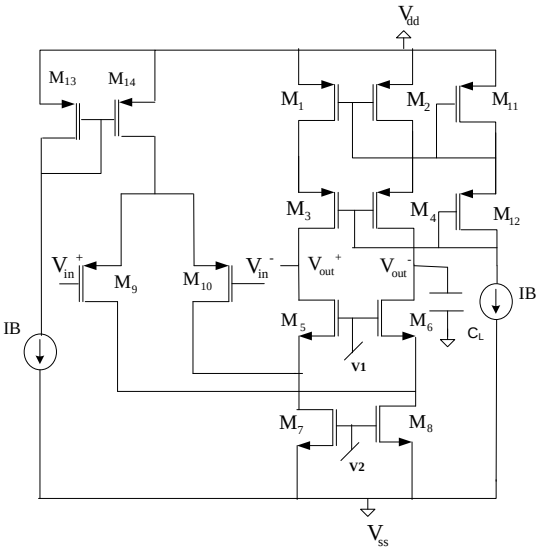

Figure 1: Folded cascode OTA circuit

The FC OTA has a differential stage consisting of PMOS transistors M_9 and M_{10}. M_{11} and M_{12} devices provide respectively the DC bias voltages to M_1, M_2, M_3 and M_4 transistors.

The open-loop voltage gain and the dominant pole are given by equations (1) and (2),

$$A_v = g_{m9}\left(\frac{g_{m3}}{g_{ds1}}.\frac{1}{g_{ds3}} // \frac{g_{m5}}{g_{ds5}}.\frac{1}{g_{ds7}+g_{ds9}}\right) \quad (1)$$

$$f_{dp} = \frac{1}{2\pi\left(\frac{g_{m3}}{g_{ds1}}.\frac{1}{g_{ds3}} // \frac{g_{m5}}{g_{ds5}}.\frac{1}{g_{ds7}+g_{ds9}}\right)C_L} \quad (2)$$

Where, g_{ds1}, g_{ds3}, g_{ds5}, g_{ds7} and g_{ds9} are respectively the conductances of M_1, M_3, M_5, M_7 and M_9 transistors. g_{m3}, g_{m5} and g_{m9} are respectively the transconductances of M_3, M_5 and M_9 devices and C_L is the capacitance at the output node.

C. Gain-Bandwidth

The gain bandwidth of the folded cascade OTA proposed given by (3):

$$GBW = \frac{g_{m9}}{I_D}\frac{I_D}{C_L} \quad (3)$$

Where gm_9 is the transconductance of transistor M_9. I_D is the bias current flowing in Mosfets M_4, M_6, and M_9. The gain bandwidth is normally much larger than the required, for low bandwidth applications.

D. Noise Analysis

E. There are two main types of noise that transistors contribute to the total circuit. They are the flicker, or 1/f noise and the thermal noise. Their effect must be minimized. In the following noise analysis, the noise contribution from the cascode transistors is neglected when compared to cascaded transistors.

The input referred thermal noise voltage of the FC OTA can be expressed as,

$$\overline{V_{in,th}^2} = 4KT\left(2\frac{2}{3g_{m9,10}} + 2\frac{2g_{m9,10}}{3g_{m9,10}} + 2\frac{2g_{m7,8}}{3g^2_{m9,10}}\right) \quad (4)$$

Where K is the Boltzmann's constant and T is the temperature. g_{m7} is the transconductance of M_7 transistor. The input referred flicker noise voltage of the FC OTA can be written as:

$$\overline{V_{in,1/f}^2} = 2\frac{KF}{C_{ox}(WL)_{1,2}f} + 2\frac{KF}{C_{ox}(WL)_{7,8}f}\frac{g_{m1,2}^2}{g_{m9,10}^2} + 2\frac{KF}{C_{ox}(WL)_{7,8}f}\frac{g_{m7,8}^2}{g_{m9,10}^2} \quad (5)$$

Where KF is the flicker noise coefficient of NMOS and PMOS transistors, f is the frequency and C_{ox} is the oxide capacitance. W and L are the transistors sizes. g_m defines the transconductance of transistors differential pair.

THE FOLDED CASCODE OTA OPTIMIZATION

In order to optimally size each component forming the OTA when satisfying constraints and performance functions, we developed an algorithm that allows automating the task [11]. This algorithm was programmed using C++ software. It is based on the flow chart given by figure 2. It describes an optimization tool based on Heuristic algorithm. The first step in the optimization is the expression of the different criteria by a technology dependent model. For accurate modeling, a small signal analysis of the OTA is carried out to explicit the different characteristics intended optimized. From the OTA structure presented in Figure 2, we opted in this step for the TSMC CMOS 0.18µm process.

A. Optimization Algorithm

The heuristic method allows solving an optimization problem. The optimization strategy is shown in Fig.2. First, we fix the parameters to optimize and their ranges of variations. Second, we generate random variables vectors and we check the preliminary conditions. The computation of the objective function to minimize or to maximize yields to optimal values of width and length of devices used, also the optimal bias current is attained.

B. Folded Cascade OTA Optimization

We used in the OTA optimization the following series of criteria:

- The gain A_v is maximized.
- The dominant frequency (f_{-3db}) is maximized.
- The input referred noise ($V_{in,th}$) is minimized.
- The power consumption (power) is minimized.
- The silicon area is minimized.

The objective function to maximize can thus be formulated as follows:

$$F = a_1 A_V + a_2 f_{-3dB} + \frac{a_3}{V_{in,th}^2} + \frac{a_4}{power} + \frac{a_5}{W_i L_i} \qquad (6)$$

Where $a_{1\text{-}5}$ are the positive coefficients used for normalization. The first step in the optimization is the expression of the different criteria by a technology dependent model.

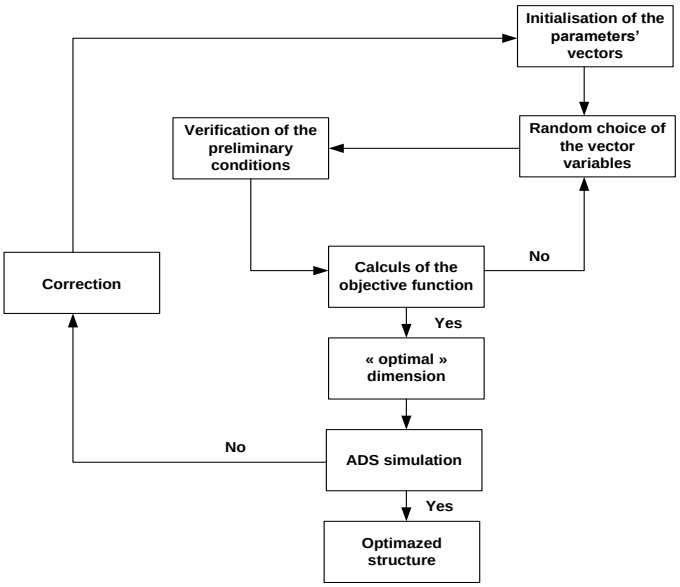

Figure 2: Optimization Algorithm flow chart

After several iterations, many valid vectors test were obtained. The transistors sizing of the OTA circuit are planned in table I.

Table I. Transistors Sizing

OTA circuit	
Device Name	***Values (µm)***
$M_{1,2,3,4,\ 11,12,\ 13}$	1
$M_{5,6,\ 7,8}$	5
$M_{9,10}$	20
M_{14}	15
Simulation Conditions	
IB	[5, 50] µA
V1	[-0.9, 0.9] V
V2	[-0.9, 0.9] V
C_L	0.1pF

The proposed OT A cell is simulated using the Advanced Design System (ADS) tool with TSMC 0.18µm CMOS process parameters under 1.8V power supply. The NMOS and the PMOS transistor threshold voltages are respectively 0.436 V and -0.438 V. The optimized value of bias current is set to 50 µA. Current sources are implemented using cascode current mirrors.

OTA CIRCUIT SIMULATIONS

The designed folded cascode OTA has a gain of 73.57dB, a large unity-gain frequency of 2.3GHz (Fig.3). Fig.4 presents the phase margin of 52degrees.

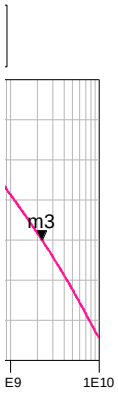

Figure 3: Gain curve of the optimized OTA

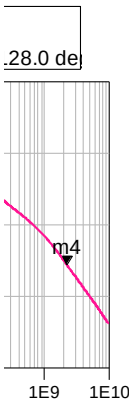

Figure 4: Phase curve of the optimized OTA

Fig.5 shows that the input referred noise (IRN) value of the proposed OTA over the 1-3GHz frequency band. The OTA input referred noise is around 2.6nV^2/Hz. Fig.6 depicts the output referred noise (ORN) value of the proposed OTA over the 1-3GHz frequency. The OTA output referred noise is around 6.23nV^2/Hz.

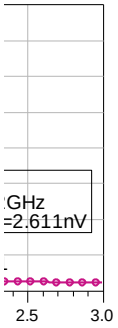

Figure 5: Input-referred noise curve

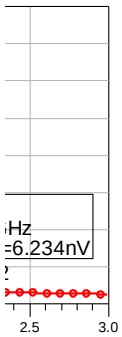

Figure 6: Output-referred noise curve

A comparative study of the optimized OTA with other works published is depicted in Table II.

After discussing the different performance of the designed OTA, we can evaluate our study toward other works. It is clearly seen that with folded cascode OTA architecture, we can reach a low power low voltage topology with high unity gain frequency.

To evaluate this work a figure of merit (FOM) can be defined as [12]:

$$FOM = \frac{Gain(GBW)}{(PowerSupply)(PowerConsumption)} \quad (7)$$

Table II: Comparison with recent works

Parameters	[13]	[14]	[15]	This work
DC Gain (dB)	85	--	84.33	73.57
Unity-gain frequency (GHz)	0.23	5	0.54	2.28
Phase Margin (degree)	46	--	51.34	52
IRN (μV2/ Hz)	1.6	28	--	0.002
ORN (μV2/ Hz)	35	--	--	0.006
Supply Voltage	2	1.8	--	1.8
Power consumption (mW)	--	0.45	1.2	0.5
CMOS Process (μm)	0.35	0.18	0.18	0.18
FOM (dB.MHz/V.mW)	--	--	--	2052

APPLICATION

The overall performance of a wireless device greatly depends on the performance of its transceiver [16-19]. RF filters are the essential components of all wireless transceiver front ends as shown in fig. 7. To design band pass filter with high quality factor, inductors play an important role [20]. Higher cost that came from large size of silicon area to entertain on-chip passive spiral inductors is one of the prime disadvantages. Another disadvantage of on-chip spiral inductor is its deficiency of tuning ability which makes the design a little bit complicated [21]. As a result the usage of on-chip spiral inductors is decreasing day by day for high frequency applications [22].

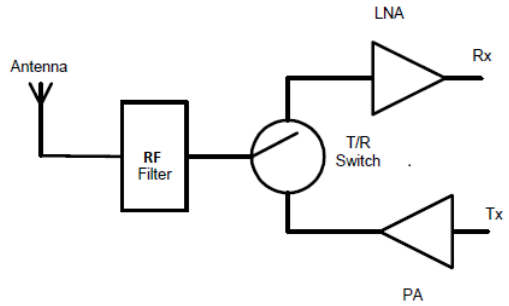

Figure 7: RF filter at the transceiver front end

Fully integrated continuous-time transconductance-C (Gm-C) filters have been widely used for high frequency applications such as digital video, RF/IF filters, etc. Gm-C filters offer many advantages in terms of low power and high frequency capability.

A Gm-C filter is a kind of the continuous time filter which needs the operational transconductance amplifier (OTA) to be a basic building block. Gm-C filters are popular for on-chip applications due to their advantages of high frequency performance and low power consumption, but have linearity problems. In order to overcome the disadvantage of linearity of Gm-C filters, many linearization techniques for transconductors have been reported such as resistive source degeneration, dynamic source Degeneration, tunable feedback, combination of dynamic source degeneration and tunable feedback, transconductor with bias feedback etc. Besides the non-ideality of the transconductors causes excessive phase shift and inherently limits the upper

operational frequencies, which restricts this type of filter from being used in gigahertz frequencies.

In our case and to demonstrate the feasibility and the performance of folded cascode OTA, we simulated several applications. We have treated current mode and voltage mode filters. Recently, analog filters design using Gm-C integrators has acquired a great popularity. Tranconductance cells are relatively simple circuits which allow to operate for high frequencies.

The reason behind the selection of Gm-C concept is that the easy tuning capability by varying the Gm value of the transconductors. Also the Gm-C filter has a low noise floor but the ability to handle large signals is limited. In order to archive the required value in terms of linearity, the Gm which depends on the width, the length and the bias current of the CMOS transistor, has to be chosen carefully. The fully differential circuit block is shown in fig. 8.

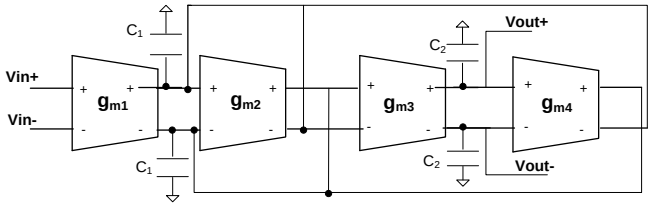

Figure 8: 2nd order Gm-C low pass filter circuit

The basic Gm-C filter, consisting of a capacitor and a transconductance, is shown in Fig. 8 and the transfer function of is given by [13]:

$$H_{(S)} = \frac{V_{out}}{V_{in}} = \frac{\frac{g_{m2} \cdot g_{m3} \cdot g_{m4}}{g_{m4}}}{S^2 + \frac{g_{m2}}{C_1} S + \frac{g_{m3} \cdot g_{m4}}{C_1 C_2}} \quad (7)$$

The common transfer function of 2nd order low pass filter (LPF) is

$$H_{(S)} = \frac{{\omega_0}^2}{S^2 + \frac{\omega_0}{Q} S + {\omega_0}^2} \quad (8)$$

The corner frequency ω0 and the quality factor Q of the circuit can obtain as:

$${\omega_0}^2 = \frac{g_{m3} \cdot g_{m4}}{C_1 C_2} \quad \frac{\omega_0}{Q} = \frac{g_{m2}}{C_1} \quad (9)$$

The simulation's result of Gm-C low pass filter is shown in fig. 9. With the following passive elements C_1=0.5pF and C_2=1pF, the obtained cutoff frequency is 737MHz. Thanks to this large cutoff frequency, the Gm-C filter can operate in RF application and modern communication receivers. This filter is able to re-configure the bandwidth, gain or linearity in order to fulfill the requirements of different standards subjecting to wireless standards.

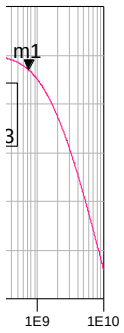

Fig. 9. Simulation result of 2nd order Gm-C low pass filter circuit

CONCLUSION

In this paper, a design of folded cascode OTA circuit has been reported. The approach of optimization OTA design has been used to improve the gain, the unity gain frequency, the input referred noise and the power consumption. Simulation results prove the effectiveness of this optimization approach which is a time consuming method. The optimized topology achieves a good input range with a high DC gain of 73.57dB and a large bandwidth. It consumes only 0.5 mW under 1.8V supply voltage. Based on this circuit, we have implemented a Gm-C low-pass filter where the cutoff frequency is 737MHz.

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