International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 13 (2017) pp. 4004-4008

Performance Analysis of Hexagonal Node Design For Packet-Switched NoC on FPGA

Shilpa K Gowda[1] and Dr. Rekha K.R.[2]

[1]Research Scholar, Jain University, Bangalore, India.

[2]Professor ECE Dept. SJBIT, Bangalore, India.

[1]ORCID: 0000-0002-5004-6045

Abstract

The NoC Architecture plays crucial role while designing communication systems for System on Chip (SoC). The NoC architecture is improved over conventional bus, shared bus design and cross bar interconnection architecture for on chip networks. In most of the NoC architecture contains mesh, torus or other topologies to design reliable router. But most of the designs are fails to improve the Quality of Service, Congestion problems, Chip, cost and mainly design throughput, area overhead and latency. In this paper we are trying to improve the above constraints by using hexagonal node architecture for packet switched Network on Chip (PS-NoC). By using Hexagonal node structure in Network, it provides better communication between the other nodes, avoids the congestion problems, network is traffic free while transmitting the packets across the on chip networks. Our design is dynamically reconfigurable for most of the on chip networks. To design hexagonal node we are using priority encoder and Deterministic XY routing algorithm. Our proposed design improves the hardware complexity in on chip networks.

Keywords : On chip Network, SoC, FPGA, NoC, Router, PE, Dynamic reconfiguration., Hexagonal pattern ,arbiter, FIFO ,Cross bar switch, packet switch, XY routing.

INTRODUCTION

In order to design SoC architecture on VLSI Technology, industry was facing lot of difficulties to provide the high bandwidth for parallel communication and energy consumption for the systems, because these methods are tradition in nature

[1].The years move on engineers are developed new communication architecture, their computation is cheaper, but encounter new problems with electrical, power problems. So the solution was founded others [2], this helps to design and emerges new notion called NoC [3-4] This paper is summarized as follows. The basic NoC architecture is explained in section 2.The proposed Hexagonal node pattern Packet-Switched Network-on-Chip (PS-NoC) is explained in detail with routing algorithm in section 3. The simulation results, design utilization and timing analysis of for single hexagonal node and complete PS-NoC are analyzed along with comparison results in Section 4. Section 5 tells about the conclusion of the proposed design work.

THE BASIC NoC ARCHITECTURE

In any NoC router is main part of the NoC and it plays a crucial role in data processing from one node to other node. The general architecture of NoC Router is as shown in the figure 1. It contains FIFO Buffers, Arbiter Module and cross bar switch.

The FIFO Buffers are used to store the data temporarily and based on the write and read operation will indicate the whether the FIFO is full or empty. The FIFO is mainly used to synchronize all the incoming packets in proper timings. Here in below figure, the FIFO Buffer contains 5 different input ports: local, east, west, south and north. Based on the read signal generated through arbiter gives you the FIFO outputs.

The Arbiter is used generate the grants based upon the requests. They are used control line for channel arbitration to make routing decision. The FIFO output generates the packets and arbiter extracts the source and destination address from the same packets and generates the grants to select the corresponding packets and finally gives the output through crossbar switch. Channel arbitration is controlled from arbiter module and it avoids the contention problem [6, 7]. The arbiter holds all the status of ports includes which port is communicating, which one is in waiting state, which port is not connected. The two or more input ports want to process the same output port, and then arbiter decides based on priority input request.

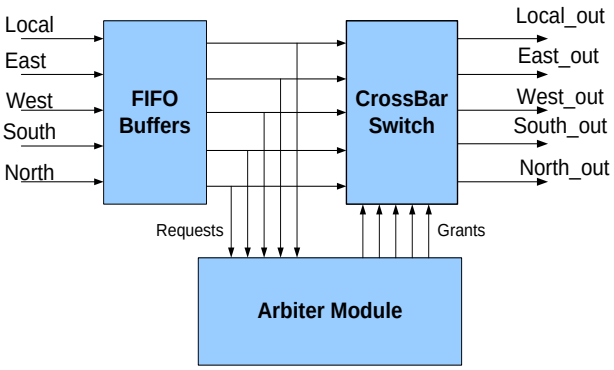

Figure 1: Basic Architecture of NoC Router

Arbiter holds the new packets which are connected to crossbar switch until router last packet transmission. Based on round robin schedule, if the data is already serviced gets lowest priority [8] [10]. Crossbar switch access the port data based on select line which is provided by the arbiter. Sometimes packets are not arrived according to the scheduled time, and then process will be incomplete. The routing process halts some time. This will be arises the live lock problems [9].

PROPOSED HEXAGONAL NODE PATTERN

The proposed Hexagonal node pattern Packet-Switched Network-on-Chip (PS-NoC) is shown in figure 2. The Hexagonal node pattern is used in packet switching NoC to improve the communication between the internal routers. Compared to the normal node, a hexagonal node avoids the bus based interconnection module limitations. The complete Hexagonal node module is used in most of the dynamic reconfigurable NoC's. The Single Hexagonal Node Pattern for PS-NoC is designed and shown in figure 3 and its Detailed Internal architecture is shown in figure 4.

The Single Hexagonal Node contains total 7 inputs (Local in and in1-in6) each is 48-bits and 7 outputs. In that single local output which is 32-bit and 6 outputs (out1-out6) each is 48bits.the whole architecture is working based on the priority encoder and routing algorithm.

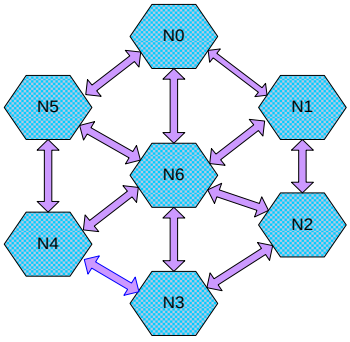

Figure 2: Hexagonal node pattern Packet-Switched Network-on-Chip (PS-NoC)

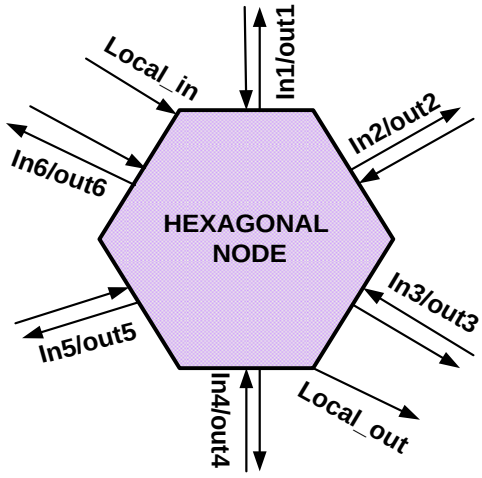

Figure 3: Single Hexagonal Node Pattern for PS-NoC

The priority encoder is contains seven input ports are shown in figure 4. The priority encoder works based on the select line information. The select line is taken from the input packet MSB bits i.e 47th bit which are 7-bits. If the select line is 0000_001 then local input will be select as packet to the routing algorithm.

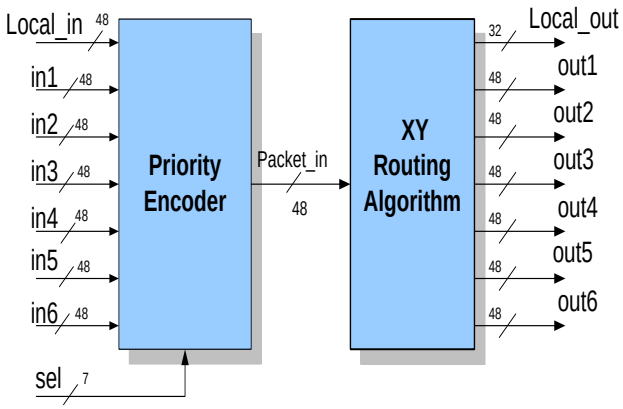

Figure 4: Detailed Internal Architecture of Single Hexagonal Node Pattern

The Generally Routing algorithm is used to select the packets in any of the east, west, south and north directions. Here we are using XY Routing algorithm and its flow is as shown in the figure 5.

The XY- algorithm is distributive-deterministic routing algorithm, which is used to avoid the network congestion problems and it transmits the packet either through y-axis direction or x-axis direction. If we use this deterministic algorithm, it provides the traffic free network to improve the

high throughput, low latency of the router design [11- 13].

The flow of XY-routing algorithm is as follows: For XY algorithm here we are introduces Z-Axis also for Hexagonal node structure to improve the communication between the node structure. Firstly it checks the current address Z is matches with destination address z of the router packets, if it matches , Then it will check x axis direction and then y-axis direction, if all the destination and current address are matched, then packet output will be generated in local output. if it is not matched, then checks others ports. If current address y is greater than the destination address y, packet will be allocated to out1 else out2. If it is not matched, then it checks others ports. If current address x is greater than the destination address x, packet will be allocated to out3 else out4. . If it is not matched, then it checks z-axis. If current address z is greater than the destination address z, packet will be allocated to out5 else out6.

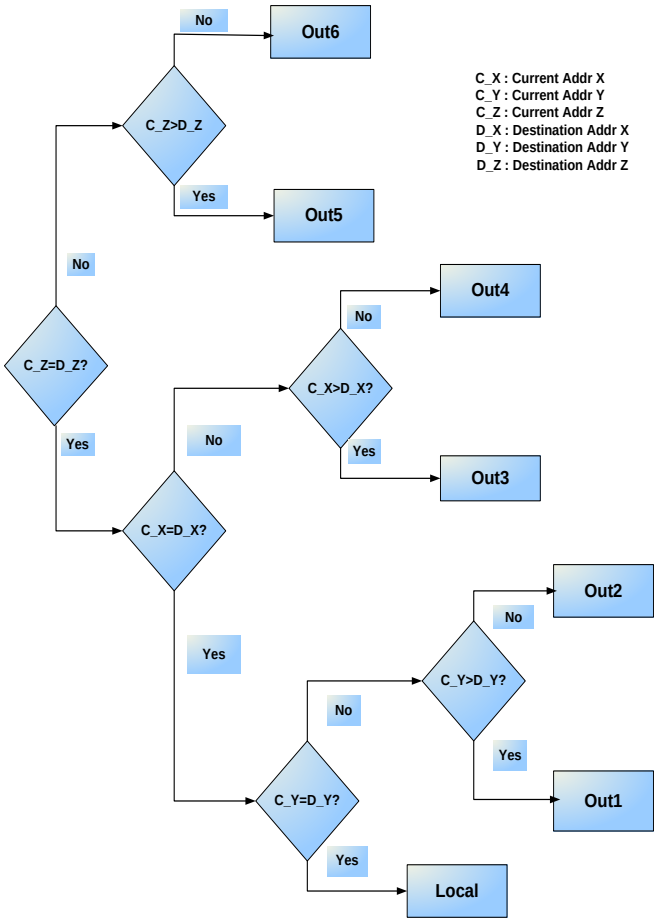

Figure 5: Flow of XY-Routing Algorithm

RESULTS AND ANALYSIS

The complete Hexagonal Packet switched NoC is designed and implemented on Xilinx 14.7 ISE and Simulated using Modelsim 6.3f. For implementation we are using Artix 7 Device: 100T, Speed:-3 and Package: CSG 324.

The Figure 6 shows the simulation results of single Hexagonal Node6. It contains all the 7 48-bit inputs including local packet and 6 48-bit outputs and single 32-bit local packet output. We can see the time taken to process one input and its generation of output in figure 6. It has taken 1 and half clock cycles to process the operation. Each clock period is 5ns.

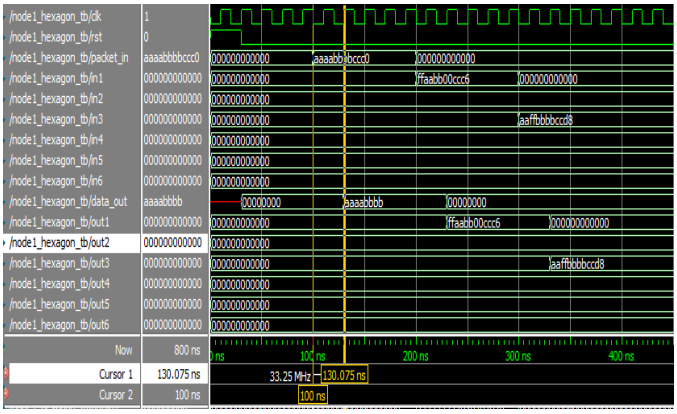

Figure 6: Simulation results of Single Hexagonal Node Pattern for PS-NoC with timings

The table 1 and 2 shows the single Hexagonal Node design utilization using different FPGA's and Timing analysis of design respectively.

Table 1: The Proposed Single Hexagonal Node Design summary using Different FPGA's–Spartan-3, Viterx-5 and Artix-7.

Logic Utilization	XC3S400-5 PQ208	5VLX110T-3 FF1136	7A100T-3CSG324
Number of Slice Registers	273	218	221
Number of Slice LUTs	217	328	355
Number of fully used LUT-FF pairs	439	176	217
Number of bonded IOBs	658	658	658
Number of BUFG/BUFGCTRLs	1	1	1

Table 2: The Proposed Single Hexagonal Node Timing Analysis using Different FPGA's–Spartan-3, Viterx-5 and Artix-7.

Timing parameters	XC3S400-5PQ208	5VLX110T-3 FF1136	7A100T-3CSG324
Minimum period (ns)	6.797	1.894	1.648
Maximum Frequency (MHz)	147.134	538.119	606.794
Setup time (ns)	10.833	4.579	2.51
Hold Time (ns)	6.216	2.775	0.645

The Figure7 shows the simulation results of Complete Hexagonal PS-NoC for figure 2. It contains all 7 node 48-bit inputs local packets and all 7 node 32-bit local packet outputs.

To process each node input it has taken 1 and half clock cycles. Each clock period is a 5ns.This simulation result proves better latency of complete Hexagonal PS-NoC.

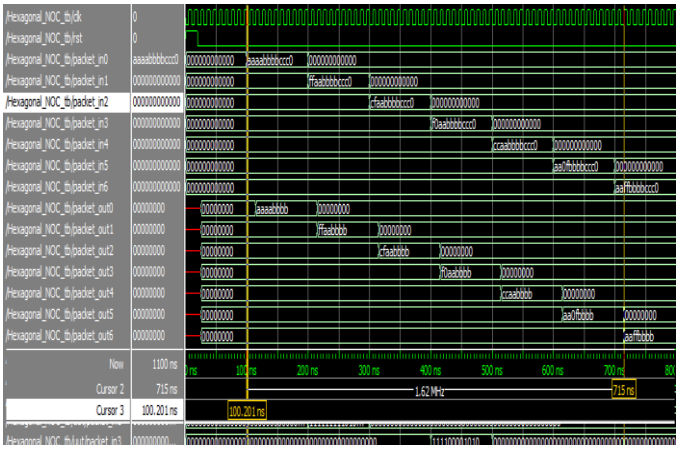

Figure 7: Simulation results of Hexagonal [all 7-Nodes] PS-NoC with timings

The table 3 and 4 shows the complete Hexagonal PS-NoC [Including all nodes] design utilization using different FPGA's and Timing analysis of design respectively

Table 3: The Proposed Hexagonal NoC Design summary using Different FPGA's–Spartan-3, Viterx-5 and Artix-7.

Logic Utilization	XC3S400-5 PQ208	5VLX110T-3 FF1136	7A100T-3CSG324
Number of Slice Registers	930	1224	910
Number of Slice LUTs	1224	1338	998
Number of fully used LUT-FF pairs	1702	1192	875
Number of bonded IOBs	562	562	485
Number of BUFG/BUFGCTRLs	1	1	1

Table 4: The Proposed Hexagonal NoC Timing Analysis using Different FPGA's–Spartan-3, Viterx-5 and Artix-7.

Timing parameters	XC3S400-5PQ208	5VLX110T-3 FF1136	7A100T-3CSG324
Minimum period (ns)	9.639	2.297	1.89
Maximum Frequency (MHz)	130.901	435.265	528.996
Setup time (ns)	10.183	2.752	1.711
Hold Time (ns)	6.216	2.783	0.645

The table 5 proves the proposed Hexagonal NoC design includes 7 individual nodes utilizes less number of Slices, Slice Register's and Slice LUT's compared to basic NoC 2x2 Design[5] includes 4 individual nodes concludes the better area improvement.

Table 5: Comparison of The Proposed Hexagonal NoC [7-Nodes] with previous [5] design 2X2 NoC [4-Nodes].

Device : Sparan 3E -5 Package: FG320		PROPOSED DESIGN		BASIC NOC DESIGN	
Logic Utilization	Available	Used	Utilization	Used	Utilization
Number of Slice Registers	4656	928	19%	2873	61%
Number of Slice LUTs	9312	1223	13%	2793	29%
Number of fully used LUT-FF pairs	9312	1699	18%	4076	43%
Number of bonded IOBs	232	562	242%	100	43%
Number of BUFG/BUFGCTRLs	24	1	4%	1	4%

CONCULSION

In this Paper, we are concluding hexagonal node pattern for packet switched NoC is mainly used in on chip networks which dynamically reconfigurable in nature. The main purpose of hexagonal node is used to improve the communication between nodes. The results are analyzed and design utilization and timing of single and complete hexagonal PS-NoC with different FPGA's are shown above tables. The slice utilization is improved over 40% when compared to normal NoC design architecture. Overall the complete proposed architecture suits to on-chip networks. In future we can design fault-elimination network in complete hexagonal NoC.

REFERENCES

[1] T. Bjerregaard and S. Mahadevan, "A survey of research and practices of Network-on-chip," ACM Computing Surveys, vol. 38, Jun. 2006.

[2] L. Benini and G. De Micheli, "Networks on chips: a new SoC paradigm," Computer, vol. 35, p. 70-78, 2002.

[3] P. Guerrier and A. Greiner, "A generic architecture for on-chip packet-switched interconnections," Proceedings of the conference on Design, automation and test in Europe -DATE '00, p. 250-256, 2000.

[4] Takieddine SBIAI and Kazuteru NAMBA, "*NoC Dynamically Reconfigurable as TAM",* Chiba, JAPAN, IEEE 21st Asian Test Symposium, 2012.

[5] H . Thang, Ph. Nam," Prototyping of a Network-on-Chip on Spartan 3E FPGA" , 2nd International Conference on Communications and Electronics, 2008 (ICCE 2008), page.24-28, June 2008..

[6] Abdelrasoul, M., Ragab, M. , Goulart, V.” Impact of Round Robin Arbiters on router's performance for NoCs on FPGAs “IEEE International Conference on Circuits and Systems (ICCAS), page 59-64, Sept 2013.

[7] Abdelrasoul, M. , Ragab, M. , Goulart, V.” Evaluation of the Scalability of Round Robin Arbiters for NoC Routers on FPGA “, IEEE 7thInternational Symposium on Embedded Multicore Socs (MCSoC), page 61-66, Sept 2013.

[8] Gwangsun Kim, Lee, M.M.-J. , Kim, J., Lee, J.W., Abts, D., Marty, M.” Low-Overhead Network-on-Chip Support for Location-Oblivious Task Placement” Computers, IEEE Transactions on Volume: 63 , Issue: 6, 2014.

[9] Fischer, E., Fettweis, G.P.,” An accurate and scalable analytic model for round-robin arbitration in network-on-chip”, Seventh IEEE/ACM International Symposium on Networks on Chip (NoCS), page 1-8,April 2013.

[10] Stojanovic, I.Z., Jovanovic, M.D., Djordjevic, G.L.” Low-cost port allocation scheme for minimizing deflections in bufferless on-chip networks”, 21st IEEE international conference on Telecommunications Forum (TELFOR), page 357-360, Nov 2013.

[11] Wang Zhang, Ligang Hou , Jinhui Wang , Shuqin Geng ; Wuchen Wu”, Comparison Research between XY and Odd-Even Routing Algorithm of a 2-Dimension 3X3 Mesh Topology Network-on-Chip”, Intelligent Systems, 2009. GCIS '09. WRI Global Congress on Volume: 3, 2009.

[12] Ye Lu, Changlin Chen, McCanny, J. , Sezer, S,” Design of interlock-free combined allocators for Networks-on-Chip”, IEEE International conference on SoC Conference (SoCC), page 358-363, Sep 2012.

[13] Singh, J.K., Swain, A.K. , Reddy, T.N.K. , Mahapatra, K.K.,” Performance evalulation of different routing algorithms in Network on Chip”, IEEE Asia Pacific Conference on Postgraduate Research on Microelectronics and Electronics (PrimeAsia), 2013.