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FPGA Implementation of Ripple Carry and Carry Look Ahead Adders Using Reversible Logic Gates

K. Rajesh[1] and Prof. G. Umamaheswara Reddy[2]

Department of Electronics and Communication Engineering,
SVU College of Engineering, Sri Venkateswara University,
Tirupati, Andhra Pradesh, India.

[1]ORCID: 0000-0001-8246-1123

Abstract

Nowadays in the world of VLSI Technology, the word low power consumption is only possible with the concept of Reversible logic design. Reversible concepts will attain more attraction of researchers in the past two decades, mainly due to low-power dissipation and high reliability. It has received great importance due to because of there is no loss of information, while we are processing the data from input to output. Moreover, the power dissipation is also very less and ideally it should be zero. So the concept of reversible design will become more dominant in the low power VLSI design. This paper focuses on the implementation of 4, 8, 16 and 32 bits of highly optimized area efficient Ripple carry adder (RCA) and Carry look ahead (CLA) adders. Finally, we can prove that the Carry look ahead adders are so fastest among all the previously existing designs. All these processes will be Simulated & Synthesized on the ISE Xilinx 14.7 software and it is successfully tested & dumped on the FPGA [2] Spartan-6 kit.

Keywords: Reversible logic, RCA-Ripple Carry Adder, CLA-Carry Look Ahead adders, ISE-Integrated Synthesis Environment, FPGA-Field Programmable Gate Array.

INTRODUCTION

Adders, The basic elements in Electronics, which is even more basic elements for implementing the multiplication, division and subtraction, Thus it will be improving the addition speed and improve almost all the arithmetic operations in array processing, Arithmetic and Logical operations, multi operand addition is often encountered. In this way we have a basic adder is ripple carry adder but, there is a one main drawback is, it will take more time to propagate the data from input to Output i.e. delay is more dominant in nature. Due to because of The accumulated delay in ripple carry adders, it can be prohibitively large then we go for carry look ahead adders, with this we are improving the speed of addition and improve the speed of all other arithmetic operations also.

REVERSIBLE LOGIC DESIGN

One and only the major goal of Low power VLSI is the Reduction of power dissipation. When we come to the concept of conventional logic design method, while we are propagating the data from input to output, there should be a some part of data must be loss due to because of the power dissipation is very intense, finally we are not getting the proper reliable output from corresponding input, all these process of bit information losses is proved by Landauer [1]. Finally, we overcome all these drawbacks present in the conventional logic gates we go for the concept of reversible logic design. In this concept, there is a minute amount of power is dissipated practically, but it should zero in case of theoretical. Thus, there is no data loss in the propagation of the input to output.

Hence, in 1973 Bennett [2] showed that how to avoid the KTln2jouls of energy dissipation in the circuit designs. It can be possible with the each and every input bit of data will be recovered from the output that is why it is simply referred as reversible. Internally there is a one-to-one mapping is present on the reversible logic gate and it has an equal number of inputs and outputs, this is also one of the main reasons to reduce the data loss during the process of propagation.

GOALS OF REVERSIBLE LOGIC

- *Garbage Output:* The total number of unused outputs present in the design.
- *Number of reversible logic gates:* The Total number of reversible gates is used in the circuit.
- *Delay:* The Time taken by the propagation of inputs to the output, i.e. the speed of the circuit.
- *Ancillary bits:* The Total number of inputs which are maintained either constant 0 or 1 in order to get the proper output.
- *Quantum cost:* The number of 1X1 & 2X2 reversible logic gates or Quantum logic used in the design.

EXISTING REVERSIBLE LOGIC GATES

A. Feynman Gate

It is a 2*2 Feynman logic gate with the Quantum cost of 1 is shown in fig 1. It is also known as CNOT gate.

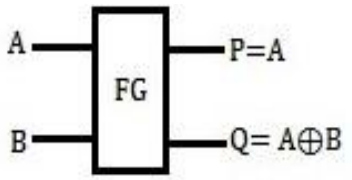

Figure 1: Feynman gate logic diagram.

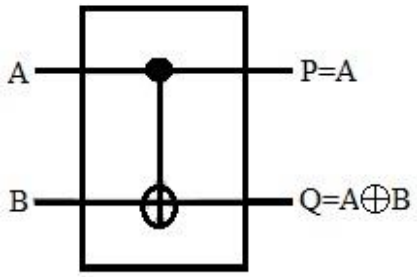

Figure 2: Quantum implementation of Feynman gate.

B. Double Feynman Gate

It is a 3*3 Feynman double logic gate with the Quantum cost of 2 is shown in fig 3.

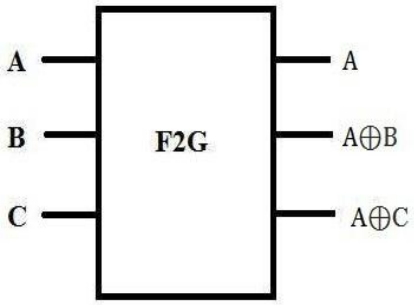

Figure 3: Double Feynman gate logic diagram.

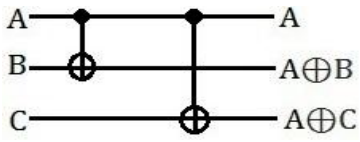

Figure 4: Quantum implementation of Double Feynman gate

C. Peres Gate

It is a 3*3 Peres logic gate with the Quantum cost of 4 is shown in fig 5.

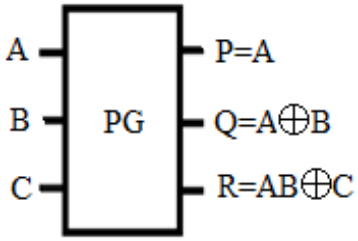

Figure 5: Peres gate logic diagram.

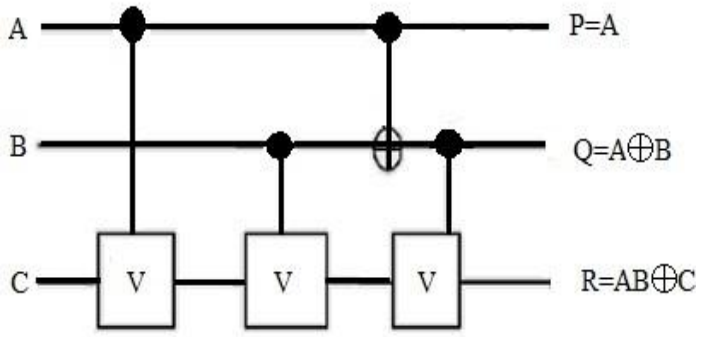

Figure 6: Quantum implementation Peres gate.

D. New Fault Tolerant Gate

It is a 3*3 NFT logic gate with the Quantum cost of 5 is shown in fig 7.

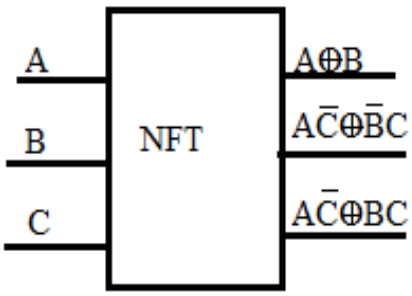

Figure 7: NFT gate logic diagram.

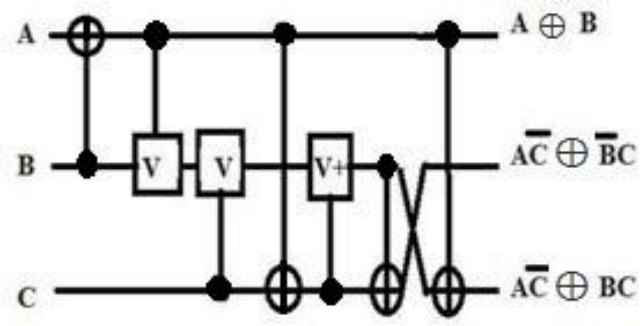

Figure 8: Quantum implementation NFT gate.

PROPOSED DESIGNS

A. Ripple Carry Adder

To designing the Ripple carry adder, the basic element is full adder. So firstly we can design a modified reversible full adder for getting the optimized results by using simple 3*3 Peres gate [10] only is shown in the fig 5. It is proved that the modified reversible full adder design can be realized with two garbage outputs and only on ancillary input. While we are designing the full adder, the 3rd input of the first Peres gate should be considered as zero. The output of the ripple carry adder is shown below.

$$Sum = A \oplus B \oplus C$$

$$Carry = (A \oplus B).\ C_{in} \oplus AB$$

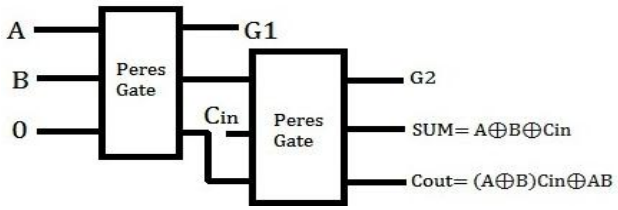

Figure 9: Full adder design using Peres gate.

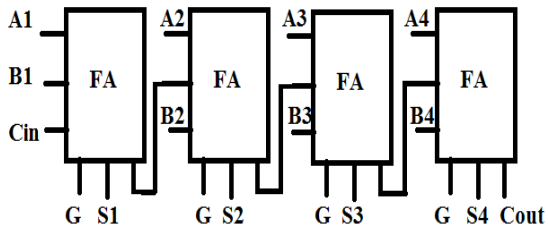

Figure 10: 4-bit full adder.

Table I: Truth table for full adder using peres gate.

A	B	C	G1	G2	SUM	C_{OUT}
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	1	0	0	1	1	0
0	1	1	0	1	0	1
1	0	0	1	1	1	0
1	0	1	1	1	0	1
1	1	0	1	0	0	1
1	1	1	1	0	1	1

RCA requires n-bit full adder design circuits, ripple carry adder propagates their individual carry input through each and every full adder circuit blocks. The output carry of the i^{th} full adder circuit is connected to $(i+1)^{th}$ full adder design circuit. Thus the coming next full adder circuit has to wait until the previous logic block to provide the carry for particular stage. Finally, it will provide the sum and carry afterwards the n-stages for n-bit RCA addition. The output of the first Peres gate is applied to the inputs of the second Peres gates respectively. Hence the sum and carry are generated at the final stages of the ripple carry design.

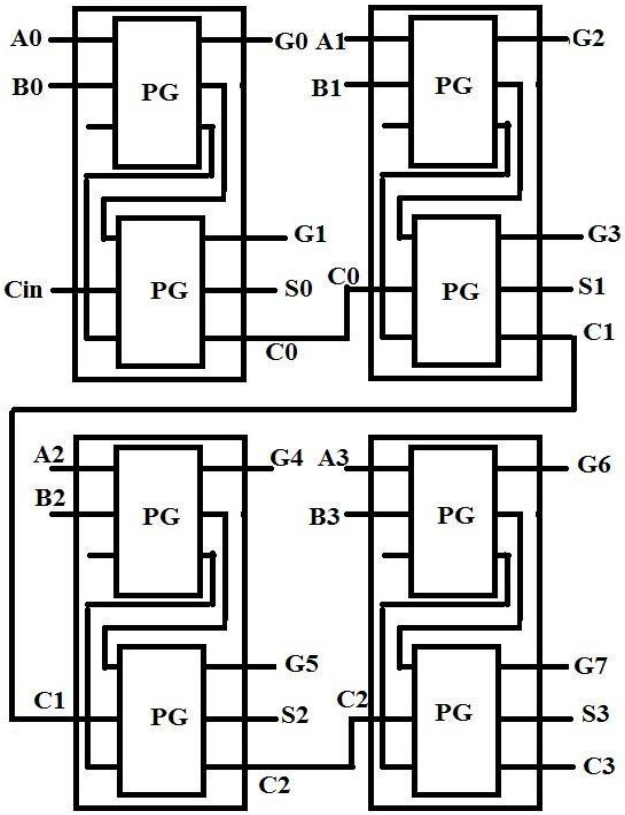

Figure 11: Proposed 4-bit Ripple carry adder.

This paper proposed the architecture for 4-bits of ripple carry adder only, but we can synthesize, simulate and FPGA implementation of remaining 8, 16, 32 bit ripple carry adders also. In this way it is possible to design any bit (n^{th}) of Ripple carry addition also. The simulation result of 32-bit ripple carry adder is shown in fig 13.

B. Carry Look Ahead Adder

Here we are designing basic elements of NFT [4] gate and Double Feynman gate for designing of CLA. The main purpose of selecting the NFT gate is that it preserving the parity bits, if there are no faults occurred in the signal level, then there is no need of requirement of intermediate signals. In this paper, we proposed a design and implementation of 32-bit CLA that is efficient in terms of delay, apart from these we

are designing 4,8,16 bits of CLA also and it can be simulated and compare the results of delay with the existing designs. There is no possibility that all the reversible logic gates will be preserved for parity bits, but both logic gates are used in CLA are parity preserving gates. Hence the whole design of adder preserves the parity.

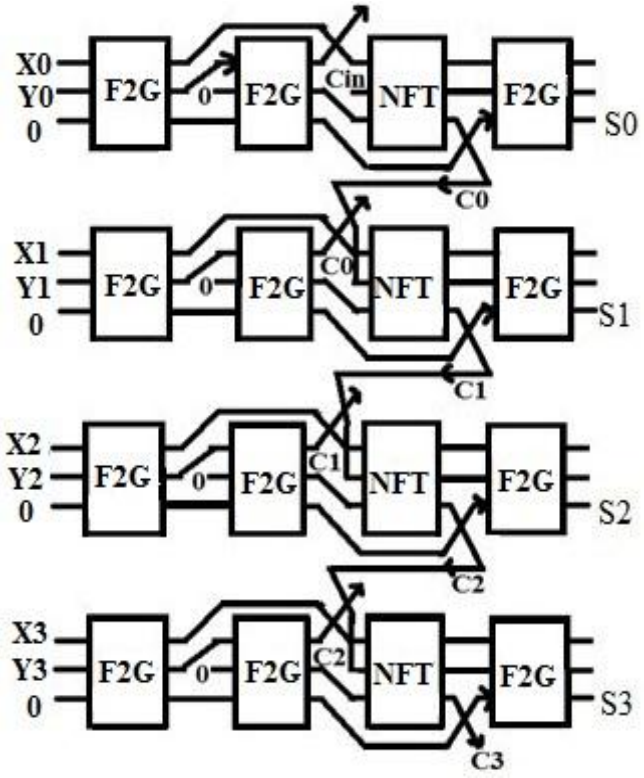

Figure 12: Proposed 4 bit Carry look ahead adder.

The basic purpose of the addition using CLA is to generate all incoming carries in parallel and to avoid the waiting until the propagation of carries from the previous stages of full adder. The simulation results of 32-bit carry look ahead adder is shown in fig 14.

SIMULATION RESULTS

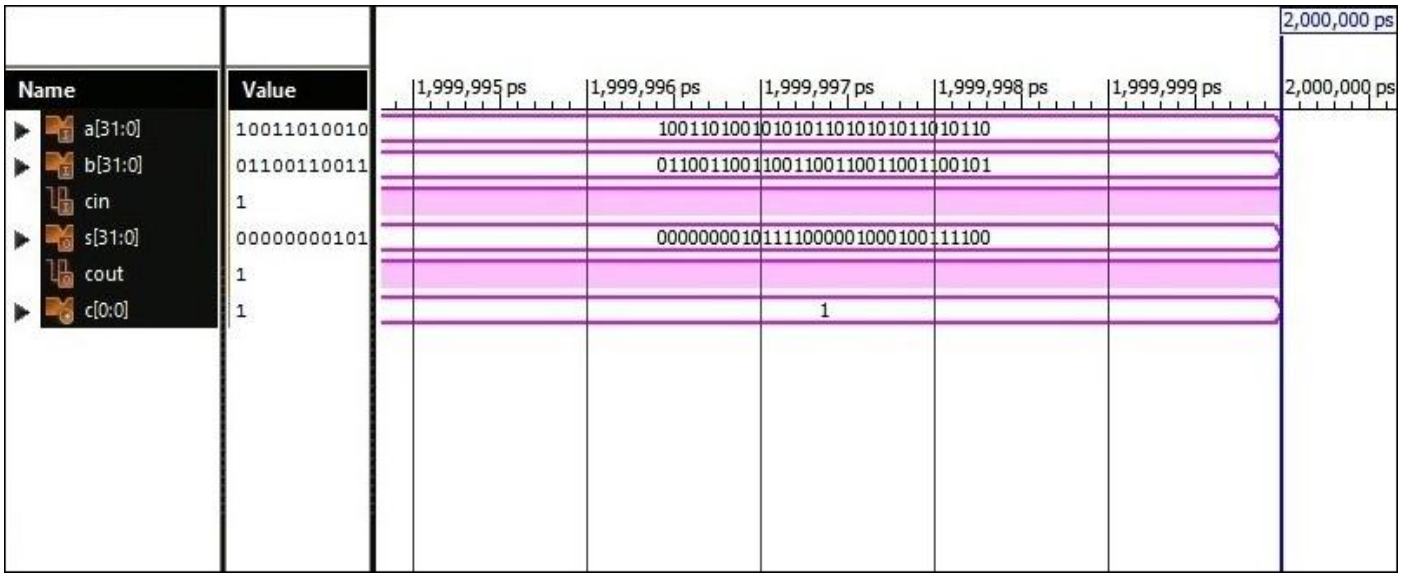

Figure 13: Simulation results for 32 bit Ripple carry adder.

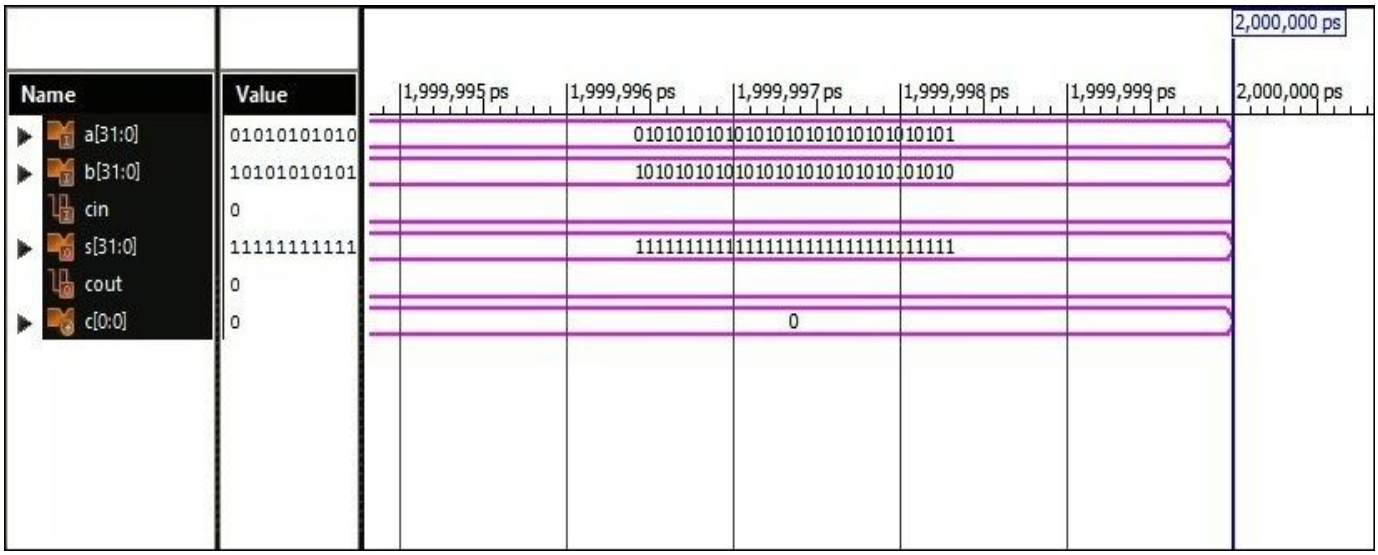

Figure 14: Simulation results for 32 bit Carry look ahead adder.

Table II. Performance Analysis Of Proposed Carry Look Ahead Adder And Existing Designs

S. No	Performance	4-Bit	8-Bit	16-Bit	32-Bit
1	Proposed design	6.637	8.751	13.14	22.58
2	Existing design[4]	50	14.53	-	-
	Improvement (%) with respect to [4]	86.72	39.77	-	-
3	Existing design[5]	8.29	12.81	-	-
	Improvement (%) with respect to [5]	19.93	31.60	-	-
4	Existing design[9]	10.04	14.13	21.30	33.96
	Improvement (%) with respect to [9]	33.94	38.08	38.30	33.51

All the values in the above table are measured in terms of delay (ns)

Table III: Comparative Results of Ripple Carry Adder with Carry Look Ahead Adder in Terms of delay (ns)

S.NO	N-Bit	RCA	CLA
1	4	8.95	6.637
2	8	13.20	8.751
3	16	28.74	13.14
4	32	38.66	22.58

ns = Unit of measuring delay

CONCLUSION

In this paper, we proposed the area efficient Ripple carry adder and Carry look ahead adder. The realization of the RCA & CLA is designed by using the basic full adder circuit, this can be realized by using two basic Peres gates only, that is the reason why only we can design these adders having less delay with comparison to the almost all the previous existing designs. It can be proved by comparing our proposed design to the existing design is shown in the above table. The highly optimized adders can be used furthermore has played a very crucial role in future development of Quantum computers. Whatever the design we are proposed in this paper, by using this it is possible to design any bit (n^{th}) of designing in RCA and CLA by simply cascading of each and every individual designs. Finally, we proposed an Ultra speed implementation of RCA and CLA.

FUTURE SCOPE

Nowadays, most of the researchers are focusing on achieving very less delay and to reduce the complexity of the circuit, this is providing a good environment for speed processing environments, not only the parameter of delay, we can put a more concentration on the Quantum cost [11] and Power dissipation. In the world of low power VLSI design everything is possible, might be in the future the full adder design is more precise than all the previous existing designs, then we may get the more ultra speed adders are designed well, it helps to design RCA and CLA are more optimized, so it is also very much needful in Quantum computing. Till now all the research work is done on reversible logic gates is proposed only in theoretically mode, might be in the future we put a more and more concentration on the fabrication of Reversible logic gates, Then we can change the complete

world of electronics.

REFERENCES

[1] "Irreversibility and heat generation in the computational process", IBM Journal of Research Development - R. Landauer 5pp, 183- 191, 1961.J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.

[2] LUT-Based FPGA-2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems-Mubin Ul Haque, Zarrin Tasnim Sworna† and Hafiz Md. Hasan Babu‡.

[3] "Logical reversibility of computation", IB.MJ.Res.Dev-C. Bennett 17 (1973), PP.525-532

[4] "An Efficient Approach for Designing a Reversible Fault Tolerant *n*-bit Carry Look ahead adder978-1-4799-1166-0/13. $00©2013IEEE – HafizMD,Hasambabu,lafifa and Nazir.

[5] "Design of high speed multiplier using Modified Booth Algorithm with hybrid carry look-ahead Adder" 2016 International Conference on Circuit, Power and Computing Technologies [ICCPCT] - Balakumaran R, Prabhu E

[6] "Fault Tolerant Reversible Logic Synthesis: Carry Look-Ahead and Carry-Skip Adders", July 15-17, 2009 Zouk Mosbeh, Lebanon, ACTEA 2009

[7] "Design of a Compact Reversible Carry Look-Ahead Adder Using Dynamic Programming" 2015 28th International Conference on VLSI Design and 2015 14th International Conference on Embedded Systems-Nusrat Jahan Lisa, Hafiz Md. Hasan Babu*

[8] "Design of a Novel Reversible ALU using an Enhanced Carry Look-Ahead Adder"- 2011 11th IEEE International Conference on Nanotechnology ,Portland Marriott ,August 15-18, 2011, Portland, Oregon, USA-Matthew Morrison, Matthew Lewandowski, Richard Meana and Nagarajan Ranganathan

[9] Reversible Adder Design For Ripple carry and Carry look ahead (4, 8, 16, 32-bit) –International Conference on Computing, Communication and Automation (ICCCA2016) - NeelamSomani. Chitrita Chaudhary, Sharad Yadav

[10] "Reversible logic and quantum computers", -A. Peres 1985.

[11] "Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage outputs,"ACM Journal on Emerging Technologies in Computing Systems - H. Thapliyal and N. Ranganathan, 2010.201.